ECE599: PLL-2 (Advance Clocking Techniques)

Course Objectives: Get to know about the state-of-the-art clocking architectures. Learn to read and present a paper. Analyze the state-of-the-art architectures and the problems they intend to solve. Understand the strength and weakness of the architectural and algorithmic choices made to solve a given problem. Learn to critique a paper. Improve upon an already existing state-of-the-art architecture or provide mathematical analysis of the architectural choices. Learn to write a research paper based on the improvements and analysis.

Classroom	STAG 261
Class time	M/W/F 10:00–10:50am
Instructor:	Tejasvi Anand, `anandt@eecs.oregonstate.edu`
Office:	KEC 4113, Ph: 541-737-4673
Office hours:	Friday 4:00-5:00pm (or by appointment)
Textbook:	No text book required
Prerequisites:	ECE599 PLL-1 or equivalent
Course website:	`https://web.engr.oregonstate.edu/~anandt/ECE599_Spring_2017`

Grading:

Project (Research Paper) 80%
In-class participation 20%

Reference books:

- B. Razavi, *RF Microelectronics*, Pearson, 2014.
- F. Gardner, *Phase lock Techniques*, John Wiley & Sons, 2005.
- D. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice-Hall, 1991.
- W. Egan, *Phase-Lock Basics*, John Wiley & Sons, 1998.
- R. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, McGraw Hill, 2003.

Reference papers: Posted online