ECE599: Phase Lock Loop

Course Description: Analysis and design of phase-locked loop (PLL) architectures and circuits for communication systems. Emphasis on fundamental understanding, design intuition, and implementation of PLLs in modern-day CMOS processes. Topics include acquisition, tracking, noise properties of PLLs, integer/fractional-N PLLs, digital PLLs, delay-locked loops, and clock and data recovery circuits.

Classroom	GBAD 103
Class time	T/TR 10:00–11:20am
Instructor:	Tejasvi Anand, `anandt@eecs.oregonstate.edu`
Office:	KEC 4113, Ph: 541-737-4673
Office hours:	Wednesday 2:00-3:00pm (or by appointment)
Textbook:	No text book required
Prerequisites:	ECE520 or equivalent
Course website:	`https://web.engr.oregonstate.edu/~anandt/ECE599_Wint_2016`

Grading:

Homework	30%
Midterm	30%
Project	35%
In-class participation	5%

Reference books:

- F. Gardner, *Phase lock Techniques*, John Wiley & Sons, 2005.
- D. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice-Hall, 1991.
- W. Egan, *Phase-Lock Basics*, John Wiley & Sons, 1998.
- R. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, McGraw Hill, 2003.

Reference papers: To be posted online