Energy efficient asymmetric binary search switching technique for SAR ADC

T. Anand, V. Chaturvedi and B. Amrutur

An asymmetric binary search switching technique for a successive approximation register (SAR) ADC is presented, and trade-off between switching energy and conversion cycles is discussed. Without using any additional switches, the proposed technique consumes 46% less switching energy, for a small input swing (0.5 $V_{ref\ P\text{-}P}$), as compared to the last reported efficient switching technique in literature for an 8-bit SAR ADC. For a full input swing (2 $V_{ref\ P\text{-}P}$), the proposed technique consumes 16.5% less switching energy.

Introduction: Owing to its low energy consumption, successive approximation register (SAR) ADCs are preferred for wireless and biomedical applications [1]. Of the three major building blocks of a SAR, the energy consumption of digital and comparator logic scales down with technology, but it is not the case with the capacitive DAC (including reference buffer). Energy consumption in the capacitive DAC depends on the total capacitance, input signal swing, and the switching technique used. For a given signal swing, noise and linearity requirements are the key factors which dictate the total capacitance. Switching technique, however, can play an important role in deciding energy consumption. By modifying the way capacitors are switched, switching energy can be reduced. Some of the recently proposed efficient switching schemes include V_{cm}-based switching [2] and monotonic switching [3]. In this Letter, we propose an energy efficient switching scheme based on an asymmetric binary search algorithm. The proposed scheme achieves switching energy efficiency by exploiting the switching energy and conversion cycle trade-off.

Asymmetric binary search switching technique: In a conventional binary search, for a positive input signal, after the sign comparison, the MSB capacitor is connected to V_{ref}. If the input is less than $1/2V_{ref}$, then either the complete or a part of the MSB capacitor is discharged by connecting it to ground. This discharge operation (down transition [4]) is the main cause of switching energy inefficiency in the conventional binary algorithm. Among various switching algorithms, linear search switching is the most switching-energy-efficient search algorithm, as shown in Fig. 1*b*, where one unit capacitor is connected to V_{ref} at a time. Linear search achieves its switching energy efficiency by ensuring that no capacitor is unnecessarily charged during the search operation. However, additional comparison operations equate to energy consumption in the comparator and digital logic. Moreover, for an n-bit SAR, linearly switching a unit capacitor at a time requires 2^n switches, as compared to 2^n switches in a conventional algorithm, and their corresponding drivers, which add to layout and digital logic complexity. Thus, the linear switching algorithm represents one extreme of the trade-off between saving in switching energy and energy dissipated during additional comparison cycles. Without using any additional switches, the proposed asymmetric search algorithm exploits this trade-off to save switching energy by slightly increasing the comparison cycles.

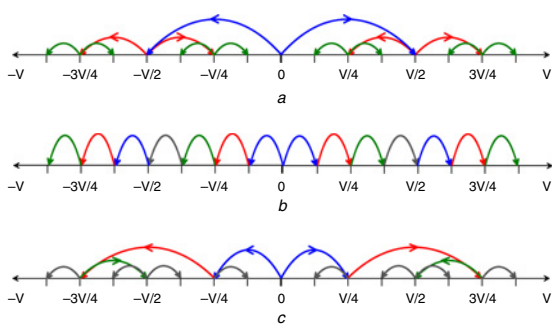

Fig. 1 *Comparison of asymmetric binary search algorithm with linear and conventional binary search algorithm*

a Conventional binary search (4-bit)
b Linear search (4-bit)
c Asymmetric binary search (4-bit)

In an asymmetric binary search, after sign determination of the input signal, instead of comparing the input with $\pm 1/2V_{ref}$, input is first compared with $\pm 1/4V_{ref}$ and the search progresses as shown in Fig. 1*c*. Asymmetric switching scheme and switching energies for a 3-bit SAR are shown in Fig. 2. As the search operation progresses from 0 to V_{ref}, only one capacitor is switched at a time. With this scheme, 3/4th of the input range is digitised by consuming less energy, and for the remaining 1/4th input range, energy consumption is nearly the same as that of the previously proposed scheme [2]. To reduce the complexity of switching logic, only 3 MSBs are resolved with the help of an asymmetric search. V_{cm}-based switching [2] is used to resolve the rest of the bits. Though, in this Letter, we have only discussed a particular type of asymmetric search, the switching energy and comparison cycles trade-off can be explored in a variety of ways to get various asymmetric binary search algorithms having varying digital complexities and energy saving numbers.

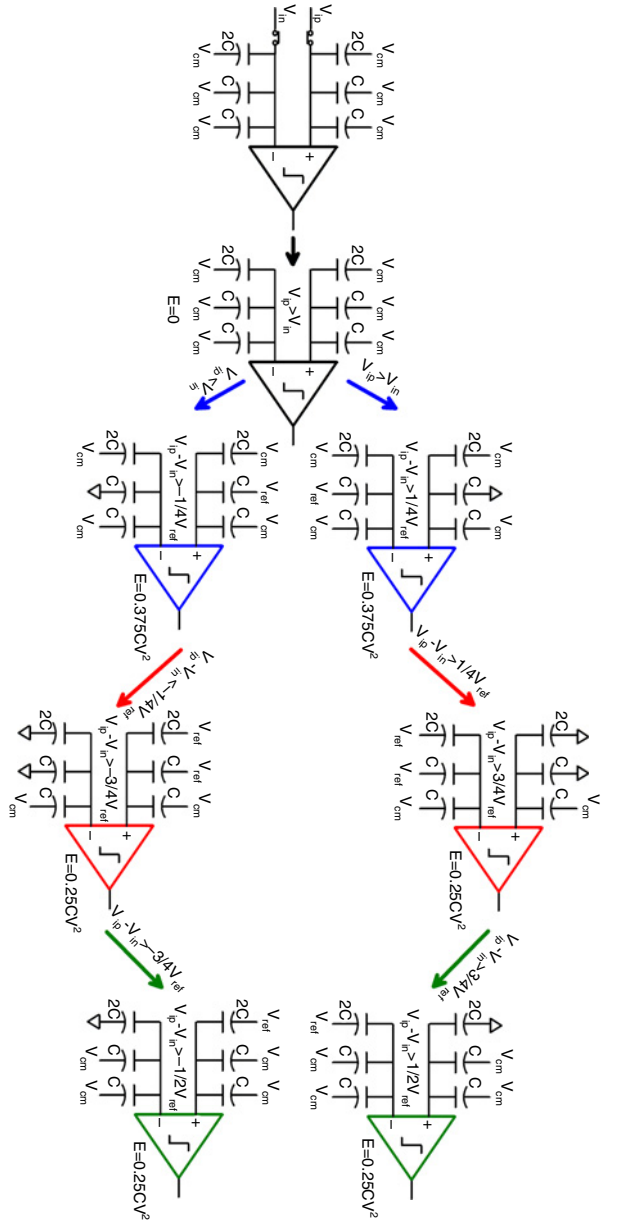

Fig. 2 *Asymmetric binary search switching scheme and energy consumption for 3-bit SAR ADC*

Average energy consumption: Energy consumption of the proposed scheme, with signal swing of 2 $V_{ref\ P\text{-}P}$, is compared with a recently published scheme in Fig. 3. For an 8-bit SAR ADC, the proposed switching scheme consumes 16.5% less energy as compared to the V_{cm}-based switching in [2]. However, for a small input signal swing (0.5 $V_{ref\ P\text{-}P}$), the proposed scheme consumes 46% less switching energy. Average switching energies of the V_{cm}-based switching, linear switching and the proposed scheme are given below.

Asymmetric binary search switching ($n \geq 4$):

$$Eavg \simeq \left[\sum_{i=1}^{n-1} 2^{n-2-2i} + \frac{7}{16}\left(1 + \sum_{i=1}^{n-4} 2^i\right)\right] CV_{ref}^2 J \quad (1)$$

Linear search switching:

$$Eavg = \frac{1}{2^{2n-1}}\left[\sum_{i=1}^{2^{n-1}-1} 2^{n-1} - i + \sum_{j=1}^{2^{n-1}-1}\sum_{j=1}^{j} 2^{n-1} - i\right] CV_{ref}^2 J \quad (2)$$

V_{cm}-based switching:

$$Eavg = \sum_{i=1}^{n-1} 2^{n-2-2i}(2^i - 1) CV_{ref}^2 J \quad (3)$$

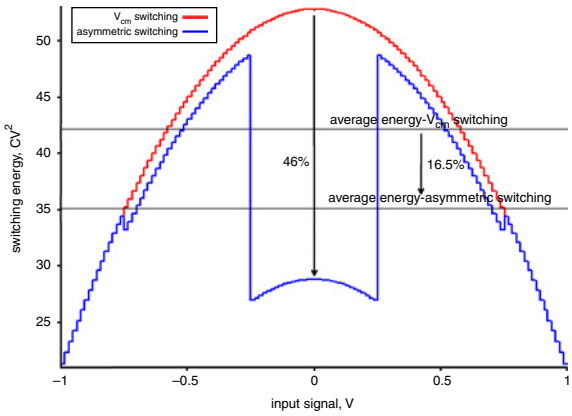

Fig. 3 *Energy saving comparison with existing scheme*

Clock cycles: Owing to the asymmetric nature of switching, for an n-bit SAR, 50% of the digital codes require $n + 1$ comparison cycles, 25% require n comparison, and the remaining 25% require $n - 1$ comparisons. Assuming uniform input signal, average comparison required is given as

$$N_{avg\_cycle} = n + 0.25 \quad (4)$$

Owing to variable comparison cycles, asynchronous SAR logic [5] is most suitable for the proposed scheme. Extra comparison cycles to resolve the input equate to extra energy consumption in the comparator and digital logic. However, it can be observed from (4) that for $n > 8$, the overhead energy consumption is a very small fraction of the total energy consumption in comparator and digital logic, and it will go even further down as the technology continues to scale.

Conclusion: An asymmetric binary search switching scheme has been proposed and compared with existing schemes. The proposed scheme, without using any additional switches, consumes less energy than recently published schemes. The saving is more pronounced with the small input signal swing. Switching energy saving and comparison cycle trade-off have been discussed also.

24 September 2010
doi: 10.1049/el.2010.2691
One or more of the Figures in this Letter are available in colour online.

T. Anand, V. Chaturvedi and B. Amrutur (*Microelectronics Lab, Department of Electrical and Communication Engineering, Indian Institute of Science, Bangalore, India*)

E-mail: tejasvianand@gmail.com

References

1 Verma, N., and Chandrakasan, A.P.: 'An ultra low energy 12- bit rate-resolution scalable SAR ADC for wireless sensor nodes', *IEEE J. Solid-State Circuits*, 2007, **42**, (6), pp. 1196–1205
2 Zhu, Yan., *et al.*: 'A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS', *IEEE J. Solid-State Circuits*, 2010, **45**, (6), pp. 1111–1121
3 Liu, C.C., *et al.*: 'A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure', *IEEE J. Solid-State Circuits*, 2010, **45**, (4), pp. 731–740
4 Ginsburg, B.P., and Chandrakasan, A.P.: 'An energy-efficient charge recycling approach for a SAR converter with capacitive DAC'. Proc. IEEE Int. Symp. Circuits and Systems, Kobe, Japan, 2005, Vol. 1, pp. 184–187
5 Chen, S.W.M., and Brodersen, R.W.: 'A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-um CMOS', *IEEE J. Solid-State Circuits*, 2006, **41**, (12), pp. 2669–2680