When the START signal is asserted, the clock multiplier exits the off state and approximately 17µW during the off-state. Bias voltages are maintained at the expense of a small power penalty of approximately 100mW. This rapid phase locking results in a small power-on time, 2psrms long-term absolute jitter, less than 10ns (3 reference cycles) power-on time, 25µW off-state power, 12pJ energy overhead for on/off transition, and 2.2mW on-state power at 2.5GHz output frequency.

The proposed clock multiplier is implemented in a 90nm logic CMOS process and occupies an active area of 0.16mm². At 2.5GHz output frequency with a divide ratio of 8, the clock multiplier consumes 2.2mW from a 1.1V supply. Fig. 14.5.3 illustrates the measured settling behavior by plotting period jitter as a function of time for N=8 and N=16 cases. The phase/frequency lock time is less than 10ns or approximately 3 reference cycles. The peak period jitter is calculated by post processing the output clock waveform captured using a Tektronix TDS7404 scope. The output clock waveforms during power cycling are also measured for different decoupling capacitor values and are shown in Fig. 14.5.3. The measured settling behavior for different decoupling capacitor values is shown in Fig. 14.5.4. As expected, a larger CD reduces jitter and increases settling time, and vice versa. The measured long-term absolute jitter is less than 100fs for 20pF and 0pF capacitors and 1.1pF/50pF/10pF capacitors, respectively. The measured settling time is 25ns and 10ns with a 20pF and 0pF capacitors, respectively.

Figure 14.5.5 shows the measured power consumption vs. duty cycle when power cycled at three different on/off time periods. The power scales linearly with on/off duty cycle and the average energy overhead for power cycling is measured as 12pJ. Measured total off-state power is 25µW of which 17µW is consumed by bias circuitry, and 8µW is due to leakage in the digital logic. The measured long-term absolute jitter for the measured settling behavior is less than 100fs for 20pF and 0pF capacitors and 1.1pF/50pF/10pF capacitors, respectively. The measured settling time is 25ns and 10ns with a 20pF and 0pF capacitors, respectively.
Figure 14.5.1: Block diagram and locking transient of the proposed fast power-on clock multiplier.

Figure 14.5.2: Schematic of the digitally controlled oscillator (DCO) with a programmable decoupling capacitor (CD) bank.

Figure 14.5.3: Measured period jitter and captured settling behavior for divide by 8 and 16 cases.

Figure 14.5.4: Measured peak period jitter as a function of time for different decoupling capacitor (CD) settings on the VCTRL node, and long-term jitter histograms for 0pF and 20pF capacitor cases with N=8.

Figure 14.5.5: Measured power consumption as a function of on-duration when power cycled at different time periods; measured power cycling energy overhead as a function of on-duration; and, power breakup for on-state and off-state conditions.

Figure 14.5.6: Performance summary and comparison with state-of-the art designs.
Figure 14.5.7: Chip micrograph of fast power-on clock multiplier.