14.5 A 2.5GHz 2.2mW/25µW On/Off-State Power 2ps$_{rms}$-Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time

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Modern mobile platforms utilize power cycling to lower power dissipation and increase battery life. By turning off the circuits that are not in use, power cycling provides a viable means to make power dissipation proportional to workload, hence achieving energy proportional operation. The effectiveness of this approach is governed by the turn on/off times, off-state power dissipation, and energy overhead due to power-cycling. Ideally, the circuits must turn on/off in zero time, consume no off-state power, and incur minimal energy overhead during on-to-off and off-to-on transitions. Conventional clock multipliers implemented using phase-locked loops (PLLs) present the biggest bottleneck in achieving these performance goals due to their long locking times. Even if the PLL is frequency locked, the slow phase acquisition process limits the power-on time [1-2]. Techniques such as dynamic phase-error compensation [3], edge-missing compensation [4], and hybrid PLLs [5] improve the phase acquisition time to at best few hundred reference cycles. However, such improvements are inadequate to make best use of power-cycling. Multiplying injection-locked oscillators (MILO) are shown to lock faster than PLLs, but suffer from conflicting requirements on injection strength to simultaneously achieve low jitter and fast locking. Increasing the injection strength extends lock range and reduces locking time, but severely degrades the deterministic jitter performance [6]. In view of these drawbacks, we propose a highly digital clock multiplier that seeks to achieve low jitter, fast locking, and near-zero off-state power. By using a highly scalable digital architecture with accurate frequency presetting and instantaneous phase acquisition, the prototype 8×/16× clock multiplier achieves 10ns (3 reference cycles) power-on time, 2ps$_{rms}$ long-term absolute jitter, less than 25µW off-state power, 12pJ energy overhead for on/off transition, and 2.2mW on-state power at 2.5GHz output frequency.

Figure 14.5.1 shows the block diagram of the proposed digital clock multiplier. It employs a split-tuned architecture wherein a coarse frequency-tuning loop consisting of a frequency detector, a digital accumulator, and a fast-settling 8b DAC combined with the static current source I_1, drives the ring oscillator close to a frequency lock. A fine phase-tuning loop uses a bang-bang phase detector and first-order digital loop filter to bring the oscillator's frequency to the desired output frequency. Stability of the phase-tuning loop is ensured by periodically resetting the oscillator's phase with the input reference clock phase using the edge replacement logic (ERL) [7]. Ideally, this also ensures phase-locking in one reference cycle if the oscillator frequency is accurately tuned.

When the START signal is de-asserted, the clock multiplier enters the off-state. The SEL signal goes high which breaks the oscillator's feedback and turns-off OUT_{CLK}. Consequently, the static current source I_1 charges the V_{CTRL} node to V_{DD}. The DACs are powered off, and the accumulators' states are held by gating both the digital input and the clock. The DAC's bias circuitry is not turned off to reduce the power-on time penalty caused by slow-settling transients. Instead, bias voltages are maintained at the expense of a small power penalty of approximately 17µW during the off-state.

When the START signal is asserted, the clock multiplier exits the off state and enters the on state, as shown in the timing diagram of Fig. 14.5.1. The DACs power-on and rapidly drive the V_{CTRL} node from V_{DD} towards its steady-state value, thus locking the oscillator's frequency almost instantaneously. The ERL receives the retimed divided-by-N rising edge signal (COUNT), and asserts SEL. Logic high of the SEL signal breaks up the digitally controlled oscillator's (DCO) feedback momentarily and allows a clean reference edge to replace the Nth DCO edge, thus aligning the DCO's phase to the REF phase. The rising edge of the REF signal de-asserts the SEL signal and closes the ring for the next N DCO cycles. Hence, a clean reference edge insertion at every reference cycle instantaneously locks the DCO's phase and resets the DCO's jitter accumulation due to phase noise and supply noise. This rapid phase locking results in a small power-on time and regular phase realignment results in superior jitter performance.

Figure 14.5.2 shows the schematic diagram of the DCO. It consists of a mux and pseudo differential delay cells coupled in a feed-forward fashion to guarantee differential oscillation. To ensure clean reference edge insertion, the rise/fall times of the REF signal are matched to the OUT_{CLK} by buffering REF with a matched delay cell. The voltage-to-frequency (V-to-F) bandwidth of the oscillator depends on the decoupling capacitor, C_D, on node V_{CTRL}. While a large C_D suppresses the ripples on the virtual supply of the oscillator and reduces jitter generation, it also reduces the V-to-F bandwidth, which increases the frequency settling time. On the other hand, a small C_D improves frequency settling time but degrades jitter performance. To quantify this tradeoff, C_D is implemented using a bank of digitally controlled capacitors.

The DACs are implemented using thermometer-coded current-mode architecture to ensure monotonicity and fast settling. Single-ended source-switched current elements are used to minimize area penalty. As opposed to a commonly used ΔΣ DAC, the employed current-mode Nyquist DAC does not require a post filter, and its high bandwidth sets the DCO's frequency rapidly during the on/off events. The high impedance of the DAC current sources also shields the DCO from the power supply transients.

The proposed clock multiplier is implemented in a 90nm logic CMOS process and occupies an active area of 0.16mm^2. At 2.5GHz output frequency with a divide ratio of 8, the clock multiplier consumes 2.2mW from a 1.1V supply. Fig. 14.5.3 illustrates the measured settling behavior by plotting period jitter as a function of time for N=8 and N=16 cases. The phase/frequency lock time is less than 10ns or approximately 3 reference cycles. The peak period jitter is calculated by post processing the output clock waveform captured using a Tektronix TDS7404 scope. The output clock waveforms during power cycling are also shown in Fig. 14.5.3. The measured settling behavior for different decoupling capacitor values is shown in Fig. 14.5.4. As expected, a larger C_D reduces jitter and increases settling time, and vice versa. The measured long-term absolute jitter over 100k hits for 20pF and 0pF capacitors is 1.1ps$_{rms}$/10ps$_{pk-pk}$ and 2ps$_{rms}$/18.6ps$_{pk-pk}$, respectively. The measured settling time is 256ns and 10ns with a 20pF and 0pF capacitors, respectively.

Figure 14.5.5 shows the measured power consumption vs. duty cycle when power cycled at three different on/off time periods. The power scales linearly with on/off duty cycle and the average energy overhead for power cycling is measured as 12pJ. Measured total off-state power is 25µW of which 17µW is consumed by bias circuitry, and 8µW is due to leakage in the digital logic. The performance summary is compared to the state-of-the-art in Fig. 14.5.6. This work achieves the lowest reported power-on time, has the best active power efficiency, and exhibits a linear relationship of power vs. usage with minimal energy overhead during transitions. The die micrograph is shown in Fig. 14.5.7.

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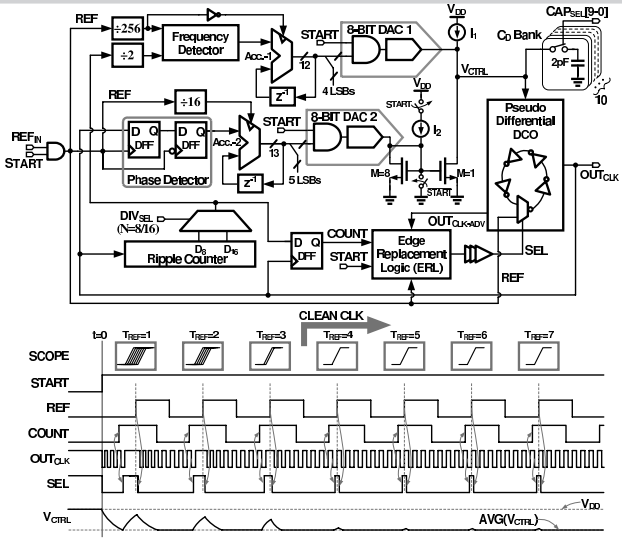


Figure 14.5.1: Block diagram and locking transient of the proposed fast power-on clock multiplier.

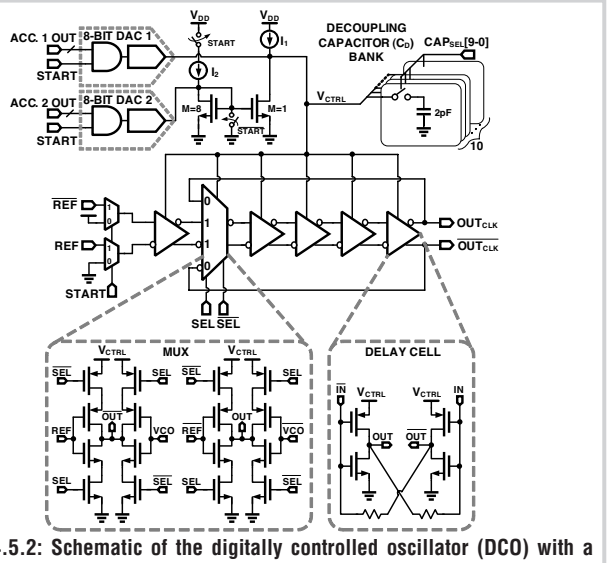
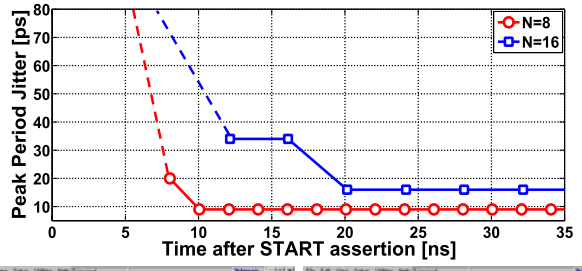


Figure 14.5.2: Schematic of the digitally controlled oscillator (DCO) with a programmable decoupling capacitor (C_D) bank.



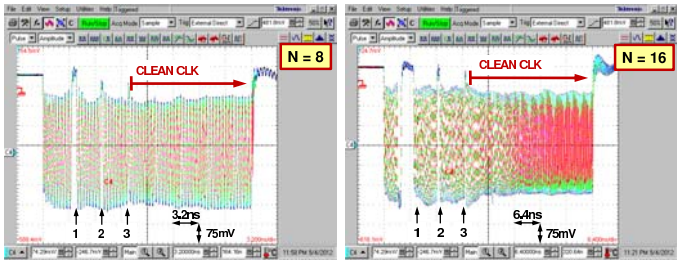
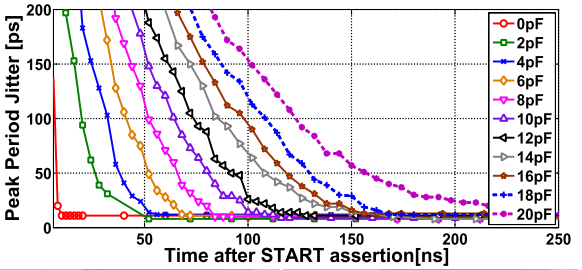


Figure 14.5.3: Measured period jitter and captured settling behavior for divide by 8 and 16 cases.



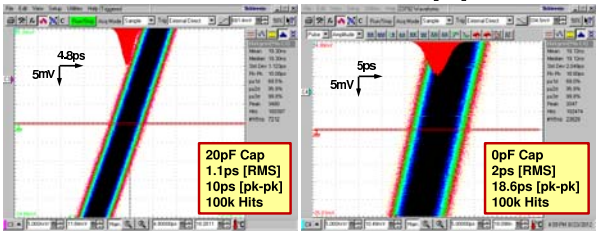


Figure 14.5.4: Measured peak period jitter as a function of time for different decoupling capacitor (C_D) settings on the V_{CTRL} node, and long-term jitter histograms for 0pF and 20pF capacitor cases with N=8.

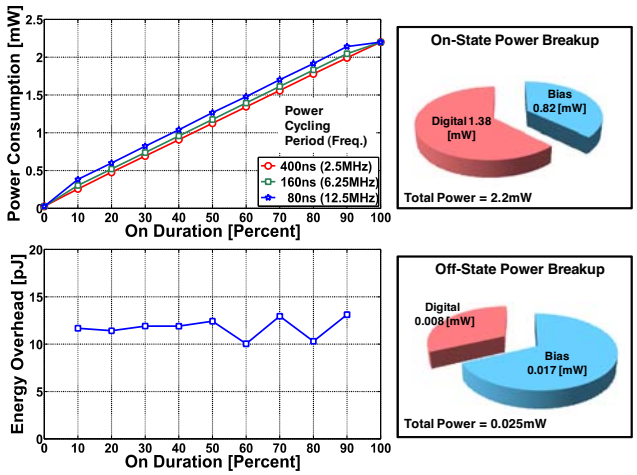


Figure 14.5.5: Measured power consumption as a function of on-duration when power cycled at different time periods; measured power cycling energy overhead as a function of on-duration; and, power breakup for on-state and off-state conditions.

	This Work	VLSI'11 J. Zerbe	ISSCC'12 [1]	JSSC'10 [2]	JSSC'10 [3]	ISSCC'09 [4]	JSSC'08 [5]
Technology	90nm	40nm	22nm	40nm	180nm	180nm	180nm
Supply [V]	1.1	NA	1	1.1	1.8	1.6	1.8
Output Freq. [GHz]	2.5	2.8	3.2	4.3	5.6	2.64	2.409
Reference [MHz]	312.5	700	100	537.5	10	80	64
Jitter-Long Term (rms/pk-pk) [ps]	2/18.6 (0pF) 1.1/10 (20pF)	NA	6/NA	NA	NA	NA	NA
Power [mW/GHz]	0.88	4.8	1.06	NA	3.53	6.9	12.28
Power-on Time [s]	10ns	8ns	1.83µs@3GHz	241.8ns	20µs	6µs	20µs
Power-on Time [Reference Cycles]	3	5.6	183	130	200	480	1280
Power Cycling Functionality	YES	YES	YES	YES	NO	NO	NO
Power [mW]	2.2	13.44	3.4	NA	19.8	25.6@3.7GHz	29.6
Architecture	MDLL	MILO	PLL	PLL	PLL	PLL	PLL

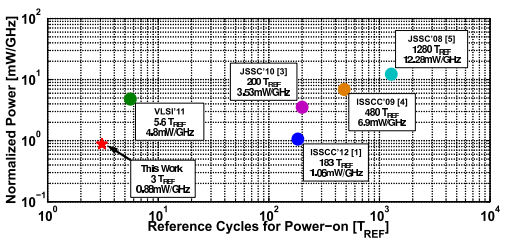


Figure 14.5.6: Performance summary and comparison with state-of-the art designs.

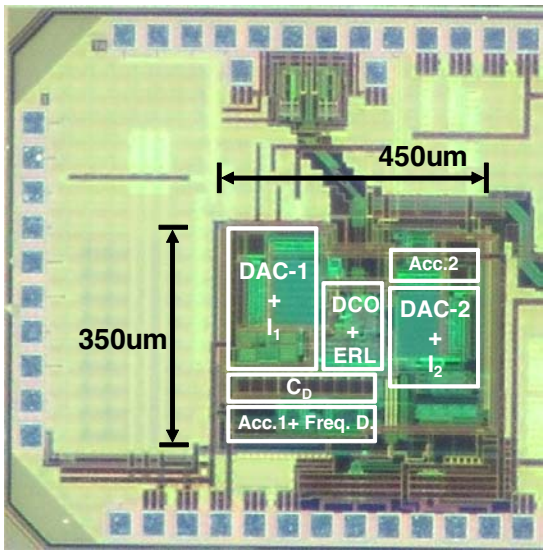


Figure 14.5.7: Chip micrograph of fast power-on clock multiplier.

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