3.7 A 7Gb/s Rapid On/Off Embedded-Clock Serial-Link Transceiver with 20ns Power-On Time, 740µW Off-State Power for Energy-Proportional Links in 65nm CMOS

Tejasvi Anand[1], Mrunmay Talegaonkar[1], Ahmed Elkholy[1], Saurabh Saxena[1], Amr Elshazly[2], Pavan Kumar Hanumolu[1]

[1]University of Illinois, Urbana, IL, [2]Intel, Hillsboro, OR

Energy-proportional operation of serial links is imperative for realizing energy-efficient data centers and low-power mobile interfaces such as MIPI [1]. Burst-mode communication, where the link is powered-off when idle and powered-on when needed, achieves energy proportional operation [2]. Ideally, a burst mode link must be turned on/off in zero time, must consume zero power in the off-state and must incur zero energy overhead while making on/off transitions. However, these requirements are difficult to meet in practice and as a consequence, the efficacy of burst mode communication in achieving energy proportional operation is reduced. The main challenges in achieving small power-on time and off-state power include the design of fast-locking PLLs, CDRs and achieving fast settling of bias node voltages. In this paper, we present a complete 7Gb/s energy-proportional embedded-clock transceiver that achieves less than 20ns power-on time while consuming 63.7mW on-state power, 0.74mW off-state power and 1.2nJ of total transition energy penalty per burst.

Figure 3.7.1 shows the block diagram of the transceiver. The transmitter is composed of parallel PRBS generators, a 16:1 mux, and a fast power-on CML driver with 3-tap FFE. The transmitter together with the PLL is powered-on by an external start signal while the receiver powers-on automatically upon detecting incoming data. Both transmitter and receiver share a low power on-chip temperature sensor and a 7GHz fast power-on LC-PLL. The PLL can be configured to operate in either transmitter or in receiver mode, and has an option to be configured in either proportional or bang-bang control. Also shown in Fig. 3.7.1 is the receiver consisting of a Start Rx generator, quarter-rate BBPD, four 1.75GHz fast power-on phase interpolators (PIs), fast power-on CDR with dynamic-gain-control logic, three 4:16 demuxes and parallel PRBS checkers. The loop gain of the digitally controlled PI based CDR loop is adaptively adjusted to minimize lock time. Instead of taking a majority vote of early and late signals, they are de-muxed and provided to the CDR logic. By adjusting the PI phase based on the number of early and late signals, the clock phase of the data sampler is quickly aligned to the center of incoming data. The recovered data is de-muxed to the parallel PRBS checker that is also designed to operate in burst-mode. Biasing of the PI and of the CML output driver is left powered-on in the off-state. This greatly reduces power-on time at the expense of 40µW increase in the off-state power. Receiver lock time is estimated from *Error* signal, which is generated by performing logical OR operation on parallel PRBS checker outputs. Receiver lock is declared when the *Error* signal goes low.

Figure 3.7.2 shows the block diagram of fast power-on digital LC-PLL. It uses a hybrid architecture wherein the proportional and integral paths are implemented in analog and digital domain, respectively [5]. Storing the digital frequency control word in the integral path accumulator during the off-state and restoring it back at power-on ensures that PLL starts in frequency-locked condition. However, this does not guarantee rapid phase locking because of the perturbation caused by the unknown initial input phase offset ($\Delta\Phi = \Phi_{REF\text{-}DEL} - \Phi_{FB\text{-}DEL}$). Conventional PLLs rely on feedback action to force $\Delta\Phi = 0$, and as a result have long lock time that is inversely proportional to the PLL bandwidth. In this work, we seek to reduce lock time by making $\Delta\Phi = 0$ on power-on without using the PLL feedback. The two main components that cause $\Delta\Phi \neq 0$ are: (a) unknown initial phase of the DCO and (b) delay in the feedback path of PLL. To mitigate the former, LC-DCO is kick-started by a pulse having a known phase relationship with the reference clock. This makes the DCO take the same phase trajectory during every power-on transient, which results in the divided DCO output signal (FB_{DEL}) to appear with a fixed phase offset ($\Delta\Phi = \Phi_X$) from the delayed reference signal (REF_{DEL}). This offset is corrected by a DLL such that $\Delta\Phi = 0$. Because Φ_X can be as large as 1 reference period (≈10ns), the DLL must have a very wide range. To ease the range requirement, a ripple-counter-based divider with programmable set/reset control is used as a coarse delay line to set Φ_X to be within one DCO period. The DLL uses PFD output and tunes the digitally controlled delay line (DCDL) such that $\Phi_X = 0$ in steady state. The fine DCDL has 250ps range and approximately 2ps resolution. This phase alignment is performed once during initial startup and is kept on during regular power-on/off operation. To bring FB_{DEL} closer to REF_{DEL}, the DLL moves the DCDL by just one LSB step on each power on/off transition (see timing in Fig. 3.7.2). Note that DLL does not influence PLL loop dynamics in steady state. A replica of DCDL and divider in REF_{DEL} path helps to maintain phase alignment even in the presence of voltage and temperature variations during long power-off periods. A 64×8 look up table (LUT) and associated logic for tracking LC frequency with temperature is also incorporated at the expense of one reference cycle power-on latency.

Figure 3.7.3 shows the measured PLL and transmitter results. Absolute phase drift of PLL output (captured using Agilent DSO-81204A, 1ns after the power-on transient) in both proportional and bang-bang control modes indicates that implemented phase calibration reduces the PLL lock time to <1ns and the phase drift to ±3ps. The capture span is approximately 2 to 3 time constants of the PLL loop and beyond this span PLL feedback ensures that the phase does not drift beyond ±3ps. With 100mV of DLL supply variation during power-off state, error in the phase drift is less than 2ps. At 7GHz output frequency, the PLL achieves an integrated jitter of $435fs_{rms}$ and reference spur of -50.1dBc while consuming 4.8mW on-state power and 41.6µW off-state power. The measured power-on time of CML output driver is less than 500ps.

Figure 3.7.4 shows the measured results of transceiver with PRBS7 data captured after 4 billion on-off transitions. When the transmitter is powered-on, output common-mode voltage drops from V_{DD} to $V_{DD} - V_{SWING}/2$, where V_{SWING} is the transmitter output swing. Start Rx generator senses this change in common mode and powers on the receiver. CDR achieves lock within 20ns of power-on. The latency of the parallel PRBS checker to generate *Error* signal to go low, which is approximately 3 to 4 CDR clock cycles (≈7ns) is included in the power-on time of 20ns. Lock time is observed to be proportional to the amount of ISI in the data, and the reported power-on time is with an eye opening of 0.25UI at the input of the samplers (see the bathtub plot in Fig. 3.7.4). Measured JTOL corner frequency in always-on case is around 2MHz.

Energy proportional behavior of the complete transceiver in operation is verified and results are shown in Fig. 3.7.5. For 128-byte data bursts, the transceiver achieves 100× effective data-rate scaling (7Gb/s to 70Mb/s) while scaling the power by 44× (63.7 to 1.43mW) and energy efficiency by only 2.2× (9.1 to 20.5pJ/b). For 8-byte data burst, compared to the always-on case, the transceiver achieves 26× energy efficiency improvement at 70Mb/s. The performance of the transceiver and PLL is compared to the state-of-the-art in Fig. 3.7.6. Among the cited designs, the LC PLL achieves lowest reported power-on time without compromising its energy efficiency and jitter performance. This work demonstrates energy-proportional operation in an embedded clock architecture. The die micrograph is shown in Fig. 3.7.7.

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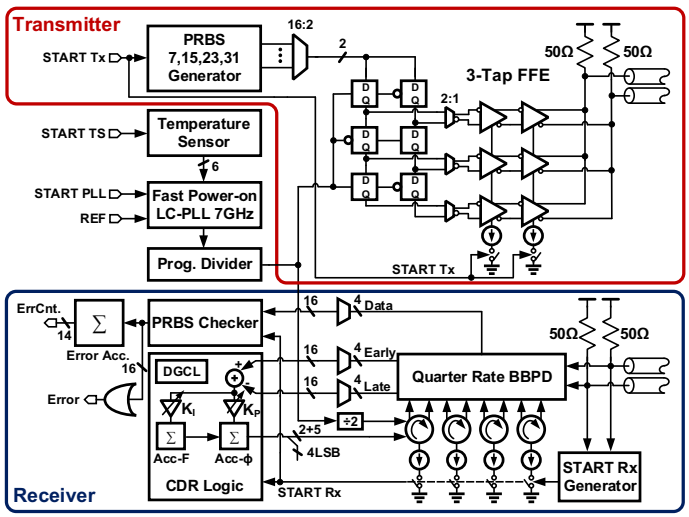

Figure 3.7.1: Block diagram of the 7Gb/s energy proportional transceiver.

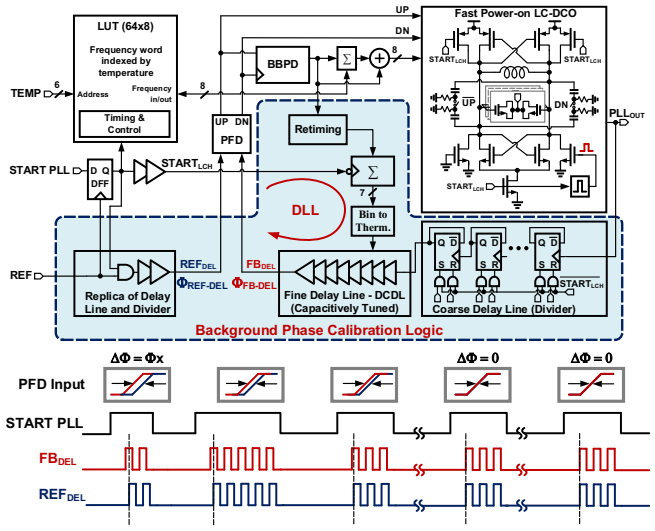

Figure 3.7.2: Block diagram of the fast power-on LC-PLL and timing diagram of background phase calibration logic.

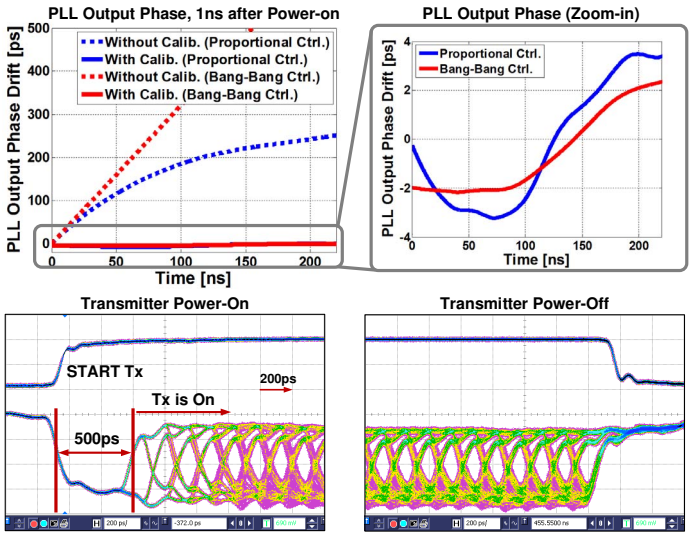

Figure 3.7.3: On/off measurements of the PLL and transmitter.

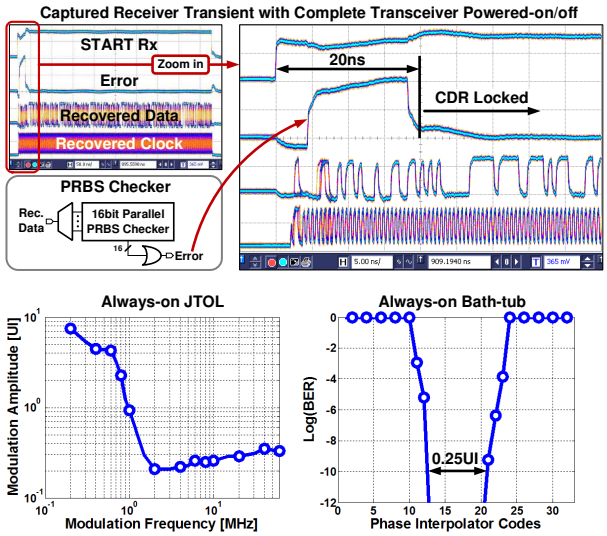

Figure 3.7.4: Measured on/off behavior of the transceiver along with the measured JTOL and bathtub plot at the input of receiver samplers.

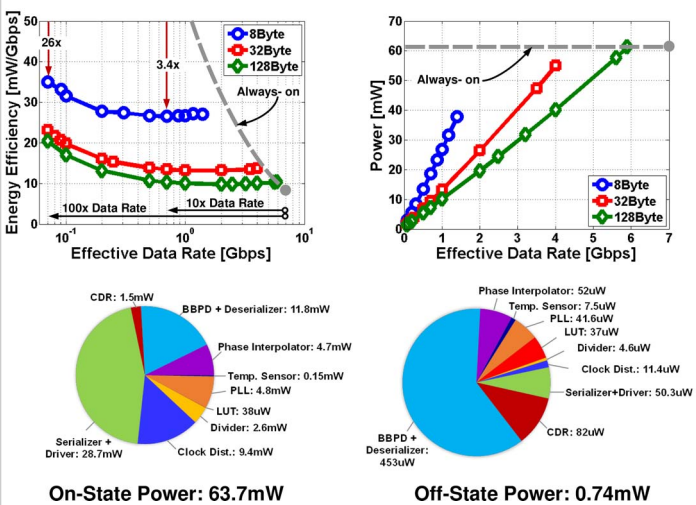

Figure 3.7.5: Measured energy efficiency and power at different data-rates obtained by duty cycling the transceiver for three different data burst lengths.

Transceiver Comparison Table

	This Work	JSSC'10 [2]
Architecture	Embedded Clock	Forwarded Clock
Technology	65nm GP	40nm LP
Supply [V]	1/1.1	1.1
Peak data rate [Gb/s]	7	2.7-4.3
Power-on time [ns]	Less than 20	241.8
Efficiency [pJ/bit]	9.1	3.3
On-state power [mW]	63.7	14.2
Off-state power [µW]	740	50
De/Serialization Ratio	16:1	8:1
Area [mm²]	1.7* (1750µmx975µm)	0.92* (1544µmx594µm)

+ Area includes de-cap, pads & test logic * Reported for 8 memory lanes

PLL Comparison Table

	This Work	VLSI'13 [3]	JSSC'10 [2]	ISSCC'13 [4]	CICC'12 Dunwell
Architecture	PLL	PLL	PLL	MDLL	MILO
Technology	65nm GP	40nm	40nm LP	90nm	65nm
Supply [V]	1	NA	1.1	1.1	1.1
Output Freq. [GHz]	7	25	4.3	2.5	2.3-4
Reference [MHz]	109.375	390	537.5	312.5	790
Integrated Jitter [fs]	435	394	N/A	752	N/A
Power-on Time [ns]	1	100	241.8	10	10
Power Efficiency [mW/GHz]	0.68	2.56	NA	0.88	30.4
On Power [mW]	4.8	64	NA	2.2	96
Off Power [µW]	41.6	N/A	NA	25	N/A

Figure 3.7.6: Performance summary and comparison with state-of-the-art designs.

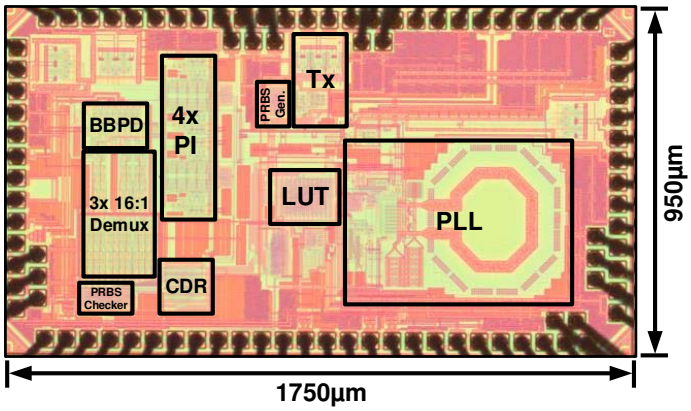

Figure 3.7.7: Die micrograph of the transceiver.

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