A VCO Based Highly Digital Temperature Sensor With 0.034 °C/mV Supply Sensitivity

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***Abstract*— A self-referenced VCO-based temperature sensor with reduced supply sensitivity is presented. The proposed sensor converts temperature information to frequency and then into digital bits. A novel sensing technique is proposed in which temperature information is acquired by evaluating the ratio of the output frequencies of two ring oscillators, designed to have different temperature sensitivities, thus avoiding the need for an external frequency reference. Reduced supply sensitivity is achieved by employing the voltage dependence of junction capacitance, thus avoiding the overhead of a voltage regulator. Fabricated in a 65 nm CMOS process, the prototype can operate with supply voltages ranging from 0.85 V to 1.1 V. It achieves supply sensitivity of 0.034 °C/mV and an inaccuracy of ±0.9 °C and ±2.3 °C from 0 to 100 °C after 2-point calibration, with and without static nonlinearity correction, respectively. The proposed sensor achieves 0.3 °C resolution, and a resolution FoM of 0.3 nJK^2. The prototype occupies a die area of 0.004 mm^2.**

***Index Terms*— CMOS based, DRAM, highly digital, processor, sensor, temperature, temperature sensor, VCO based.**

I. Introduction

MODERN-day processors and DRAMs utilize several on-chip temperature sensors for thermal monitoring [1]. In the case of processors, temperature sensors help to maintain performance and reliability by monitoring both the cold and hot spots [2]. On the other hand, DRAMs control the rate of self-refresh operations based on current die temperature to save power [3]. Since it is difficult to predict hot spot locations during the design phase, microprocessors incorporate as many as ten or more sensors per-core [4]. With the increase in the number of cores per processor each year [5] fueled by the ever-growing computational demand, the number of temperature sensors in the processor will continue to increase. Therefore, an efficient and low-cost temperature sensor suitable for integration in processors and DRAMs is highly needed.

Sensors must incorporate several key features to make them suitable for use in processors. First and foremost, they must be small and compact so that they can be placed very close to hot spots. A sensor designed to operate from the local (logic) supply voltage helps in reducing the overhead associated with the routing of a separate dedicated power supply. However, because of the constant switching of logic gates, the logic supply is very noisy, as shown in Fig. 1. Furthermore, its average voltage can vary substantially due to the use of dynamic voltage scaling (DVS) in modern processors. Therefore, the sensor must be immune to supply voltage variations [6]. SoCs and processors also employ dynamic frequency scaling algorithm (DFS), where the switching frequency is scaled to trade power with performance. The use of both dynamic voltage and frequency scaling algorithms (DVFS) constrains the temperature sensor design in such a way that the sensor can no longer rely on using external frequency or supply voltage as a reference. Routing a dedicated reference frequency, voltage and bias current to temperature sensors all over the processor is an expensive endeavor. Therefore, the temperature sensor must be self-referenced. Finally, the temperature sensor architecture should be such that it is relatively easy to design and port to different process nodes.

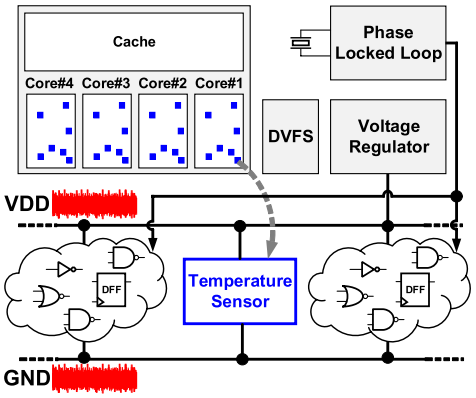

Fig. 1. Example of a temperature sensor integrated inside a processor.

Several all-CMOS-based sensor architectures have been proposed to meet the above-mentioned requirements. Thermal diffusivity-based sensors offer high accuracy and small area [7], but their power dissipation is on the high side. DTMOST-based sensors [8] offer high accuracy, low power, and sub-1 V operation, but occupy a large area. Delay- and frequency-based sensors employing TDCs, DLLs, and ring oscillators scale well with process [9], [10]. However, the area penalty associated with large delay lines [11]–[13], the requirement for an external reference clock [14]–[16], and the need for operational amplifiers [17] and voltage regulators [18] could hinder their integration in processors. Given these drawbacks, we present a highly digital VCO-based self-referenced sensor with digital readout, reduced supply sensitivity, and compact size.

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Fabricated in a 65 nm CMOS process, the proposed sensor [19] with a digital readout circuit occupies an active area of 0.004 mm^2. The sensor achieves a supply sensitivity of 0.034 °C/mV. Operating from a 1 V supply, measurement time can be as fast as 6.5 μs, for a quantization error of 1 °C, resolution of 0.3 °C, and a resolution FoM [20] of 0.3 nJK^2. With two-point calibration at extreme temperatures (compatible with processor testing [2]), the proposed sensor achieves peak-to-peak nonlinearity with and without polynomial correction of ±0.9 °C and ±2.3 °C, respectively over a 0 °C to 100 °C temperature range. With one-point calibration, the sensor achieves peak-to-peak nonlinearity with and without polynomial correction of ±3.3 °C and ±4.3 °C, respectively.

The remainder of this paper is organized as follows. Section II introduces the proposed temperature sensor concept. Design details for making the sensor less sensitive to the supply voltage variations is described in Section III. Architecture and circuit details of the sensor are presented in Section IV. Section V analyzes the effect of VCO phase noise on achievable sensor resolution. Section VI presents the measured results. Section VII concludes the paper.

II. Temperature Sensor Concept

The proposed sensor operates by measuring the oscillation frequency of two different ring oscillators (sensing elements), each having different temperature sensitivity. The ratio of oscillator frequencies, when digitized, represents the temperature. Temperature affects the frequency of a CMOS ring oscillator either through mobility or through the threshold voltage variations. Mathematically, frequency of a ring oscillator, to a first-order approximation, is inversely proportional to the delay of the delay stage ($1/RC_L$) and can be expressed as [21]

$$F_{VCO} \propto \frac{4}{3}\frac{\mu C_{ox} W/L (V_{DD} - V_{TH})^2}{V_{DD}\left(1 - \frac{5}{6}\lambda V_{DD}\right) C_L} \quad (1)$$

where μ is the mobility of electrons/holes, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the MOS transistors, V_{DD} is the supply voltage of oscillator, V_{TH} is the average threshold voltage of transistors used in the delay stage (assuming NMOS and PMOS have the same threshold voltage), λ is the channel length modulation parameter, and C_L is the load capacitance of the delay stage. Mobility and threshold voltage as a function of temperature (Temp) can be written as

$$\mu \propto \mu_0 (\text{Temp}/T_0)^{-p} \quad (2)$$

$$V_{TH} = V_{TH0} - k(\text{Temp} - T_0) \quad (3)$$

where p is a fitting parameter typically in the range of 1.2 to 2.0, μ_0 is the mobility at room temperature T_0, V_{TH0} is the threshold voltage at room temperature, and k is approximately in the range of 1 to 3 mV/°C.

The temperature sensitivity of an oscillator can be modified by either changing the mobility, threshold voltage or the supply voltage. The designer has no direct control over the mobility, and it is often cumbersome to route two separate power supply rails to a sensor placed deep inside a processor. Therefore, in this work, threshold voltage is used to create temperature sensitivity difference. The proposed sensor incorporates two ring oscillators: VCO1 and VCO2, each having different temperature sensitivities, as shown in Fig. 2(a). VCO2 is designed with transistors having smaller threshold voltage as compared with VCO1, that is, the PMOS and NMOS pair in VCO2 has smaller threshold voltage compared with the PMOS and NMOS pair in VCO1. As a result, the effect of mobility variation due to temperature on VCO2 frequency is more dominant than that on VCO1. Consequently, the frequency versus temperature plot of VCO2 has a steeper slope as compared to VCO1 [see Fig. 2(a)].

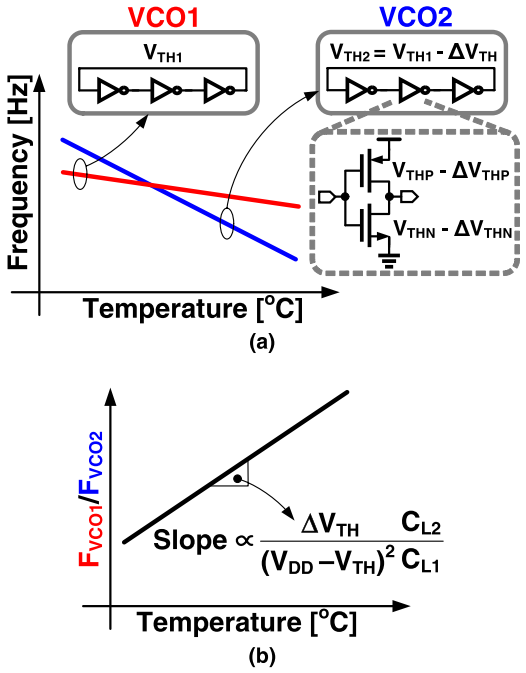

Fig. 2. Operating principle of the proposed sensor. (a) VCO1 and VCO2 frequency versus temperature. (b) Ratio of VCO1 frequency over VCO2 frequency versus temperature.

The ratio of frequencies of VCO1 and VCO2 [F_{VCO1}/F_{VCO2}] exhibits the desired PTAT characteristic [see Fig. 2(b)]. This ratio is digitized to obtain the digital output proportional to the temperature. In the proposed sensor, the frequency ratio is digitized with the help of a digital logic (explained in Section IV). Unlike conventional time-based sensors, the proposed sensor, once calibrated, can operate without the help of an external reference frequency or voltage.

Threshold voltage difference between VCO1 and VCO2 can be introduced in several ways. Primary among them is body biasing the transistors or using two flavors of transistors, i.e., high/low threshold voltages together with the nominal threshold voltage transistors. Body bias may require analog components such as a bandgap reference and voltage regulators to generate and buffer reference voltages. On the other hand, using two flavors of transistors requires an extra mask during the fabrication process. Therefore, in the proposed sensor, reverse short channel effect (RSCE) is leveraged to create a threshold voltage difference. The

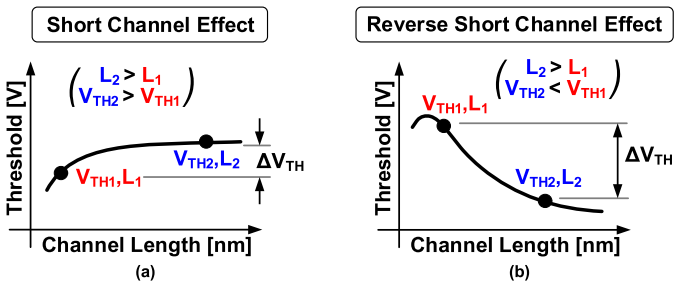

Fig. 3. (a) Effect of channel length on threshold voltage due to short channel effects. (b) Effect of channel length on threshold voltage due to reverse short channel effects.

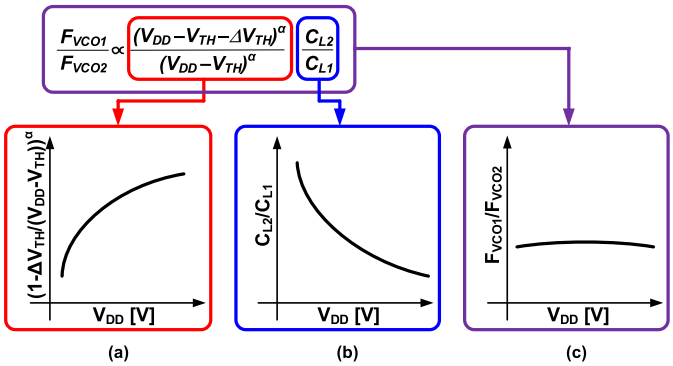

Fig. 4. Concept of designing supply insensitive sensor. (a) The first term has a positive supply sensitivity. (b) The second term has a negative supply sensitive. (c) Supply insensitivity is achieved in frequency ratio.

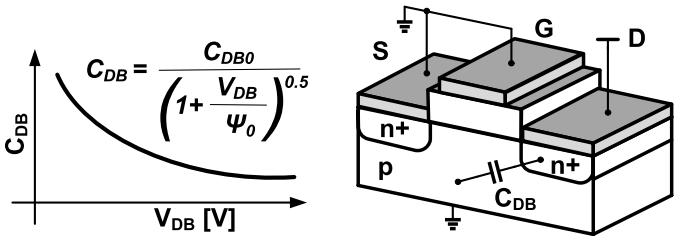

Fig. 5. Drain to bulk junction capacitance (C_{DB}) versus reverse bias voltage.

difference between short channel effect and reverse short channel effect is illustrated in Fig. 3. In the case of short channel effect, threshold voltage reduces as the channel length decreases [see Fig. 3(a)]. On the other hand, reverse short channel effect [22] increases the threshold voltage as the channel length decreases [see Fig. 3(b)]. Reverse short channel effect happens due to the presence of halo implants in planar devices. In 65 nm CMOS, RSCE is dominant and is therefore used to create a difference in the threshold voltages.

In this work, threshold voltage difference was created by using longer channel length transistors in VCO2 as compared with the transistors used in VCO1. In the case of advance technology nodes where RSCE is weak or absent, two flavors of transistors could be used to design this sensor.

III. Making Sensors Less Sensitive to Supply Voltage Variations

The frequency ratio F_{VCO1}/F_{VCO2} is sensitive to the supply voltage. Mathematically, to a first order, it can be written as

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \frac{(V_{DD}-V_{TH1})^{\alpha}C_{L2}}{(V_{DD}-V_{TH2})^{\alpha}C_{L1}} \tag{4}$$

where V_{TH1} and V_{TH2} are the threshold voltages of transistors in VCO1 and VCO2, C_{L1} and C_{L2} are the load capacitance of the delay stages in VCO1 and VCO2, and α is from the α-power law model [23] ($\alpha \approx 1$ for submicron CMOS process). Since the threshold voltage of transistors in VCO1 is larger than that of in VCO2 by ΔV_{TH}, (4) can simplified as

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1-\frac{\Delta V_{TH}}{V_{DD}-V_{TH}}\right)^{\alpha}\frac{C_{L2}}{C_{L1}} \tag{5}$$

where V_{TH} is the threshold voltage of transistors in VCO2. This expression consists of two terms. The first term, which is inside the bracket has a positive sensitivity to the supply voltage, i.e., F_{VCO1}/F_{VCO2} increases as the supply voltage increases, as shown in Fig. 4(a).

The second term is the ratio C_{L2}/C_{L1} where C_{L2} and C_{L1} are the load capacitances seen at the output node of the delay cells used in VCO2 and VCO1, respectively. In the proposed sensor, the load capacitance ratio is designed such that it has negative sensitivity to the supply voltage, as shown in Fig. 4(b). The combined effect of both of these terms is such that the ratio F_{VCO1}/F_{VCO2} is made less sensitive to supply voltage variations [see Fig. 4(c)].

The load capacitance of a typical delay cell consists of a gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}), wire capacitance (C_W), and drain-to-bulk capacitance (C_{DB}). Of these capacitors, C_{DB} is due to the reverse biased pn junction, and it reduces when the reverse bias voltage across the pn junction increases [24], as illustrated in Fig. 5. In the proposed sensor, delay cells of VCO2 are designed such that the C_{DB} dominates the total load capacitance. The size of C_{DB} in VCO2 was chosen such that supply sensitivity of the ratio of C_{L2}/C_{L1} cancels out the supply sensitivity of the first term. Consequently, the ratio F_{VCO1}/F_{VCO2} becomes less sensitive to supply voltage variations.

The effect of process variation on supply sensitivity is observed with the help of process corner simulation, as shown in Fig. 6(a). For a DC supply voltage variation of 0.85 V to 1.05 V at room temperature, the worst-case error in the temperature sensor occurs in the slow-slow (SS) corner. Simulated worst-case supply sensitivity is 0.046°C/mV for the SS corner. The effect of capacitor mismatch on the supply sensitivity is simulated by performing Monte Carlo simulations at two different DC supply voltages. One thousand mismatched simulations were done for a typical corner at 0 °C and 100 °C, with supply varying from 0.95 V to 1.05 V, and the results are shown in Fig. 6(b) and (c), respectively. At 0 °C, and 100 °C, the standard deviation of the error is 0.005 °C/mV.

The effect of AC supply voltage variations on the proposed sensor for three different temperatures, and 200 $mV_{pk\text{-}pk}$ of sinusoidal variation is shown in Fig. 7. For 100 °C at 1.3 MHz, the simulated supply sensitivity is 0.004°C/mV. The integrating nature of the proposed sensor averages out those voltage variations whose frequencies are higher than the conversion

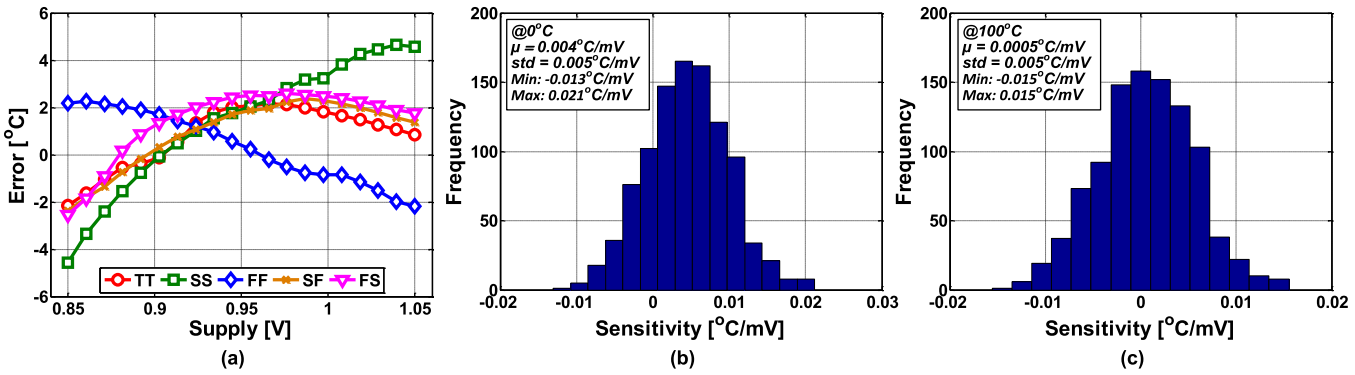

Fig. 6. (a) Simulated DC supply sensitivity across process corners at room temperature. (b) Simulated supply sensitivity with 1000 mismatched simulations at TT corner, 0 °C with 50 mV DC supply voltage variation. (c) Simulated supply sensitivity with 1000 mismatched simulations at TT corner, 100 °C with 50 mV DC supply voltage variation.

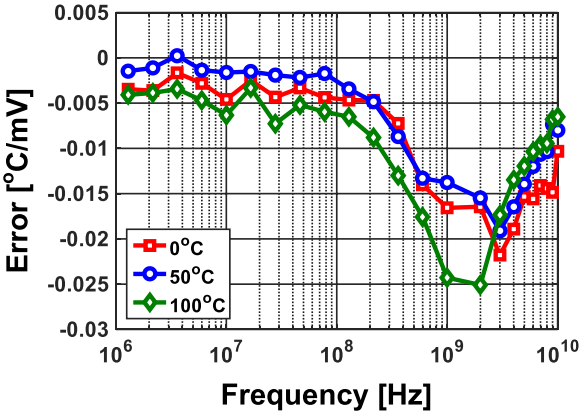

Fig. 7. Simulated supply sensitivity for 200 $mV_{pk\text{-}pk}$ AC supply voltage variations at three different temperatures.

rate of the sensor. This results in lower supply sensitivity as compared to the DC voltage variations. However, at frequencies in the neighborhood of 1 GHz, the supply sensitivity increases because the capacitance ratio C_{L2}/C_{L1} is a weak function of frequency. Supply sensitivity of the sensor at high frequencies can be reduced by adding a low pass filter on the power supply. For example, adding a 100 Ω resistor and a 16 pF decoupling capacitor on the sensor power supply can provide approximately 20 dB suppression of supply noise at 1 GHz. Due to low power consumption of the proposed sensor, DC voltage drop across the 100Ω resistor will be only 15.4 mV.

IV. Temperature Sensor Architecture

The goal of the proposed sensing technique is to design the sensor architecture with all digital logic gates so as to make the design compact, amenable to technology scaling, and portable. A simplified sensor architecture is shown in Fig. 8(a). The proposed sensor consists of two VCOs followed by an accumulator and a latch. Accumulator-1 and Accumulator-2 accumulates the VCO1 and VCO2 frequency to produce output phase Φ_{VCO1} and Φ_{VCO2}, respectively. Graphical representation of accumulation of phase in VCO1 and VCO2 versus time is shown in Fig. 8(b). When Accumulator-2 output (Φ_{VCO2}) reaches threshold N (Φ_{TH}), output of Accumulator-1 (Φ_{VCO1}) is latched (M). Mathematically the phase of Accumulator-1 at the sampling instant equals:

$$\Phi_{OUT} = 2\pi F_{VCO1} T \tag{6}$$

where F_{VCO1} is the oscillation frequency of VCO1, and T is the measurement interval. The relationship between the measurement time T and the programmable threshold Φ_{TH} (N) can be established with the following expression:

$$\Phi_{TH} = 2\pi F_{VCO2} T \tag{7}$$

where F_{VCO2} is the VCO2 oscillation frequency. Dividing (6) by (7), we obtain

$$\Phi_{OUT} = \Phi_{TH} \frac{F_{VCO1}}{F_{VCO2}}. \tag{8}$$

It can be observed from (8) that Φ_{OUT} is proportional to the ratio of VCO frequencies. Thus, the F_{VCO1}/F_{VCO2} ratio can be obtained with the help of a simple accumulate and latch operation.

A. Detailed Architecture

Detailed sensor architecture is shown in Fig. 9. VCO1 consists of 33 inverter stages while VCO2 consists of 17 inverter stages. A larger number of delay stages increases the delay through the loop and lowers the oscillation frequency. Low oscillation frequency helps to reduce the power dissipation in the synthesized digital processing blocks such as counters and state machine. However, this power reduction comes at the cost of increased conversion time.

Bit widths of Accumulator-1 and Accumulator-2 directly affect the accuracy with which F_{VCO1} and F_{VCO2} are measured. Frequency measurement inaccuracy translates to the quantization step size. Wide accumulators help to accumulate the VCO phase for a longer period of time and reduce quantization error at the cost of increased measurement time and energy/measurement. In this work, accumulator size was chosen based on simulations to achieve a minimum quantization error of approximately 0.1 °C. Accumulator-1

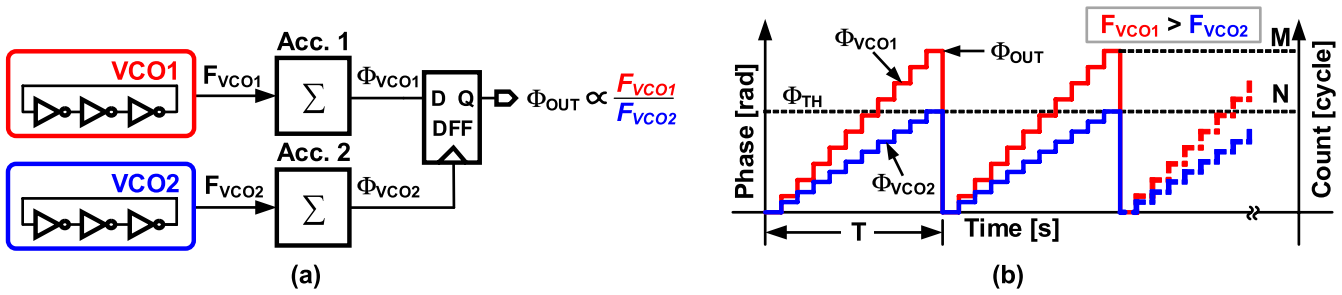

Fig. 8. (a) Simplified architecture of the proposed temperature sensor. (b) Phase versus time plot of the proposed architecture.

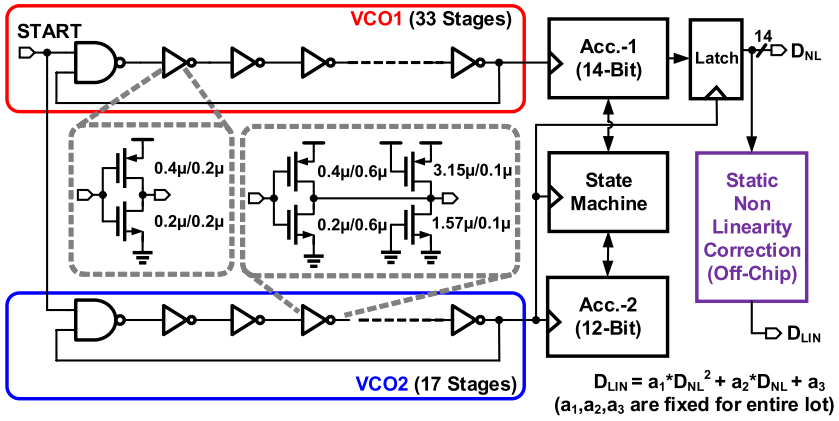

Fig. 9. Proposed temperature sensor architecture.

is 14 bits wide while Accumulator-2 is 12 bits wide. The quantization step size of the sensor is made programmable by adjusting Φ_{TH} (N). Since VCO1 and VCO2 are not synchronized, metastability could occur while sampling Φ_{OUT}. State machine, which operates on the VCO2 clock is designed to freeze the contents of Accumulator-1 before sampling, thus avoiding any metastable behavior.

The threshold voltage difference between the transistors used in the delay cells of VCO1 and VCO2 is created using the reverse short channel effect. Transistors in VCO2 are designed with 3× channel lengths ($L_2 = 600$ nm) as compared with the transistors in VCO1 ($L_1 = 200$ nm). In 65 nm technology, 3× channel length difference helps to create a threshold voltage difference of approximately 33 mV in NMOS and 30 mV in PMOS at room temperature.

Supply sensitivity of the sensor is reduced by increasing the junction capacitance C_{DB} of delay stages in VCO2. It is accomplished by adding additional NMOS and PMOS transistors with their gates connected to ground and supply voltages, respectively. In this design, the size of these transistors was chosen based on simulations.

B. Systematic Nonlinearity Removal

Output of the sensor has a systematic nonlinearity with respect to temperature. This nonlinearity comes from the fact that the frequency ratio F_{VCO1}/F_{VCO2} has nonlinear dependence on temperature. Assuming $\alpha \approx 1$ (for submicron CMOS process), (5) can be rewritten as

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1 - \frac{\Delta V_{TH}}{V_{DD} - (V_{TH0} - k(Temp - T_0))}\right)\frac{C_{L2}}{C_{L1}}. \quad (9)$$

The denominator is expanded with the help of Taylor series to obtain

$$\frac{F_{VCO1}}{F_{VCO2}} \propto \left(1 - \frac{\Delta V_{TH}}{V_{DD} - V_{TH0} - kT_0} \times \sum_{n=0}^{\infty}\left(\frac{-kTemp}{V_{DD} - V_{TH0} - kT_0}\right)^n\right)\frac{C_{L2}}{C_{L1}}. \quad (10)$$

It can be observed from (10) that F_{VCO1}/F_{VCO2} is a nonlinear function of temperature.

A second-order polynomial correction helps to remove this nonlinearity, as shown in Fig. 10. The polynomial correction block is a second-order multiply-and-accumulate unit. The input to the multiply-and-accumulate unit is a nonlinear digital temperature sensor code, and output is a linear digital code. Simulation results suggest that a second-order polynomial with fixed coefficients can correct systematic nonlinearity across

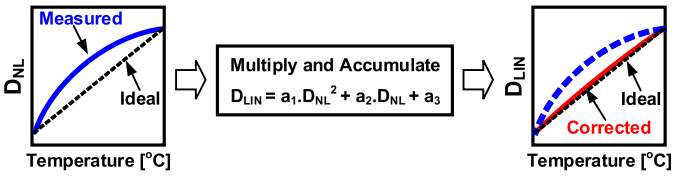

Fig. 10. Systematic nonlinearity correction concept.

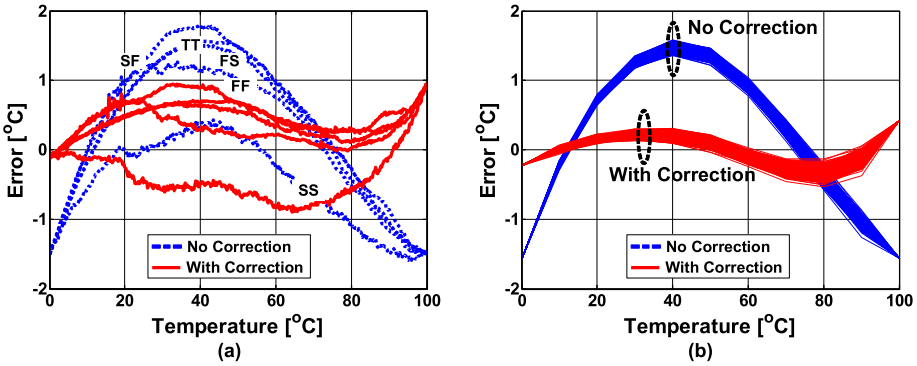

Fig. 11. (a) Simulated nonlinearity across process corners at room temperature. (b) Simulated nonlinearity with 1000 mismatched simulations at TT corner.

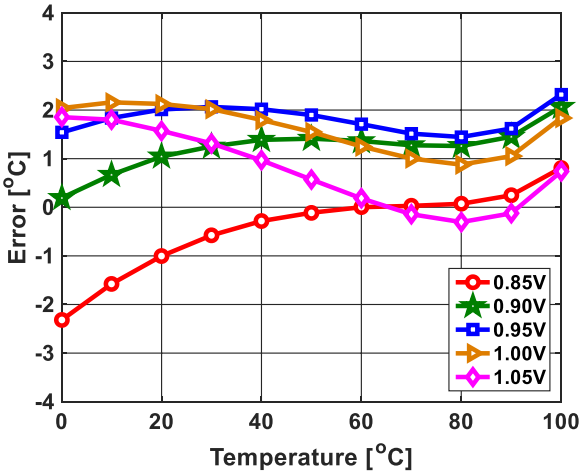

Fig. 12. Simulated peak-to-peak inaccuracy after nonlinearity correction across temperature and DC supply voltage variations for TT corner.

corners, as shown in Fig. 11(a). After polynomial correction, the peak-peak error is ±0.9 °C. The effect of the mismatch on nonlinearity is estimated with 1000 mismatched simulations at the typical corner, and the results are shown in Fig. 11(b). Simulated nonlinearity before and after polynomial correction is approximately ±1.6 °C and ±0.46 °C, respectively. The effect of supply variation on the nonlinearity correction is simulated for a typical process corner, 200 mV of DC supply variation, 0 °C-to-100 °C temperature variation, and the results are shown in Fig. 12. Simulated peak-to-peak inaccuracy is ±2.3 °C.

In the present work, the polynomial correction is implemented off-chip. However, this logic can be easily synthesized on-chip, and can be shared among the several sensors present on a processor. Area overhead of such a synthesized block operating at 10 MHz is 0.0042 mm^2 in 65 nm CMOS. The polynomial multiplication logic features three 13-bit fractional polynomial coefficients, 9-bit input and output, and can support more than 200 temperature sensors in a time-multiplexed fashion.

V. Effect of Phase Noise on Sensor Resolution

Phase noise in a VCO manifests itself as jitter or uncertainty in the VCO time period, which eventually reduces the temperature sensor resolution. A graphical representation of the effect of VCO phase noise on the VCO time period is shown in Fig. 13(a). In this example, T_0 is the VCO time period, t denotes the random process representing VCO period jitter and t[n] denotes error in the nth VCO period.

In the proposed sensor, phase noise of VCO1 introduces uncertainty in sampled phase Φ_{OUT} [see Fig. 13(b)]. On the other hand, phase noise in VCO2 independently introduces uncertainty in the time taken to reach Φ_{TH} [see Fig. 13(c)]. Consequently, it results in the uncertainty in Φ_{OUT}. Mathematically, σ_{OUT} can be expressed as (11), shown at the bottom of the page, where M and N are the number of cycles for which Accumulator-1 and Accumulator-2 accumulates and then resets, respectively, T_1 is the VCO1 time period, $S\phi_1(f)$ denotes the phase noise of VCO1, T_2 is the VCO2 time period, $S\phi_2(f)$ denotes the phase noise of VCO2, and F_{VCO1} is the VCO1 frequency. Detailed derivation of (11) can be found in the Appendix.

Standard deviation of the measurement error due to phase noise is calculated to be approximately 0.06 °C and 0.17 °C for the case when the sensor is configured for a quantization error setting of 0.1 °C and 1 °C, respectively. In the present work, both VCOs consume approximately 60μW of power. A small value of σ_{OUT} (0.17 °C) compared with large quantization error (1 °C) indicates that there is an opportunity to reduce VCO power and bring σ_{OUT} close to the quantization error value.

VI. Measurement Results

The proposed temperature sensor is fabricated in a 65 nm CMOS process and operates with a supply voltage range of 0.85 V to 1.1 V (250 mV). All measured results are reported with a supply voltage of 1.0 V unless otherwise stated. The total area of this sensor is 0.004 mm^2, as shown in the die

$$\sigma_{OUT}[\text{cycle}] = \sqrt{2M\left(\frac{1}{\pi}\right)^2 \int_0^\infty S\phi_1(f)\sin^2(\pi f T_1)df + 2NF_{VCO1}^2\left(\frac{T_2}{\pi}\right)^2 \int_0^\infty S\phi_2(f)\sin^2(\pi f T_2)df} \quad (11)$$

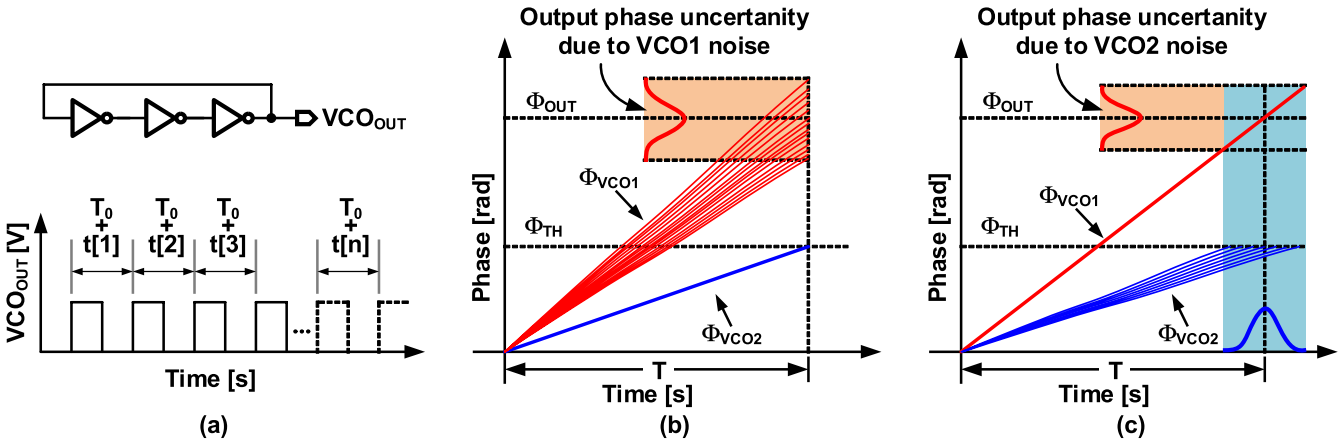

Fig. 13. Effect of VCO phase noise on sensor resolution. (a) Period uncertainty in a VCO due phase noise. (b) Effect of VCO2 phase noise on the sampled output phase Φ_{OUT}. (c) Effect of VCO1 phase noise on the sampled output phase Φ_{OUT}.

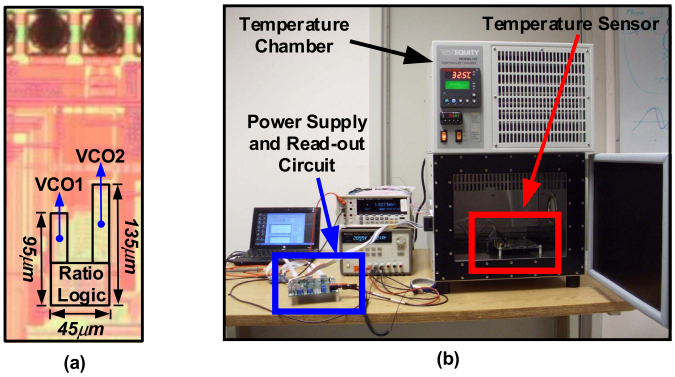

Fig. 14. (a) Die micrograph of the proposed temperature sensor. (b) Test setup for the proposed temperature sensor.

micrograph in Fig. 14(a). The die was packaged in a 10 mm $\times$10 mm, QFN package.

A photograph of the lab test setup is shown in Fig. 14(b). The sensor package is mounted on an FR4 board and placed in a temperature chamber manufactured by Test Equity (model #107). Temperature inside the chamber was accurately measured using a calibrated sensor, manufactured by Analog Devices (part #ADT7420).

The sensitivity of VCO1 and VCO2 frequency to temperature is measured, and the results are plotted in Fig. 15(a) and (b), respectively. VCO1 frequency varies from 239 MHz to 202.8 MHz with a slope of approximately -1640 ppm/°C for a temperature change from approximately 0°C to 100°C. VCO2 frequency varies from 64.37 MHz to 51.2 MHz with a slope of approximately -2260 ppm/°C for a temperature change from approximately 0°C to 100°C. As designed, the negative slope of VCO2 is steeper compared to the negative slope of VCO1 because the threshold voltage of transistors in VCO2 is smaller. The ratio of frequencies of two VCOs shows the desired PTAT characteristics, as shown in Fig. 15(c).

The linearity of the proposed temperature sensor with one-point, and two-point calibration is shown in Fig. 16(a) and (b), respectively. With one-point calibration, at 50°C, measured peak-to-peak nonlinearity with and without polynomial correction is ±3.3°C and ±4.3°C, respectively, over a temperature range of 0°C to 100°C. In the case of a two-point calibration, the calibration temperatures are 0°C and 100°C, and measured peak-to-peak nonlinearity with and without polynomial correction is ±0.9°C and ±2.3°C, respectively.

The sensitivity of VCO1 and VCO2 frequency to supply voltage variation is measured, and the results are plotted in Fig. 17(a) and (b). VCO1 frequency varies from 138.5 MHz to 258.8 MHz with a slope of 1514 ppm/mV for a supply voltage variation of 0.75 V to 1.1 V. VCO2 frequency varies from 37.04 MHz to 68.38 MHz with a slope of 1500 ppm/mV for a supply voltage variation of 0.75 V to 1.1 V. It can be observed that both VCO1 and VCO2 have approximately the same sensitivity to the supply. The sensitivity of load capacitance (C_{DB}) of VCO2 to supply voltage helps to match the supply sensitivity of the two oscillators. Temperature sensor error due to supply voltage variation was measured for seven test chips at 30°C and 70°C, and the results are shown in Fig. 18(a) and (b). For these measurements, the supply voltage was varied by 200 mV, ranging from 0.85 V to 1.05 V. At 30°C, the measured peak-to-peak variation is 6.4°C for 200 mV of DC supply voltage variation, which is equivalent to a supply sensitivity of 0.032°C/mV. At 70°C, the measured peak-to-peak variation is 7.4°C for 200 mV of DC supply voltage variation, which is equivalent to a supply sensitivity is 0.037°C/mV. In the current implementation, the junction capacitance (C_{DB}) is fixed, which resulted in limited supply noise cancellation. However, if this capacitance is trimmed based on the operating supply voltage, reduced supply sensitivity could be achieved over a wide variation of supply voltage and across process corner.

Power consumption of the proposed sensor is measured across temperature, and the results are shown in Fig. 19(a). Operating at 1 V, the proposed temperature sensor consumes 154 μW at room temperature. Power in the synthesized logic blocks is approximately 94 μW while the VCOs consume approximately 60 μW. In fine process nodes, logic power is expected to reduce and consequently, the sensor is expected

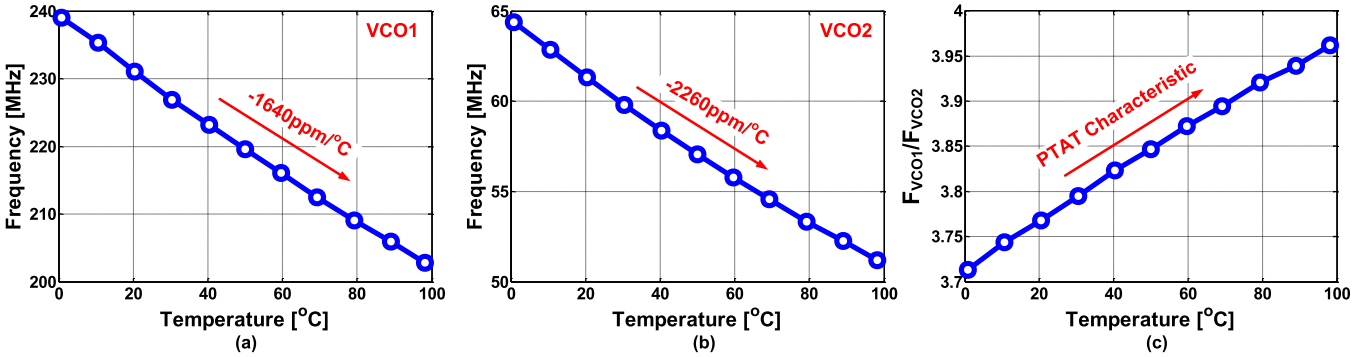

Fig. 15. (a) Measured VCO1 frequency (F_{VCO1}) versus temperature. (b) Measured VCO2 frequency (F_{VCO2}) versus temperature. (c) Measured frequency ratio of VCO1 frequency over VCO2 frequency (F_{VCO1}/F_{VCO2}) versus temperature.

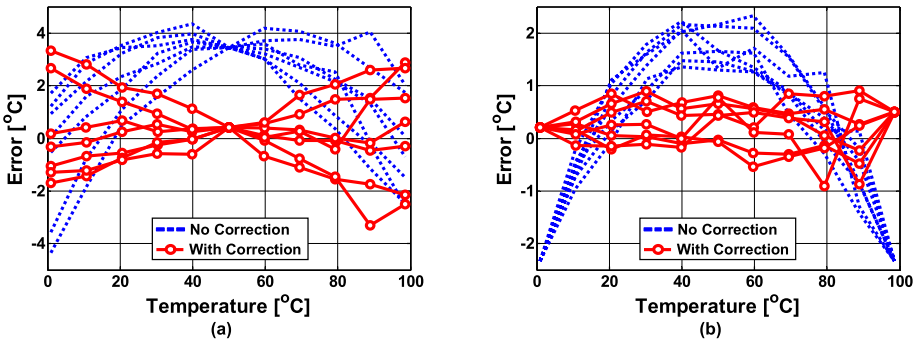

Fig. 16. Measured linearity of seven test chips for (a) one-point calibration at 50 °C with and without polynomial correction. (b) Two-point calibration at 0 °C and 100 °C with and without polynomial correction.

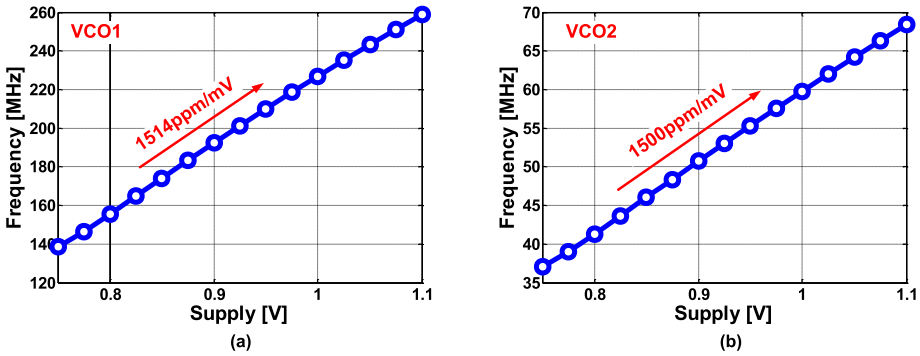

Fig. 17. (a) Measured VCO1 frequency (F_{VCO1}) versus supply. (b) Measured VCO2 frequency (F_{VCO2}) versus supply.

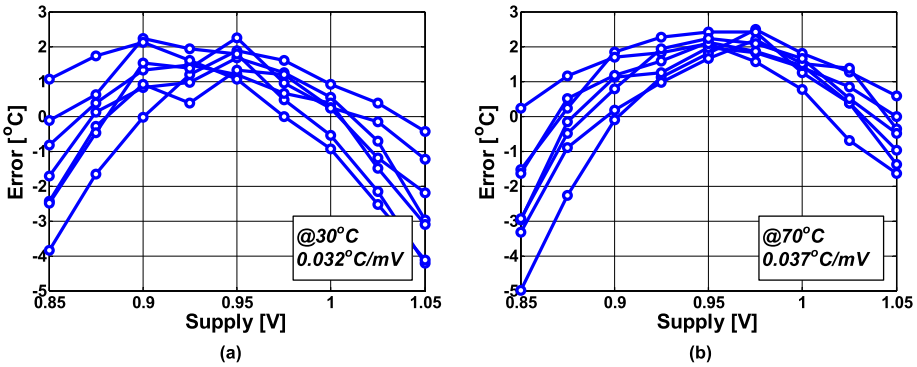

Fig. 18. (a) Measured temperature sensor error versus supply voltage for seven test chips operating at 30 °C. (b) Measured temperature sensor error versus supply voltage for seven test chips operating at 70 °C.

to become more energy efficient. In case of end-of-the-road-map technologies, the sensor power will be dominated by the VCO power, which can be easily traded off with the desired resolution.

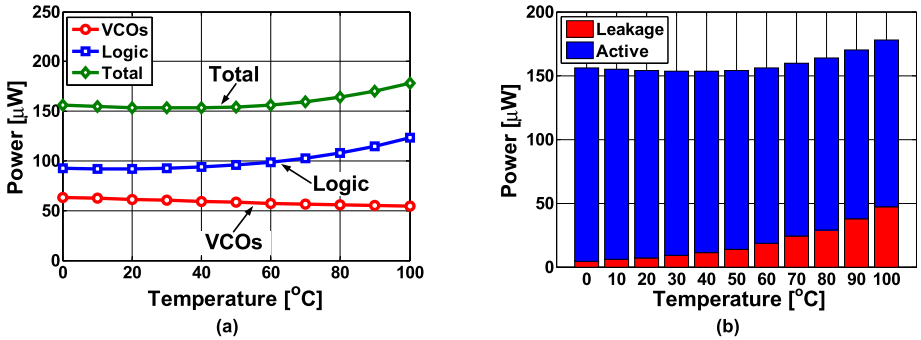

Fig. 19. (a) Measured power break down versus temperature. (b) Measured power components versus temperature.

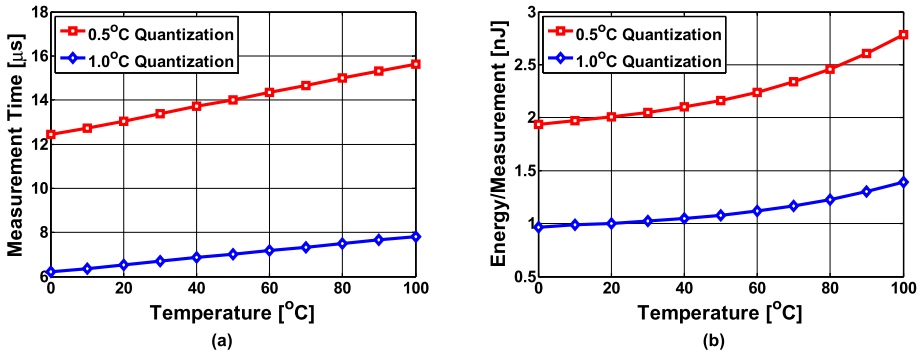

Fig. 20. (a) Measurement time versus temperature for two different quantization error settings. (b) Energy/measurement versus temperature for two different quantization error settings.

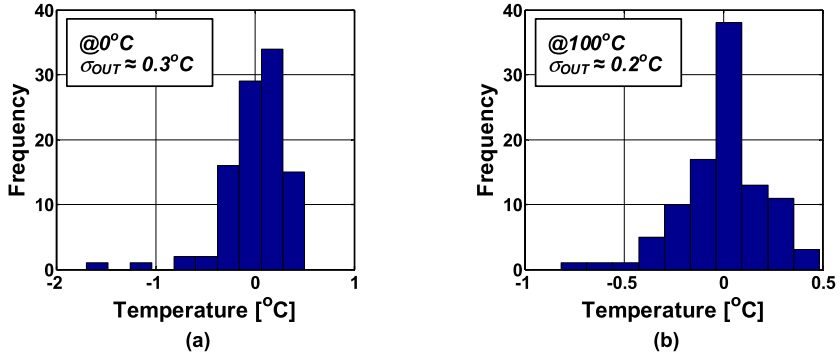

Fig. 21. (a) Measured histogram of 100 sensor readings at 0 °C. (b) Measured histogram of 100 sensor readings at 100 °C.

Leakage and active power component of the sensor are measured versus temperature, and the plot is shown in Fig. 19(b). At high temperatures, VCO frequency reduces, which reduces the active power. However, leakage in logic and VCO increase at high temperature and as a result total power consumption of the sensor increases.

Measurement time, also known as conversion time of the proposed sensor, is measured across temperature for two quantization error settings, and the results are shown Fig. 20(a). The amount of quantization error can be altered by changing the threshold count (Φ_{TH}). At 20 °C, the sensor takes approximately 6.5 μs and 13 μs to complete the measurement for a quantization error of 1 °C and 0.5 °C, respectively. Energy-per-measurement versus temperature for two quantization error settings is shown Fig. 20(b). At 20 °C, the sensor takes approximately 1 pJ and 2 pJ to complete the measurement for a quantization error of 1 °C and 0.5 °C, respectively.

A lower bound on the measured sensor resolution is obtained by measuring the spread of sensor error at 0 °C and 100 °C, as shown in Fig. 21(a) and (b), respectively. At 0 °C and 100 °C, the standard deviation of the measurement is 0.3 °C and 0.2 °C, respectively. The spread in the measured error is due to phase noise of VCOs and temperature fluctuations inside the chamber. According to the specifications of the Test Equity (model #107), the chamber has a control tolerance (short term variations after stabilization) of ±0.5 °C, and a uniformity (variation throughout the chamber after stabilization) of ±1 °C. Based on the phase noise simulation and calculations in Section V and specifications of the temperature chamber, we think that the minimum achievable resolution is

TABLE I

PERFORMANCE COMPARISON OF THE PROPOSED TEMPERATURE SENSOR WITH STATE-OF-THE-ART DESIGNS

	This Work	JSSC'14 [17]	ISSCC'14 [8]	TCAS-I'13 [18]	VLSI'08 [28]	JSSC'15 [29]	CICC'15 [30]	CICC'15 [10]	CICC'15 [31]	JSSC'15 [2]
Technology	**65nm**	180nm	160nm	65nm	65nm	65nm	65nm	40nm	180nm	14nm
Type	**MOSFET**	MOSFET	DTMOST	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	p-n diode	BJT
Area[mm^2]	**0.004mm^2 + 0.0042mm^2** †	0.09mm^2	0.085mm^2	0.008mm^2	0.0012mm^2	0.000279mm^2 +	0.00003mm^2 +	0.058mm^2	0.00055mm^2	0.0087mm^2
Supply[V]	**0.85-1.05**	1.2	0.85-1.2	1	1.1	0.6-1	0.4-1	0.5 and 1	1.8	1.35
External Clock Reference	**NO**	NO	NO	NO	YES	NO	NO	NO	NO	NO
Supply Regulator	**NO**	NO	NO	YES	NO	NO◇	NO	NO	NO	NO*
Temperature Range[°C]	**0-100°C**	0-100°C	-40-125°C	0-110°C	40-100°C	0-100°C	0-100°C	-40-100°C	35-100°C	0-100°C
Resolution[°C]	**0.3°C**	0.3°C	0.063°C	0.18°C	1°C	N/A	N/A	0.02°C	N/A	0.5°C
Measurement (Conversion) Time[s]	**22μs (0.3°C Quant.)** / **6.5μs (1°C Quant.)**	30ms	6ms	2.1μs	1ms	50μs	N/A	20μs	0.5s	20μs
Calibration or Trim	**2-point**	2-point	1-point	1-point	N/A	2-point	2-point	2-point	N/A	2-point
Inaccuracy[°C] (w/ and w/o correction)	**±0.9°C (w/)@1V** / **±2.3°C (w/o)@1V**	+1.5°C/-1.4°C	+0.4°C/-0.4°C	±1.5°C	3.1°C	+1.5°C/-2.4°C	+0.6°C/-0.4°C	+0.97°C/-0.95°C	±0.1°C	3.3°C
Power	**154μW@1V**	71nW	600nW	500μW	N/A	0.36mW	N/A	241μW	3.96μW	1.1112mW
Energy/Measurement[J]	**3.4nJ (0.3°C Quant.)** / **1nJ (1°C Quant.)**	2.2nJ	3.6nJ	1.1nJ	N/A	18nJ	1pJ	4pJ	1.98μJ	22.8nJ
FoM[nJK^2]	**0.3**	0.198	0.0141	0.97	N/A	N/A	N/A	0.0016	N/A	5.7
Supply Sensitivity[°C/mV]@DC	**0.034°C/mV** △	0.014°C/mV	0.00045°C/mV	(regulated)	0.018°C/mV	0.0008°C/mV	N/A	N/A	N/A	N/A

† Off-chip non-linearity correction logic area is approximately 0.0042mm^2.

△ Measured for DC voltage variation from 0.85V to 1.05V. To achieve even lower sensitivity in the presence of DC voltage variations, a regulator such as in [18] (≈0.001mm^2) can be utilized.

+ Reported area is without read-out circuit.

◇ Requires a fixed bias voltage, which is less than supply.

*** Area of linear voltage regulator used for sigma delta ADC is included in the reported area.**

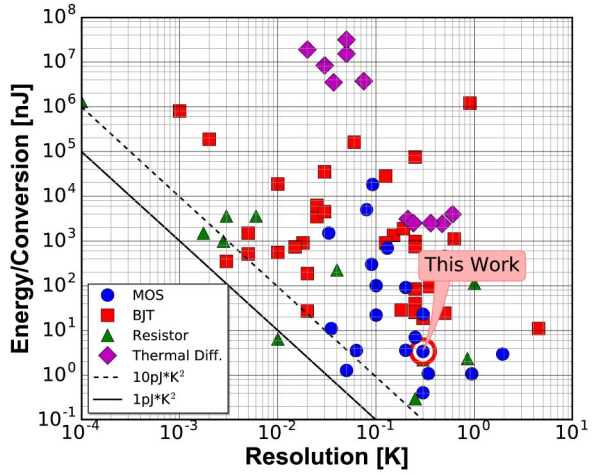

Fig. 22. Graphical comparison of the proposed sensor in the energy-per-measurement versus resolution plot [25].

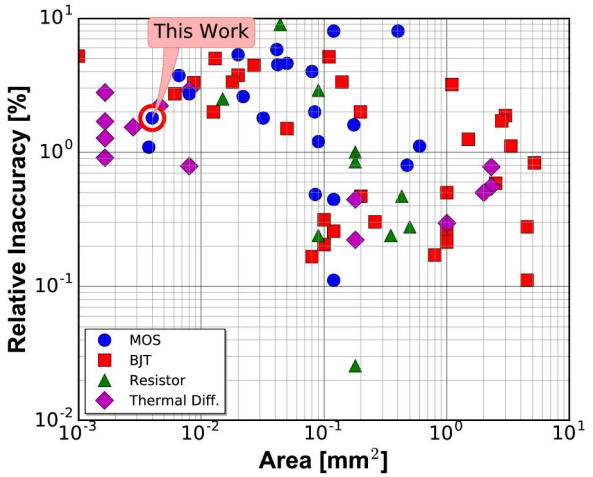

Fig. 23. Graphical comparison of the proposed sensor in the relative inaccuracy versus area plot [25].

primarily limited by the thermal stability of the temperature chamber.

Table I compares the proposed sensor with the state-of-the-art temperature sensors. A graphical comparison of the

proposed sensor with all previously published temperature sensors is shown in Figs. 22 and 23 [25]. The proposed sensor does not use any external clock reference or voltage regulators. It is designed with digital logic gates, and it achieves a competitive supply sensitivity of 0.034 °C/mV and a resolution FoM of 0.3 nJK^2, within a compact area of 0.004 mm^2.

VII. Conclusion

A self-referenced temperature sensor designed with logic gates was presented. The sensor works on the principle of converting temperature to frequency information to digital bits. A novel temperature measurement technique by creating threshold voltage difference between the transistors used in oscillators was proposed. RSCE of planar transistors was leveraged to create threshold voltage difference. Supply sensitivity of the sensor is reduced by employing junction capacitance. Therefore, the overhead of voltage regulators and an external ideal reference frequency were avoided. The effect of phase noise on achievable sensor resolution was evaluated. The prototype temperature sensor was fabricated in 65 nm CMOS technology and occupies an active die area of 0.004 mm^2. It achieves a supply sensitivity of 0.034 °C/mV, a resolution FoM of 0.3 nJK^2, and its peak-to-peak nonlinearity with and without polynomial correction is ±0.9 °C and ±2.3 °C, respectively, with two-point calibration over a temperature range from 0 °C to 100 °C.

Appendix

Phase noise of VCO1 and VCO2 are uncorrelated, and their effect on sensor resolution is analyzed in this appendix.

A. Effect of VCO1 Phase Noise

Let us assume that the random variable P, which denotes period jitter of VCO1, is wide-sense stationary with zero mean, white PSD, and P[n] denotes error in the nth VCO period. Let K denote the random process representing uncertainty in the sampled phase Φ_{OUT} and K_i denote the random variable representing uncertainty in the ith temperature measurement period. Because the Accumulator-1 accumulates for M cycles and then resets, the output jitter sequence of this accumulator is of the form {(P[1] + P[2] + P[3] + ... + P[M]), (P[M+1]+P[M+2]+P[M+3]+...+P[2M]), ...}. Assuming VCO2 is noiseless, i.e., the sampling time T is constant, the variance of sampled output phase due to noise in VCO1

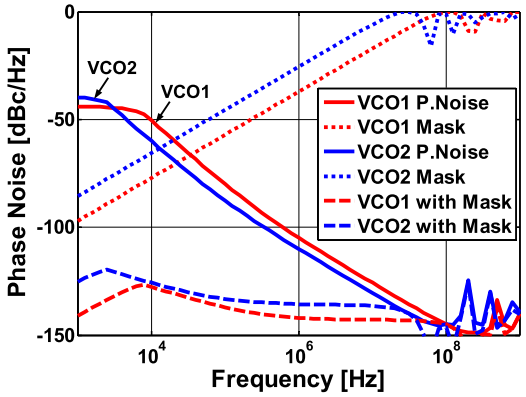

Fig. 24. Simulated phase noise of VCO1 and VCO2 along with the filter mask to obtain period jitter.

($\Phi_{OUT\text{-}VCO1}$) is equal to the variance of K_i, which can be expressed as

$$\sigma^2_{Ki} = E[(P[1] + P[2] + ... + P[M])^2] \quad (12)$$

$$\sigma^2_{OUT\text{-}VCO1}[\text{cycle}^2] = \sigma^2_{Ki} = M\sigma^2_P \quad (13)$$

where σ^2_P is the variance of the period jitter of VCO1. Here, σ^2_P can be estimated from the phase noise of VCO1 using the following expression:

$$\sigma^2_P[\text{cycle}^2] = 2\left(\frac{1}{\pi}\right)^2 \int_0^\infty S\phi_1(f)\sin^2(\pi f T_1)df \quad (14)$$

where T_1 is the VCO1 time period, $S\phi_1(f)$ denotes the phase noise of VCO1, $\sin^2(\pi f\, T_1)$ is the mask to estimate period jitter from phase noise [26], [27], as shown in Fig. 24. In (14), units of σ^2_P is cycles^2. In the next subsection, σ_P will be multiplied by the quantization error to obtain σ_P in °C.

B. Effect of VCO2 Phase Noise

Let us assume that the random variable L, which denotes period jitter of VCO2, is wide-sense stationary with zero mean and white PSD, and L[n] denotes error in the nth VCO period. Let J denote the random process representing uncertainty in measurement time T and J_i denote the random variable representing uncertainty in the ith measurement time. Because Accumulator-2 accumulates for N cycles and then resets, the output jitter sequence of this accumulator is of the form {(L[1] + L[2] + L[3] + ... + L[N]), (L[N + 1] + L[N + 2] + L[N + 3] + ... + L[2N]), ...}. Similar to (12), variance of J_i can be written as

$$\sigma^2_{Ji}[\text{sec}^2] = N\sigma^2_L \quad (15)$$

where σ^2_L is the standard deviation of the period jitter of VCO2. Here, σ^2_L can be estimated from the phase noise of

$$\sigma_{OUT}[\text{cycle}] = \sqrt{\sigma^2_{OUT\text{-}VCO1} + \sigma^2_{OUT\text{-}VCO2}} \quad (18)$$

$$\sigma_{OUT}[\text{cycle}] = \sqrt{2M\left(\frac{1}{\pi}\right)^2 \int_0^\infty S\phi_1(f)\sin^2(\pi f T_1)df + 2NF^2_{VCO1}\left(\frac{T_2}{\pi}\right)^2 \int_0^\infty S\phi_2(f)\sin^2(\pi f T_2)df} \quad (19)$$

VCO2 using the following expression:

$$\sigma_L^2[\text{sec}^2] = 2\left(\frac{T_2}{\pi}\right)^2 \int_0^\infty S\phi_2(f)\sin^2(\pi f T_2)df \qquad (16)$$

where T_2 is the VCO2 time period, $S\phi_2(f)$ denotes the phase noise of VCO2, and $\sin^2(\pi f\, T_2)$ is the mask to estimate period jitter from phase noise, (see Fig. 24). Assuming VCO1 is noiseless, using (16), variance of Φ_{OUT} due to VCO2 can be written as

$$\sigma^2_{OUT\text{-}VCO2}[\text{cycle}^2] = F^2_{VCO1}\sigma^2_{Ji}. \qquad (17)$$

Using (13) and (17), σ_{OUT} can be calculated as (18), shown at the bottom of the previous page.

The units of σ_{OUT} are converted to °C by multiplying (19), shown at the bottom of the previous page, with the quantization step size [°C/cycle]

$$\sigma_{OUT}[^oC] = \sigma_{OUT}[\text{cycle}]\text{xQuantization}[^\circ C/\text{cycle}]. \qquad (20)$$

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