A Stochastic Wireline Communication System

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***Abstract*—This paper proposes a stochastic wireline communication system. In the proposed stochastic system, the information is encoded in the statistical parameter of noise such as standard deviation, and the noise signal is transmitted on the channel. The receiver estimates the standard deviation of the received noise signal and recovers the information. A stochastic receiver architecture, which can differentiate between the noise signals with two different standard deviations is presented. Using mathematical modeling, this paper demonstrates that the proposed stochastic transceiver has a potential to improve the SNR by more than 3dB over a conventional uncoded deterministic transceiver.**

I. Introduction

The proliferation of data-rich services has fueled the demand for high-speed device-to-device communication. To address this demand, data rates in wireline communication has been increasing exponentially [1]. The insertion loss of wireline channels increases with frequency, and, therefore, at higher data rates, the wireline channel becomes noise limited and bandwidth limited. Bandwidth limitation results in inter-symbol-interference (ISI), which can be overcome with the help of equalization techniques such as feed forward equalization (FFE) [2], decision feedback equalization (DFE) [4], and integrated pulse width modulation (iPWM) [5]. On the other hand, high noise at the receiver input reduces the signal to noise ratio (SNR) and results in high bit error rate (BER), which is unacceptable to several applications.

Traditionally, there are 2 popular ways to improve the SNR: (a) increase the signal power launched by the transmitter, and (b) use forward error correction techniques such as low density parity check (LDPC) and Turbo codes to improve BER thereby increasing the SNR. Increasing the signal power at the transmitter comes at the cost of an increase in the transmitter power consumption. For example, a 3dB increase in SNR doubles the transmitter power (output driver) consumption. Moreover, in wireline links, the output signal swing is limited by the supply voltage available at the transmitter. In fine CMOS process, the available supply voltage is less than 1V for the core devices, and therefore, it is difficult to launch more than 500mV signal in a 50Ω terminated wireline channel. Forward error correction codes (FEC) such as LDPC and Turbo can help to provide effective SNR gain by improving the BER [6]. However, these codes require large code block size ((2048, 1723) LDPC) to reduce the coding overhead and need several iterations to converge resulting in large latency (660ns [7]). Such large latency is not acceptable in memory-to-processor or processor-to-processor communication links.

While noise in a conventional communication system is an undesirable quantity, one can leverage noise as a means to perform secret key exchange in a secure way [8], [9]. This paper proposes a stochastic wireline transceiver architecture, which can communicate information by encoding the digital bits in the standard deviation of noise signal, as shown in Fig. 1. This paper demonstrates that the proposed stochastic transceiver has a potential to improve the BER, which results in effective SNR improvement of more than 3dB over a conventional wireline transceiver.

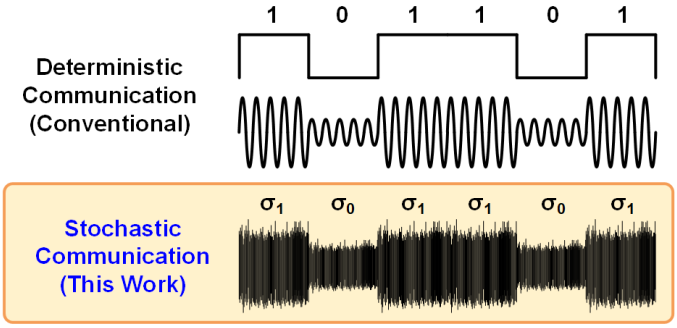

Fig. 1. Conventional deterministic communication and proposed stochastic communication.

The rest of the paper is organized as follows. Section II introduces the proposed stochastic wireline transceiver architecture. A mathematical model of the stochastic transceiver and BER derivation is presented in Section III. Simulation results of stochastic wireline link on a wireline channel are presented in Section IV. Finally, Section V concludes this paper.

II. Proposed Stochastic Transceiver

Architecture of the proposed stochastic wireline transceiver and the associated timing diagram is shown in Fig. 2. The transmitter consists of two Gaussian noise sources NS_0 and NS_1, which are represented by random variable N_0 (mean = 0, σ_0) and N_1 (mean = 0, σ_1), respectively. When a logic 1 has to be transmitted then, NS_1 is connected to the channel, and when logic 0 has to be transmitted, then NS_0 is connected to the channel. The stochastic receiver estimates the standard deviation of noise of the received signal to detect whether the transmitted signal is logic '0' or logic '1'.

There can be several ways to estimate the standard deviation of the received signal. One way is to digitize the received signal with an ADC and process the ADC output to estimate the standard deviation. In the proposed transceiver, only two bits are transmitted {0 and 1}, and therefore, the receiver can determine if the received signal is logic 0 or logic 1 by simply

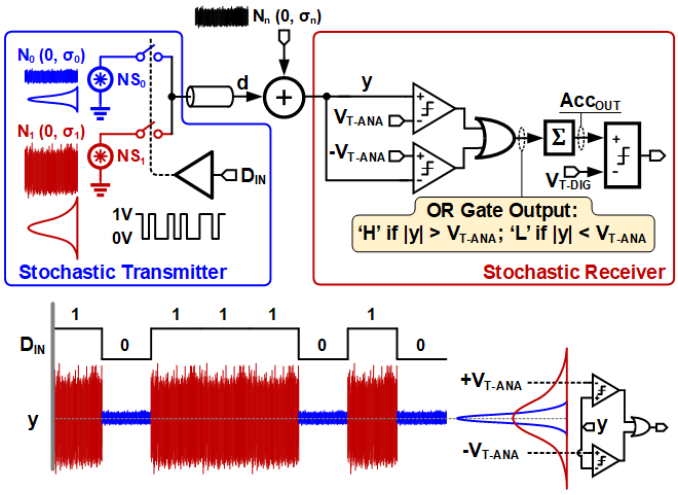

Fig. 2. Proposed stochastic wireline transceiver architecture and timing diagram.

checking if the standard deviation of the received signal is above or below a certain threshold.

The proposed stochastic receiver consists of two slicers, which slices the received noise signal at two threshold voltages $V_{T\text{-}ANA}$, and $-V_{T\text{-}ANA}$. The outputs of the slicers are logically ORed. If the received signal is above $V_{T\text{-}ANA}$ or below $-V_{T\text{-}ANA}$, the output of the OR gate is high (H) else the output is low (L). The output of the OR gate is accumulated in a digital accumulator. At the end of bit duration, the output of the accumulator (Acc_{OUT}) is compared against the digital threshold ($V_{T\text{-}DIG}$). If the Acc_{OUT} is above the $V_{T\text{-}DIG}$, then it is determined that the received bit is '1', else it is '0'.

To increase the accuracy of estimating the standard deviation of the received signal, the receiver takes multiple samples of the received signal and accumulate the output (mathematically proved in Section III-A). At high data rates, the time period of the data bit reduces to few 10s of picoseconds, which makes it difficult to take multiple samples from two slices in a single bit period. In that case, a bank of slicers can be employed, which are sampled at different clock phases.

III. Mathematic Model of Stochastic Transceiver

Let us assume that in the proposed stochastic transceiver, the logic 1 is transmitted by Gaussian noise source with standard deviation σ_1 and logic 0 is transmitted by Gaussian noise source with standard deviation σ_0. Let k denotes the ratio of slicer threshold normalized to σ_1, that is, $k = V_{T\text{-}ANA}/\sigma_1$.

A. Bit Error Rate Calculation

Let $P_{H/1}$ denotes the probability that the OR gate output will be high (H) such that logic 1 was transmitted, and $P_{L/1}$ denotes the probability that the OR gate output will be low (L) such that logic 1 was transmitted. A graphical representation of the above-mentioned probabilities is shown in Fig. 3. $P_{H/1}$ and $P_{L/1}$ are mathematically expressed as:

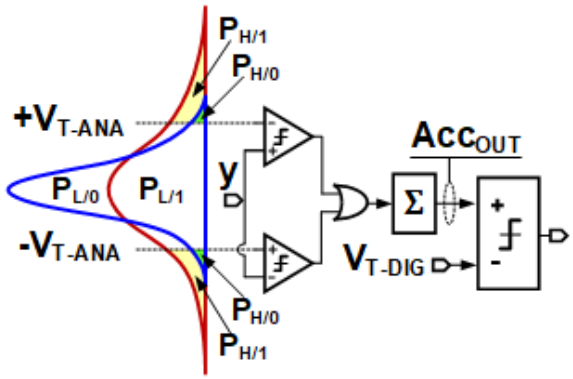

Fig. 3. Graphical representation of probabilities $P_{H/1}$, $P_{H/0}$, $P_{L/1}$ and $P_{L/0}$ in the received signal.

$$P_{H/1} = \frac{2}{\sigma_1\sqrt{2\pi}} \int_{k\sigma 1}^{\infty} e^{\frac{-x^2}{2\sigma_1^2}} dx; \quad P_{L/1} = 1 - P_{H/1} \tag{1}$$

Let $P_{H/0}$ denotes the probability that the OR gate output will be high (H) such that logic 0 was transmitted and $P_{L/0}$ denotes the probability that the OR gate output will be low (L) such that logic 0 was transmitted. $P_{H/0}$ and $P_{L/0}$ is mathematically expressed as:

$$P_{H/0} = \frac{2}{\sigma_0\sqrt{2\pi}} \int_{k\sigma 1}^{\infty} e^{\frac{-x^2}{2\sigma_0^2}} dx; \quad P_{L/0} = 1 - P_{H/0} \tag{2}$$

In the proposed receiver, multiple samples are taken by the slicer to detect the standard deviation. Let 'S' denotes the number of samples of the slicer used to detect if the received bit is logic 1 or logic 0. The receiver makes a decision on the received signal based on the following two conditions:

1) If $Acc_{OUT} \geq V_{T\text{-}DIG} \Rightarrow$ Logic 1
2) If $Acc_{OUT} < V_{T\text{-}DIG} \Rightarrow$ Logic 0

where Acc_{OUT} is the output of the accumulator (see Fig. 3) such that $Acc_{OUT} \leq S$. A bit error can occur based on the following two conditions:

1) If $Acc_{OUT} < V_{T\text{-}DIG}$ and transmitted bit was Logic 1
2) If $Acc_{OUT} \geq V_{T\text{-}DIG}$ and transmitted bit was Logic 0

The probability of occurrence of the first condition $P_{0/1}$ = probability of detecting the received bit as logic 0 such that logic 1 was transmitted. Mathematically, $P_{0/1}$ can be written as:

$$P_{0/1} = P(Acc_{OUT} = 0|1) \text{ OR } P(Acc_{OUT} = 1|1) \text{ OR } \ldots P(Acc_{OUT} = V_{T-DIG} - 1|1) \tag{3}$$

where $P(Acc_{OUT} = m|1)$ is the probability of getting m OR gate outputs as H such that logic 1 was transmitted. The $P(Acc_{OUT} = m|1)$ can be expressed as:

$$P(Acc_{OUT} = m|1) = \binom{S}{m} (P_{H/1})^m (P_{L/1})^{S-m} \tag{4}$$

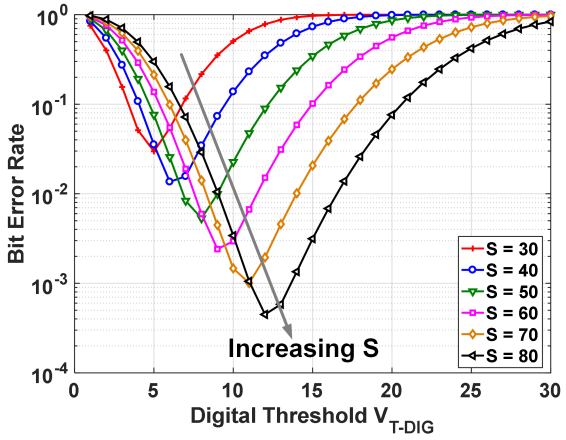

Fig. 4. Plot of BER versus $V_{T\text{-}DIG}$ for various S at k=1, and $\sigma_1 = 2\sigma_0$.

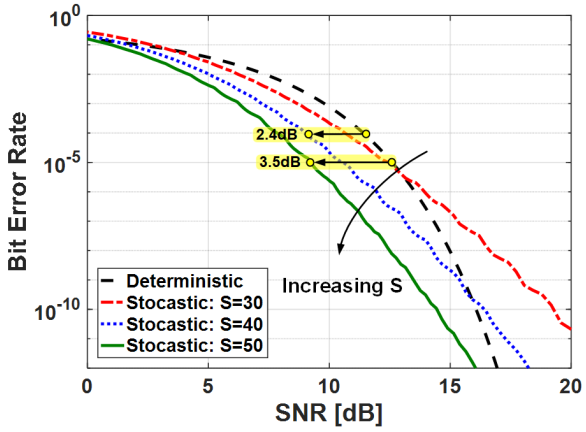

Fig. 5. Plot of BER versus SNR for various samples (S) per data bit.

From equations (3) and (4), $P_{0/1}$ can be written as:

$$P_{0/1} = \sum_{i=0}^{V_{T-DIG}-1} \binom{S}{i} (P_{H/1})^{i} (P_{L/1})^{S-i} \tag{5}$$

For the second bit error condition, the $P_{1/0}$ = Probability of detecting the received bit as logic 1 such that logic 0 was transmitted. Mathematically, $P_{1/0}$ can be written as:

$$P_{1/0} = P(Acc_{OUT} = V_{T-DIG}|0) \text{ OR } P(Acc_{OUT} = V_{T-DIG}+1|0) \text{ OR } ... \text{ } P(Acc_{OUT} = S|0) \tag{6}$$

where $P(Acc_{OUT} = m|0)$ is the probability of getting m OR gate outputs as H such that logic 0 was transmitted. The $P(Acc_{OUT} = m|0)$ can be expressed as:

$$P(Acc_{OUT} = m|0) = \binom{S}{m} (P_{H/0})^{m} (P_{L/0})^{S-m} \tag{7}$$

From equations (6) and (7), $P_{1/0}$ can be expressed as:

$$P_{1/0} = \sum_{i=V_{T-DIG}}^{S} \binom{S}{i} (P_{H/0})^{i} (P_{L/0})^{S-i} \tag{8}$$

From equations (5) and (8), the BER of the proposed transceiver can be written as:

$$BER = P_{0/1} + P_{1/0} \tag{9}$$

Using equation (9), the effect of the number of samples (S) on BER is estimated and results are shown in Fig. 4. As S increases, the BER reduces. This is due to the fact that the accuracy of estimating the standard deviation improves by increasing the number of samples at the receiver. For S = 30 the BER is 0.029 and it improves to 4.49×10^{-5} for S = 80.

B. Stochastic Transceiver in the Presence of Noise

In the proposed stochastic transceiver, bit error rate depends on the standard deviation of the noise source σ_0, σ_1, and architectural parameters such as number of samples taken at the receiver (S), analog threshold ($V_{T\text{-}ANA}$), and digital threshold ($V_{T\text{-}DIG}$). Since, the additive white Gaussian noise (AWGN) represented by random variable N_n (see Fig. 2) is independent to the noise generated by the transmitter for representing logic 0 and 1, the addition of AWGN results in the change of standard deviation of the noise for logic 0 an logic 1 at the receiver. In the presence of noise, the standard deviation of the received signal for logic 0 (σ_{0R}) and logic 1 (σ_{1R}) are written as:

$$\sigma_{0R} = \sqrt{\sigma_0^2 + \sigma_n^2}; \quad \sigma_{1R} = \sqrt{\sigma_1^2 + \sigma_n^2} \tag{10}$$

In the proposed stochastic transmitter, the signal is contained in the standard deviation difference of NS_1 and NS_0. Therefore, signal power can be expressed as $\sqrt{\sigma_1^2 - \sigma_0^2}$. The signal to noise ratio (SNR) of the proposed stochastic transceiver can be expressed as:

$$SNR[dB] = 20 \times \log\left(\frac{\sqrt{\sigma_1^2 - \sigma_0^2}}{\sigma_n}\right) \tag{11}$$

Using equations (9) to (11), the BER of the proposed stochastic transceiver is calculated at different SNRs for various values of S, and the plot is shown in Fig. 5. For S=40, the proposed stochastic receiver achieves 7.9×10^{-5} BER at 9dB SNR, and for S=50, the proposed stochastic receiver achieves 1.4×10^{-5} BER at 9dB SNR, which is equivalent to 2.4dB, and 3.5dB effective SNR improvement, respectively, over the conventional uncoded deterministic wireline transceiver.

IV. Stochastic Transceiver Simulations

Operation of the proposed stochastic transceiver is demonstrated by simulating a 2Gb/s wireline transceiver in Cadence using a wireline channel with a loss of -4.6dB at 1GHz and -22.6dB at 10GHz. For these simulations, PRBS-7 data was

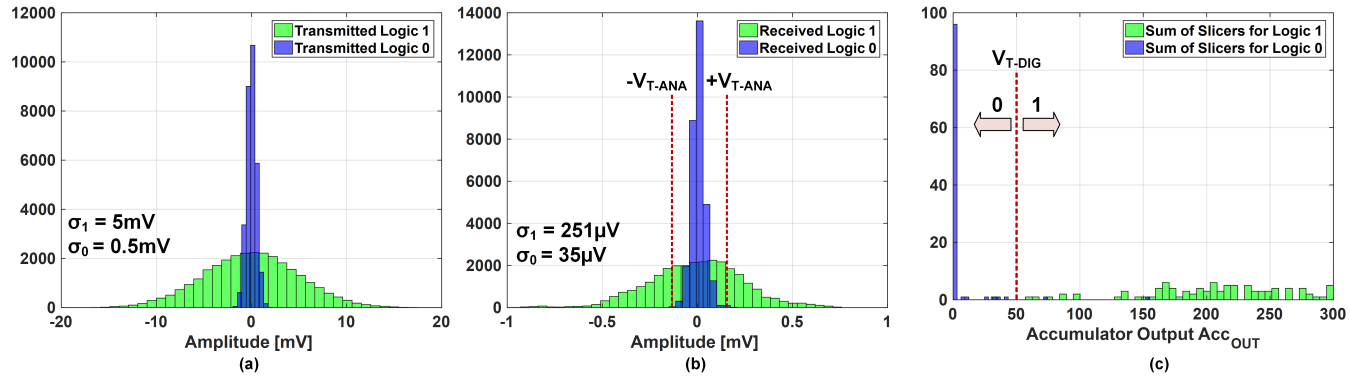

Fig. 6. (a) Histogram of the transmitted stochastic PRBS-7 data. (b) Histogram of the received stochastic PRBS-7 data. (c) Histogram of the accumulator output Acc_{OUT}.

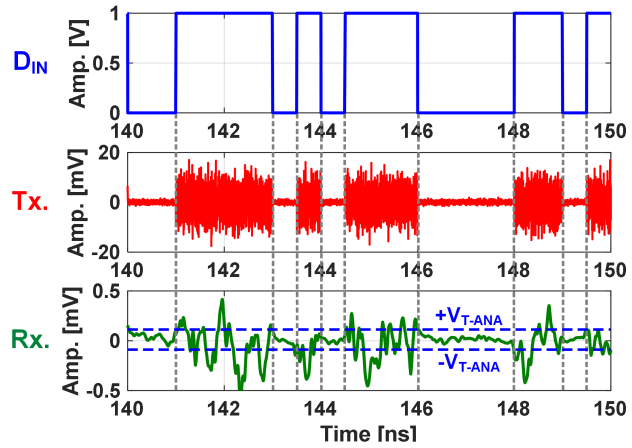

Fig. 7. Transient of PRBS-7 data. D_{IN}: Digital data to be transmitted, Tx.: Stochastic data launched on the channel, and Rx.: Stochastic data at the receiver input.

transmitted and received. For logic 1, σ_1=5mV and for logic 0, σ_0=0.5mV is launched on the wireline channel. Histogram of the transmitted noise waveform on the channel is shown in Fig. 6(a).

The transient waveform of the transmitted and received data is shown in Fig. 7. Histogram of the received data is shown in Fig. 6(b). The standard deviation of the received logic 1 and logic 0 is 251μV and 35μV, respectively. At the receiver, $\text{V}_{\text{T-ANA}}$ is set to 100μV and S=300. A plot of histogram of the Acc_{OUT} is shown in Fig. 6(c). It can be observed that by setting $\text{V}_{\text{T-DIG}}$=50, logic 1 and logic 0 can be detected. These results demonstrate that successful stochastic communication can be achieved on a wireline channel.

V. Comparison and Conclusion

The proposed stochastic wireline communication has several advantages over a deterministic wireline communication:

1) The proposed stochastic wireline transceiver can achieve SNR improvement (more than 3dB) over a conventional deterministic transceiver.
2) By increasing the number of samples taken at the slicer to detect the received bit, the SNR of the stochastic transceiver can be further improved much more than what has been achieved in Fig. 5.
3) Stochastic communication is orthogonal to any other means SNR improvement techniques, forward error correction codes can be used along with the proposed stochastic transceiver to improve the SNR even further.
4) In future, investigation in efficient standard deviation estimation approach can help to reduce the number of samples required to achieve SNR improvement.

This paper presented a wireline transceiver architecture, which can achieve communication by transmitting noise signals. Operation of the proposed transceiver was successfully demonstrated by achieving stochastic communication on a lossy wireline channel.

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