

29.4 A 16Gb/s 3.6pJ/b Wireline Transceiver with Phase Domain Equalization Scheme: Integrated Pulse Width Modulation (iPWM) in 65nm CMOS

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Asymmetric links such as memory interfaces and display drivers require the transmitter to perform necessary equalization, while the receiver remains simple and has minimal or no equalization capability. Traditionally, FFE-based equalization techniques on power-efficient voltage-mode drivers have been used on the transmit end. Based on the FFE tap resolution requirement, the output driver and pre-driver are divided into multiple segments. Although such a segmented FFE implementation helps to maintain a constant output termination impedance (50Ω) across all tap settings, it comes at the cost of (a) increased signaling power, and (b) increased switching power since multiple segments are required to achieve desired linearity [1]. Phase domain equalization techniques, such as pulse width modulation (PWM), can equalize the channel without increasing signaling power or segmenting the output driver. However, PWM encoding requires the insertion of a precise narrow pulse in every data bit, which necessitates very wide bandwidth in the high-speed data path, resulting in poor energy efficiency [2] and difficulty in scaling PWM encoding to higher data rates [3]. For example, creating a 10% duty cycle on a 64Gb/s PWM data stream would require a pulse width of 1.5ps with less than 1ps of rise/fall time at the transmitter output. Other phase domain pre-emphasis techniques are ineffective for high-loss channels [4]. In view of these limitations, we present a new phase-domain equalization technique: integrated pulse width modulation (iPWM) in a 16Gb/s transceiver, which can equalize 19dB of channel loss, while consuming 57.3mW power. Compared to state-of-the-art PWM designs, the proposed iPWM scheme achieves 36 \times better energy efficiency for the same data rate [2], and 3.2 \times higher data rate for the same energy efficiency [3].

Figure 29.4.1 shows the proposed iPWM concept. The iPWM modulation is built on the observation that it is possible to reduce post-cursor ISI by reducing the pulse width of the transmitted data bits. Pulse width reduction can be achieved by scaling and adding up the widths by which individual bits are reduced, and appending them at the end of consecutive identical digits (CIDs). Consequently, narrow pulse widths do not need to be precisely reproduced at the transmitter output. Importantly, the bandwidth requirement on the high-speed data path in case of iPWM is the same as that of NRZ modulation, which helps in increasing the data rates without exponentially increasing the switching power. Furthermore, the conventional PWM scheme has a lower limit on the minimum pulse width that can be transmitted because of the bandwidth limitation on the data path, which often results in over equalizing a low loss channel. On the other hand, the proposed iPWM scheme can change the pulse width of CIDs with high precision (~ 3 ps in this work), which helps to equalize a wide range of channel losses. The equalizing nature of iPWM can be visualized from the measured power spectral density of transmitted data (see Fig. 29.4.1), which demonstrates the amplification of the high-frequency component of the spectrum.

Figure 29.4.2 shows the block diagram of the proposed transceiver. The transmitter consists of a 32b wide parallel PRBS generator, a 32:4 multiplexer, a 4-tap integrated pulse width modulator, and a source-series terminated output driver. The receiver consists of a two-stage continuous time linear equalizer (CTLE), amplifiers, quarter rate samplers, a 4:32 de-multiplexer, and a PRBS checker. An off-chip PLL is used to provide a half-rate clock to the transceiver. The iPWM consists of 3 independently tunable coefficients: α_1 , α_2 and α_3 . The XOR and XNOR logic to generate necessary control signals for iPWM are implemented at lower data rates (before the 4:1 mux), which helps to reduce the switching power.

Figure 29.4.3 shows the block diagram of the proposed integrated pulse width modulation circuit. Tunable coefficients α_1 , α_2 and α_3 , are implemented in 3 independent iPWM logic stages and are enabled with control signals, Ctrl1, Ctrl2, and Ctrl3, respectively. These stages are cascaded together, due to which the pulse width modification by the n^{th} stage can be accumulated with the modification done by the $n+1^{\text{th}}$ stage. Such cascading results in a modular design, which can be scaled to accommodate more taps to equalize even higher loss in the channels. The Ctrl1, Ctrl2, and Ctrl3 signals are asserted high in the presence of 2, 3 and 4 consecutive identical digits in the data stream, respectively. When the Ctrl signal goes high, it limits the maximum output swing on the Dint node by pulling it towards $V_{DD}/2$ (see Fig. 29.4.3). As a result, Dint settles to either $V_{DD} - \delta V$ (for logic 1) or δV (for logic 0). A lower swing on Dint helps to reduce the time to transition from 0-to-1 or 1-to-0, resulting in reduced CID pulse width. The CID pulse width reduction can be controlled using a binary weighted 4b control word ($\alpha_i[n]$) with a resolution of approximately 3ps.

Figure 29.4.4 shows the iPWM in action with measured data at the channel output. Without iPWM, the ISI caused due to 2, 3 and 4 CIDs results in undetected bits by the receiver. As the values of coefficients α_1 , α_2 and α_3 are increased, the width of CIDs is reduced. Consequently, the ISI caused by CIDs is also reduced, resulting in horizontal and vertical eye opening.

Figure 29.4.5 shows the far-end output eye openings and BER bathtub curve with iPWM for two different channel loss profiles with PRBS7 data pattern. Operating at 16Gb/s, the proposed transmitter achieves 80mV_{pp} (single-ended) and 28mV_{pp} (single-ended) vertical eye opening with channels 1 and 2, respectively. For BER $<10^{-12}$, the proposed transmitter achieves a horizontal eye opening of 24ps (0.38UI) and 16ps (0.26UI) with channels 1 and 2, respectively. The receiver performance is measured with various CTLE equalization settings. Operating at 16Gb/s, the receiver alone can equalize more than 3dB channel loss and achieves a horizontal eye opening of 42ps (0.67UI) and 12ps (0.19UI) with and without CTLE equalization for BER $<10^{-12}$, respectively.

Operating at 16Gb/s, the complete transceiver consumes 57.3mW of power from 0.9V/1V/1.1V supply, can equalize more than 19dB loss and occupies an active area of 0.21mm². The performance of the proposed transceiver is compared with the state-of-the-art in Fig. 29.4.6. This work proposed a new phase domain equalization technique and demonstrates a working prototype at 16Gb/s. The micrograph of the chip, which is fabricated in 65nm CMOS, is shown in Fig. 29.4.7.

Acknowledgment:

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References:

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- [2] H. Cheng, A. C. Carusone, "A 32/16 Gb/s 4/2-PAM transmitter with PWM pre-emphasis and 1.2 V_{pp} per side output swing in 0.13- μ m CMOS," in Proc. *IEEE CICC*, Sept. 2008, pp.635-638.
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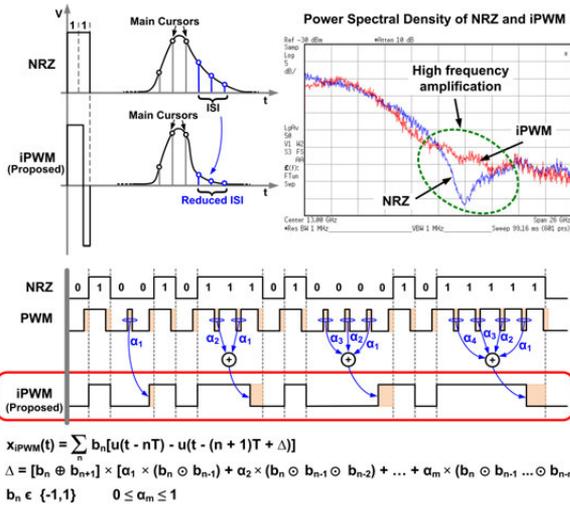


Figure 29.4.1: Time domain response and measured power spectral density of the proposed iPWM and comparison with NRZ. Evolution of iPWM from PWM and mathematical representation.

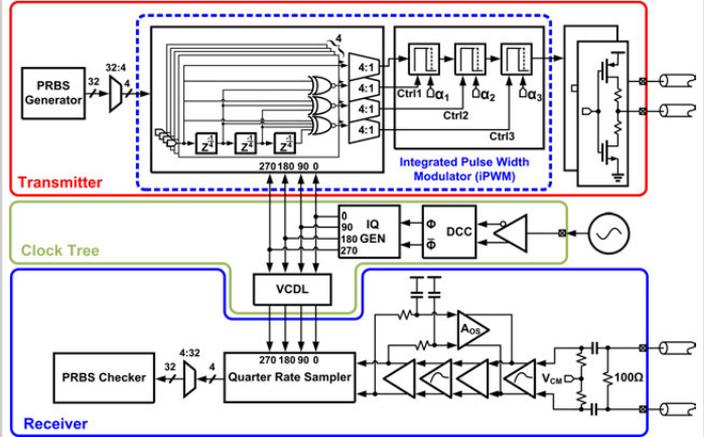


Figure 29.4.2: Block diagram of the proposed 16Gb/s transceiver.

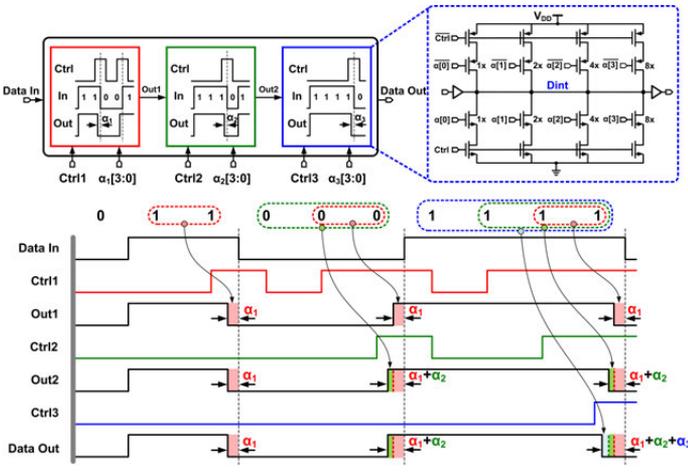


Figure 29.4.3: Block diagram of the proposed integrated pulse width modulation logic and timing diagram in the presence of consecutive identical digits.

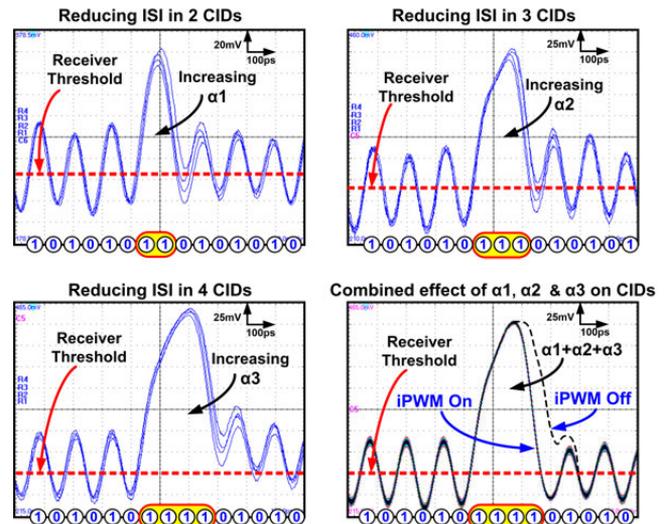


Figure 29.4.4: Measured channel output demonstrating ISI reduction in the presence of CIDs as the iPWM is turned on and coefficients are increased.

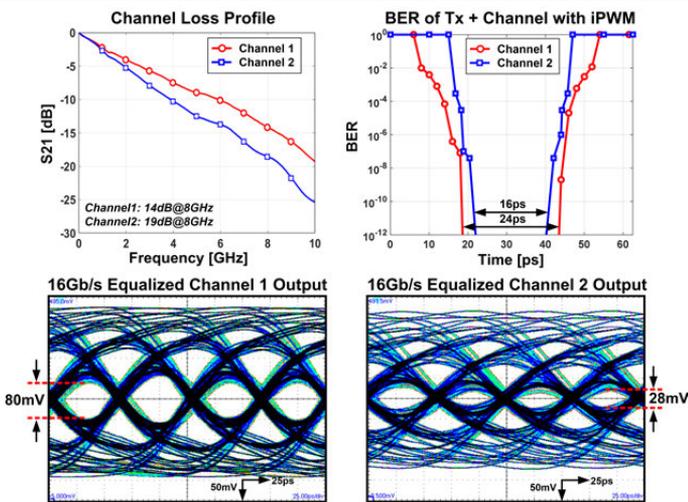


Figure 29.4.5: Insertion loss profiles of the channels. BER bathtub curves at the channel outputs with equalized 16Gb/s PRBS-7 data. Equalized eye diagrams at the far-end channel output.

	This Work	ISSCC'14, Balan	JSSC'14, [5]	JSSC'11, Zhong	JSSC'10, Wang
Technology [nm]	65	28	22	40	65
Data rate [Gb/s]	16	20	4-32	1-14	20
Tx Equalization	iPWM	2-tap FFE	3-tap FFE	4-tap FFE	3-tap FFE
Rx Equalization	CTLE	CTLE + 2-tap DFE	CTLE + 6-tap DFE	CTLE + 10-tap DFE	CTLE + 1-tap DFE
Loss [dB]	19	20	26*	26*	21.2
Tx Output Swing [V _{pp-dm}]	1	0.5	0.515	1.1	0.4
Mux-Demux Ratio	32:1	16:1	2:1	16:1	2:1
Power [mW]	57.3	130	73.6	102.5	87
Efficiency [pJ/bit]	3.58	6.5	4.6*	7.3*	4.35
Supply [V]	0.9/1.0/1.1	0.9/1.35	0.9	1.1	1.2
Area [mm ²]	0.210	0.166*	0.078	0.97*	0.070

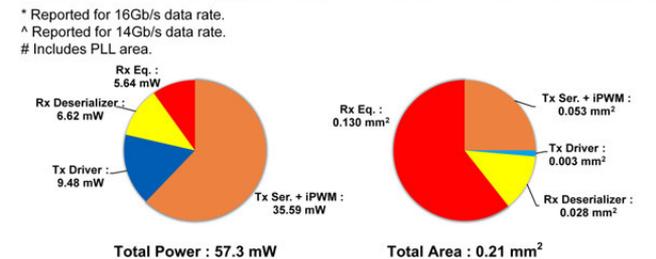


Figure 29.4.6: Performance summary and comparison with state-of-the-art designs.

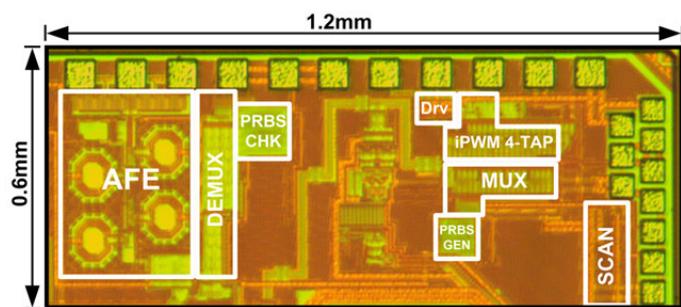


Figure 29.4.7: Die micrograph of the proposed transceiver.