16.4 A 0.5-to-0.9V, 3-to-16Gb/s, 1.6-to-3.1pJ/b Wireline Transceiver Equalizing 27dB Loss at 10Gb/s with Clock-Domain Encoding Using Integrated Pulse-Width Modulation (iPWM) in 65nm CMOS

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Improving the energy efficiency of wireline interconnects has become a necessity to sustain growing data rates. Low-voltage wireline link operation is a promising approach to achieve close to pico-joules/bit energy efficiency [1-3]. However, conventional low-voltage wireline links suffer from two limitations: (a) limited equalization (12dB) or no channel equalization, and (b) low data rates (8Gb/s @0.75V) even with fine process technology nodes [2]. Limited equalization in low-voltage links is due to the fact that conventional equalization (FFE, DFE) is performed on the high-speed data path. As a result, when the supply voltage is reduced (below 0.6V), the bandwidth of the data path is severely diminished, which compromises FFE and DFE operation. Moreover, the requirement to generate and transport narrow clock pulses in conventional low-voltage output drivers limits the maximum achievable data rates [1,3]. In view of these limitations, we propose a new approach to equalize heavy channel loss at low supply voltages by moving the equalizing operation out of the data path and into the clock path. Integrated pulse width modulation (iPWM) has been demonstrated to efficiently equalize heavy channel loss by encoding data transition edges [4]. In this work, we present a modified iPWM encoding, an energy-efficient wireline transceiver with a clock-domain low-voltage iPWM encoder, and a low-voltage multiplexer + output driver architecture, which can operate from 0.5-to-0.9V and 3-to-16Gb/s compensating 27dB channel loss at 10Gb/s with an energy efficiency of 1.8pJ/b. Compared to prior low-voltage links [2], the proposed transceiver can compensate 15dB higher loss at 25% higher data rate (10Gb/s) operating at 13% lower supply voltage (0.65V) while using an older technology node (65nm). Compared to state-of-the-art iPWM-based wireline transceiver operating at nominal supply voltage [4], the proposed transceiver achieves 2.5× lower energy/bit while compensating similar channel loss, and compared to a conventional equalization-based transceiver it compensates 8dB higher loss with similar energy efficiency [5].

Figure 16.4.1 shows the conventional FFE implementation on the high-bandwidth data path and the proposed clock domain iPWM encoding on the low-bandwidth clock path. At low supply voltages, the rise/fall time of the CMOS logic in pre-drivers and serializers increases and as a result, it fails to pass narrow data pulses, which compromises the FFE. In the proposed approach, equalization is performed by encoding the sub-rate clock edges operating at a lower supply voltage. The proposed iPWM encoding is a highly digital operation and low supply voltage implementation helps to quadratically reduce the switching power. The encoded sub-rate clock phases multiplex the data using an N:1 multiplexer, thus generating iPWM encoded data at the output. The proposed iPWM encoding is based on the observation that both pre-cursor and post-cursor ISI can be reduced by modulating the pulse width at the leading and trailing edges of the consecutive identical digits (CIDs), respectively. The position of CIDs leading and trailing edges is controlled using encoding coefficients β_m and α_m, respectively. These encoding coefficients are estimated based on the channel loss profile.

Figure 16.4.2 shows the block diagram of the proposed low-voltage transceiver. The transmitter consists of a parallel PRBS generator, 4-tap quarter-rate iPWM control signal generator and 4:1 multiplexed source-series terminated output driver. An off-chip PLL is used to provide the clock, which is divided down on-chip to quarter-rate four-phase clocks and provided to the transmitter through the iPWM encoder. The receiver consists of a passive equalizer, amplifiers and quarter-rate samplers with offset correction. At lower supply voltage, clock distribution suffers from duty cycle errors and phase offsets. In view of this, phase and duty cycle correction blocks are multiplexed between the transmitter and receiver, which help to clean up the clock phases. The quarter-rate clocks to the transmitter are encoded with the proposed iPWM.

Figure 16.4.3 shows the proposed iPWM encoder, timing diagram, and block diagram of the proposed low voltage 4:1 multiplexed 50Ω output driver. The four clock phases of the output driver are independently iPWM encoded. The tunable coefficients α_1, α_2, β_1, and β_2, are implemented in 4 independent iPWM logic stages and are enabled with control signals generated at quarter-rate. These encoding coefficients equivalently provide two pre-cursor (β_1, β_2) and two post-cursor correction taps (α_1, α_2). In the proposed clock domain iPWM encoding, pulse width modulation of CIDs is achieved by modulating the duty-cycle of the quarter-rate clocks relative to each other, which in turn modulates the CID pulse width at the serializer. Duty-cycle modulation is achieved by varying the rise and fall time using current starved inverters. Each iPWM encoder tap consists of two sets of transition-time modulators and the strength of the modulation is controlled by the tap coefficient with a precision of 0.1ps. Multiple taps can be implemented by using a cascaded architecture making the proposed design highly scalable.

In the proposed multiplexing output driver, Stg1 latches the incoming data at quarter-rate on node 'X'. Stg2 keeps the Final stage tri-stated for 3/4th of a clock cycle and propagates the latched data for 1/4th of the clock cycle. The Final stage implements a 50Ω pull-up and pull-down impedance using tuned PMOS and NMOS transistors (shaded), respectively, which are shared by all four multiplexers. Unlike conventional architectures, no narrow pulses propagate through the pre-drivers. As a result, the proposed multiplexing output driver architecture operates at high data rates at low-supply voltages.

Figure 16.4.4 shows the measured insertion loss profiles of the channels and far-end output eye openings of the transmitter with clock domain iPWM equalization for 3Gb/s, 10Gb/s and 16Gb/s PRBS7 data with 21dB, 20dB, and 24dB loss, respectively. Operating at 3Gb/s (0.5V), 10Gb/s (0.65V), and 16Gb/s (0.9V), the proposed transmitter achieves vertical eye openings of 24mV$_{pp}$, 20mV$_{pp}$, and 40mV$_{pp}$, respectively. Figure 16.4.5 shows the measured BER bathtub curves of the complete transceiver for three different data rates and FR4 channels. For BER $<10^{-12}$, the proposed transceiver achieves a horizontal eye opening of 78.8ps (0.24UI), 9.8ps (0.1UI), and 19.6ps (0.31UI) at 3Gb/s, 10Gb/s, and 16Gb/s compensating 21dB, 27dB and, 22dB of loss, respectively. The measured power spectral density of iPWM-encoded and NRZ-encoded transmitted data at 16Gb/s shows the high-frequency amplification, thus demonstrating the equalization capability of the proposed iPWM encoding. The low-frequency amplification is achieved through passive equalizers at the receiver. The effect of added noise on the clock due to the iPWM encoder is measured. In the presence of the proposed clock domain iPWM encoding at 5GHz, the RMS jitter, integrated from 1kHz to 100MHz, degrades marginally from 1.483ps to 1.487ps. The performance of the proposed transceiver is compared with the state-of-the-art in Fig. 16.4.6. Operating at 10Gb/s, the complete transceiver consumes 18mW of power from 0.65V supply, can equalize 27dB loss, and occupies an active area of 0.13mm^2. The die micrograph is shown in Fig. 16.4.7.

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[1] W. Choi, et al., "A 0.45-to-0.7V 1-to-6Gb/s 0.29-to-0.58pJ/b source-synchronous transceiver using automatic phase calibration in 65nm CMOS," *ISSCC*, pp. 66-67, Feb. 2015.
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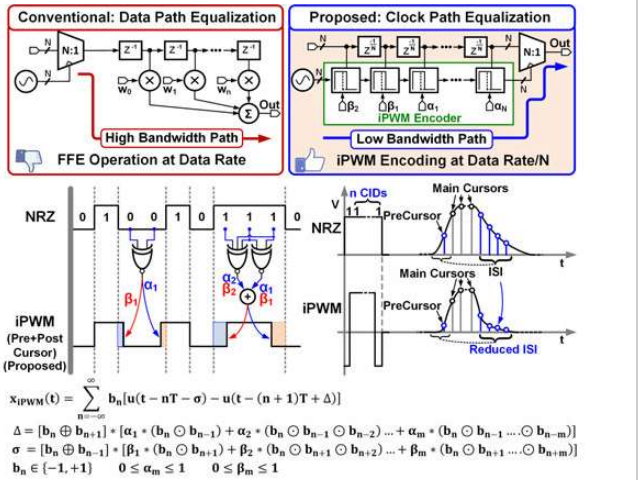

Figure 16.4.1: Conventional FFE implementation on the high-speed data path and proposed iPWM implementation on N[th] rate clock path. Timing diagram and time domain response of iPWM. Mathematical representation of the proposed iPWM with pre-cursor and post-cursor correction.

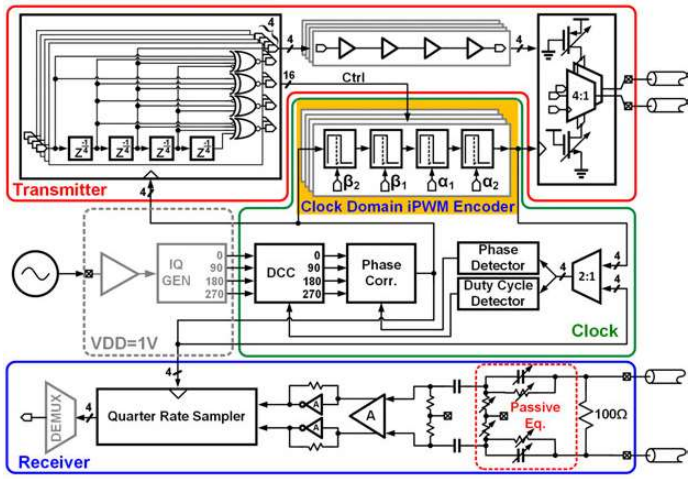

Figure 16.4.2: Block diagram of the proposed low-voltage transceiver with clock domain iPWM encoder.

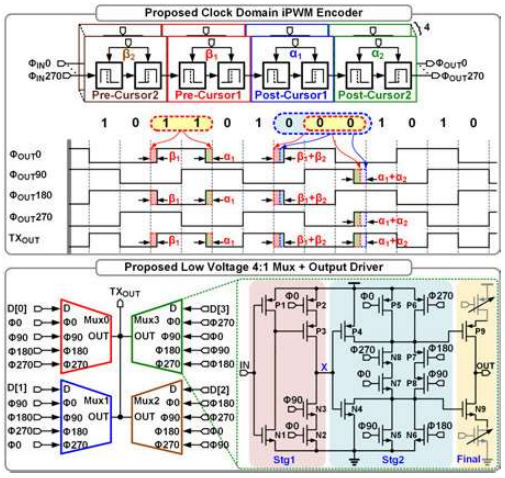

Figure 16.4.3: Block diagram of the proposed clock domain integrated pulse width modulation (iPWM) encoder and timing diagram in the presence of consecutive identical digits. Block diagram of the proposed low voltage 4:1 multiplexed 50Ω output driver.

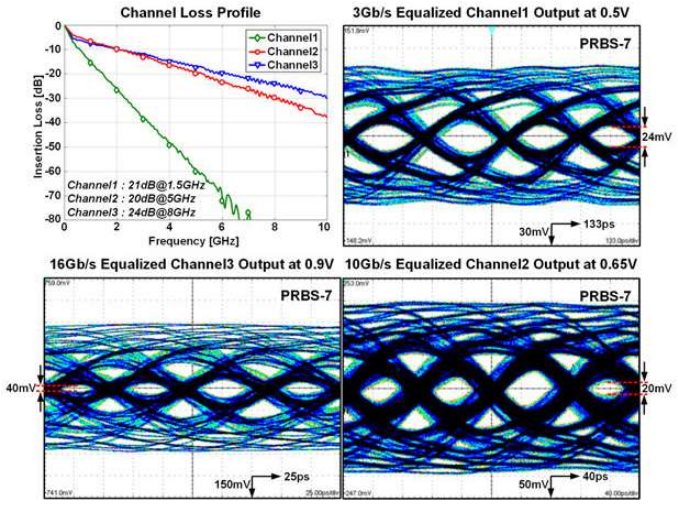

Figure 16.4.4: Measured insertion loss profiles of the channels. Equalized eye diagrams at the far-end channel outputs for 3Gb/s, 10Gb/s and 16Gb/s for 21dB, 20dB and 24dB loss, respectively.

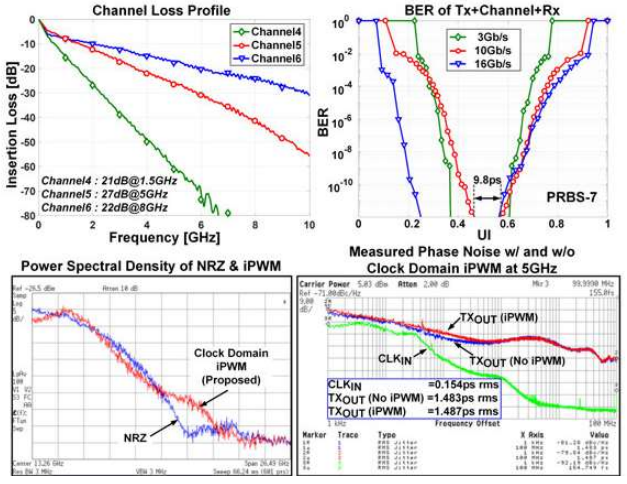

Figure 16.4.5: Measured insertion loss profiles of the channels. BER bathtub curves for the complete transceiver with equalized 3Gb/s, 10Gb/s, and 16Gb/s PRBS7 data. Measured power spectral density of NRZ and iPWM encoded data. Measured phase noise with and without clock-domain iPWM at 5GHz.

	This Work			Low Voltage Transceivers				Nominal Voltage Transceivers			
				ISSCC'15 [1]	VLSI'15 [2]	JSSC'13 [3]	VLSI'15 Shekhar	ISSCC'17 [4]		JSSC'11 Zhong	ISSCC'09 [5]
Technology [nm]	65	65	65	65	22	65	22	65	65	40	65
Supply [V]	0.5	0.65	0.9	0.7	0.75	0.65	0.7	0.9/1.0/1.1	1.0/1.1	1.1	1.0
Data rate [Gb/s]	3	10	16	6	8	6.4	5	16	16	14	8.9
Tx Equalization	iPWM (Clock)	iPWM (Clock)	iPWM (Clock)	None	2-tap FFE	None	2-tap FFE	iPWM (Data)	iPWM (Data)	4-tap FFE	None
Rx Equalization	Passive Eq.	Passive Eq.	Passive Eq.	None	None	CTLE	None	CTLE	CTLE	CTLE +10-tap DFE	DFE-IIR
Loss [dB]	21	27	22	N/A	12	8.4	8	19	27	26	19
Tx Power [mW]	1.74	6.17	18.94	1.86	0.32	1.92	3	45.1	45.5	102.5	11.6
Rx Power [mW]	1.82	4.93	11.44	1.02	0.25	1.07		12.2	24.4		5.4
Clk Power [mW]	1.37	6.87	19.84	0.66	0.22	0.038	7	-	-		-
Efficiency [pJ/bit]	1.65	1.8	3.14	0.59	0.79	0.47	2	3.58	4.37	7.3	1.91
Area [mm²]	0.13	0.13	0.13	0.15	-	0.057	0.041	0.21	0.21	0.97	0.023

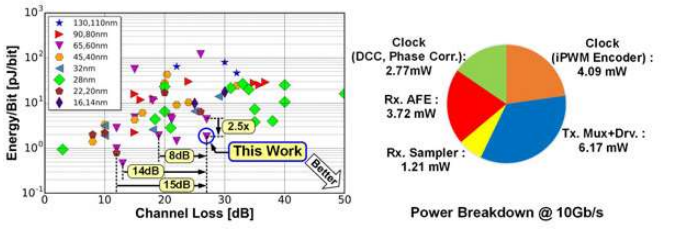

Figure 16.4.6: Performance summary and comparison with state-of-the-art designs.

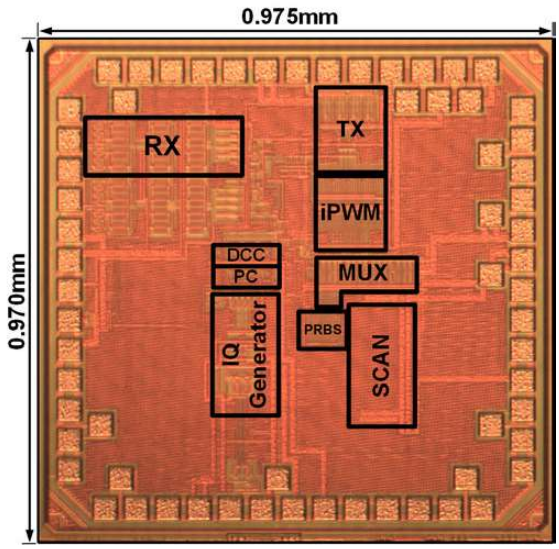

Figure 16.4.7: Die micrograph of the proposed transceiver.

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