

Line Coding Techniques for Channel Equalization: Integrated Pulse-Width Modulation and Consecutive Digit Chopping

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Abstract—This paper presents two new line-coding schemes, integrated pulse width modulation (iPWM) and consecutive digit chopping (CDC) for equalizing lossy wireline channels with the aim of achieving energy efficient wireline communication. The proposed technology friendly encoding schemes are able to overcome the fundamental limitations imposed by Manchester or pulse-width modulation encoding on high-speed wireline transceivers. A highly digital encoder architecture is leveraged to implement the proposed iPWM and CDC encoding. Energy-efficient operation of the proposed encoding is demonstrated on a high-speed wireline transceiver that can operate from 10 to 18 Gb/s. Fabricated in a 65-nm CMOS process, the transceiver operates with supply voltages of 0.9 V, 1 V, and 1.1 V. With the help of the proposed iPWM encoding, the transceiver can equalize over 27-dB of channel loss while operating at 16 Gb/s with an efficiency of 4.37 pJ/bit. The design occupies an active die area of 0.21 mm².

Index Terms—Line coding, transceiver, I/O, energy efficient, low power, serial link, phase-domain, equalization, serdes, wireline.

I. INTRODUCTION

GROWTH of online video content for high resolution (4k, 8k) video, and data generated by IoT devices has resulted in an exponential increase in the data rates at each and every point in the communication chain from data centers to smartphones. Wireline communication system addresses the bandwidth demand in two ways: (1) by increasing the number of channels and (2) by increasing the data rate per channel. Increasing the channels typically requires investment in new infrastructure, and is therefore discouraged. Consequently, increasing the data rates per channel has been the trend in wireline links over the last 16 years, as shown in Fig. 1(a) [1]. While the energy efficiency of these links has continued to improve, the efficiency improvement has slowed down in the last six years, as shown in Fig. 1(b).

A major reason for the slow down in energy efficiency improvement is the fact that, while data rates continue to

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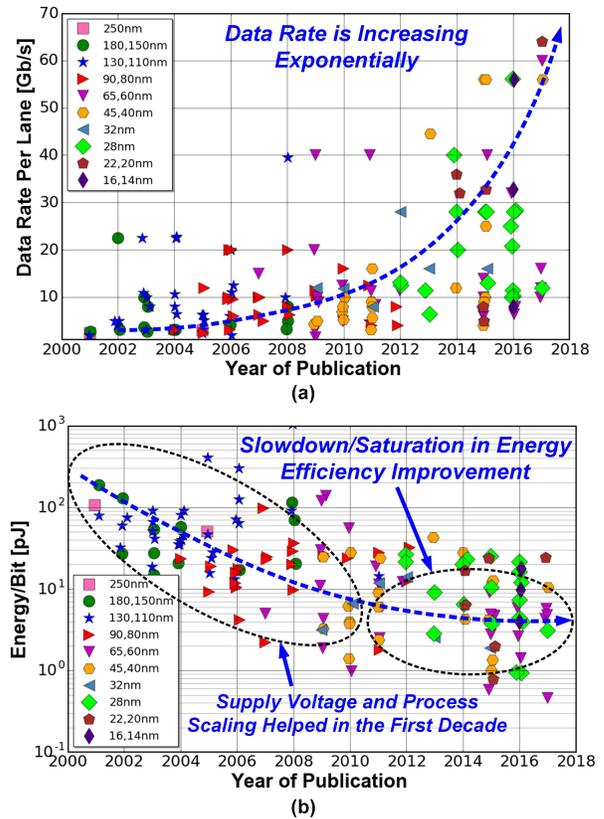


Fig. 1. (a) Data rate vs. year of wireline link publication. (b) Energy efficiency vs. year of publication [1].

increase, communication channels have remained more or less same since channel upgrades are very expensive. The same channel at higher data rates results in more inter-symbol-interference (ISI), which requires greater equalization to compensate the channel loss [2]. Equalization of the channel loss consumes significant power and degrades the energy efficiency of the wireline communication link.

Conventional equalization techniques on the receiver end such as decision feedback equalizers [3]–[5] have tight feedback timing constraints, which result in higher power consumption as the data rate increases. Feed forward equalization (FFE) on the transmitter with voltage mode driver avoids the feedback path and results in efficient equalization [6]–[8]. Based on the FFE tap resolution requirement, the output driver and pre-driver are divided into multiple segments. Although such a segmented FFE implementation helps to maintain a

constant output termination impedance (50Ω) across all tap settings, it comes at the cost of (a) increased signaling power, (b) increased switching power since multiple segments are required to achieve desired linearity [8], and (c) tight coupling between 50Ω termination tuning and FFE tap coefficients tuning. These three constraints reduce the FFE efficiency as the number of FFE taps are increased to equalize heavy channel loss.

Conventional line-coding techniques such as Manchester encoding [9] (also known as pulse width modulation or PWM), can equalize the wireline channel without increasing signaling power, without segmenting the output driver, and without coupling the 50Ω termination tuning with the coefficient tuning. However, PWM encoding requires the insertion of a precise narrow pulse in every data bit. These narrow pulses must be accurately reproduced at the transmitter output, which necessitates very wide bandwidth in the high-speed data path, resulting in poor energy efficiency [10], [11] and difficulty in scaling PWM encoding to higher data rates [12]. For example, creating a 10% duty cycle on a 64Gb/s PWM data stream would require a pulse width of 1.5ps with less than 1ps of rise/fall time at the transmitter output. Researchers have shown that phase pre-emphasis encoding scheme can help to reduce data dependent jitter [13]. However, it is ineffective at equalizing high-loss channels.

In view of these limitations, we propose two highly-digital phase-domain line-coding/modulation technique for equalization: (a) integrated pulse width modulation (iPWM) [14] and (b) consecutive digit chopping (CDC). The proposed iPWM technique can compensate more than 27dB of channel loss at 16Gb/s while consuming 69.9mW of power. Compared to the state-of-the-art PWM designs, the proposed iPWM scheme achieves $36\times$ better energy efficiency for the same data rate [11], and $3.2\times$ higher data rate for the same energy efficiency [12]. The proposed CDC encoding technique in tandem with iPWM, can equalize a channel loss of upto 30dB at 14Gb/s.

In the past, researches have also proposed digital phase modulation techniques such as pulse width modulation (PWM) [15]–[17] to encode the information in pulse widths instead of voltage levels (example: PAM-4/8/16). This work differentiates itself from the prior PWM based modulation research by the fact that the proposed work presents line-coding technique to equalize a wireline channel and it does not modulate the pulse width to encode information. In the proposed work, the information is contained in the two voltage levels only.

This paper is organized as follows. Section II introduces the proposed integrated pulse width modulation scheme, highlights its benefits, and compares it with the existing equalizing techniques. The concept of the proposed CDC encoding technique is discussed in Section III. Section IV describes the design and implementation of the proposed line-coding techniques in a wireline transceiver. Section V presents the measured results and Section VI summarizes observations based on the measured results. Finally, Section VII concludes this paper.

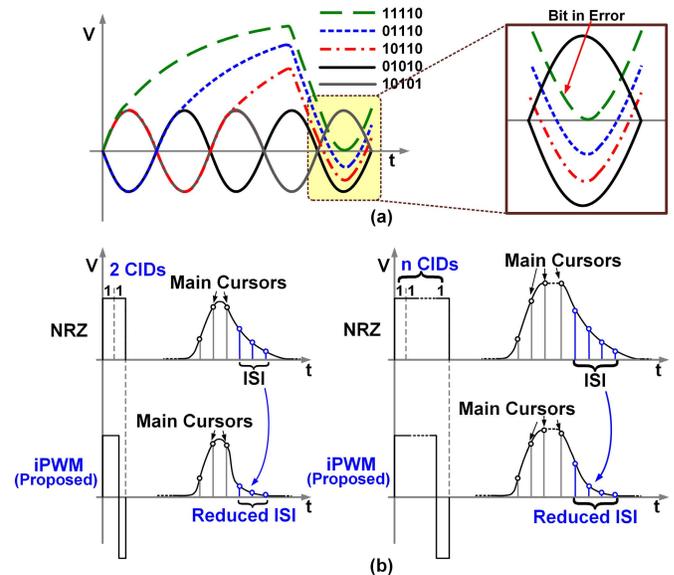


Fig. 2. (a) Effect of consecutive identical digits on inter-symbol-interference (ISI). (b) Time domain pulse response of NRZ data and proposed iPWM encoded data in the presence of CIDs.

II. CONCEPT OF THE PROPOSED iPWM

Wireline communication channels have low-pass characteristics. That is insertion loss of the channel increases with frequency. Let's say the data through the channel has 0 consecutive identical digits (CIDs), that is, the data is an alternating data (101010...), whose power spectrum is limited to just one frequency. With such data, the loss offered by the channel is constant and there is no ISI (no eye closure), as shown in Fig. 2(a). In reality, the transmitted data has consecutive identical digits (CIDs) such as 10110 (2 CIDs), 01110 (3 CIDs), 11110 (4 CIDs), etc, which causes the power spectral density of the data to have a wide bandwidth. Because of frequency dependent insertion loss of the channel, the loss offered to 4 CIDs is less as compared 3 CIDs or 2 CIDs because the majority of the power spectrum of data with 4 CIDs is located at a lower frequency as compared to the power spectrum of data with 3 CIDs and 2 CIDs. As a result, the data with 4 CIDs has a higher amplitude at the channel output than the data with 3 CIDs and 2 CIDs. Consequently, the transition time to a bit of opposite polarity immediately following the CIDs is higher for 4 CIDs as compared to 3 CIDs and 2 CIDs. The long transition time reduces the horizontal and vertical eye opening of the data bit immediately following the CIDs. Hence, due to the difference in the insertion loss offered to CIDs, the data bit immediately following the CIDs, suffers from inter-symbol-interference (see Fig. 2(a)).

The proposed iPWM operates on the fact that the ISI on the data bits following the CIDs can be reduced by reducing the pulse width of CIDs at the transmitter. The concept of reducing the pulse width is graphically explained in Fig. 2(b). In the proposed iPWM, instead of transmitting 2 UI (unit interval), 2 CIDs are transmitted for less than 2 UI. As a result, the transition to the bit of opposite polarity happen early, in other words,

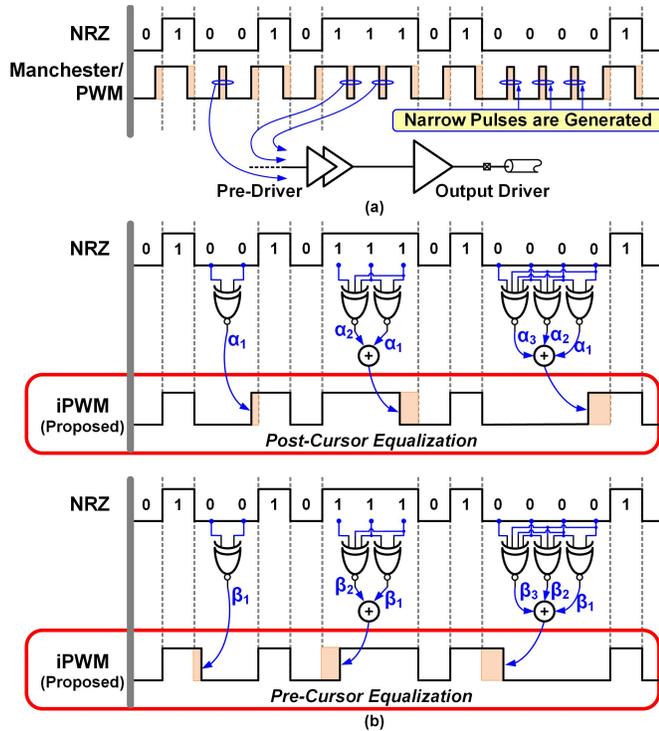


Fig. 3. (a) Manchester/PWM encoded data and problem of narrow pulse width generation. (b) Timing diagram of the proposed iPWM encoding for post-cursor and pre-cursor equalization.

the post-cursors generated by 2 CIDs is reduced, which helps to reduce the ISI. Similarly, this technique can be leveraged to remove ISI while transmitting 3 or more CIDs.

A. Benefits of iPWM Encoding

The timing diagram of the proposed iPWM encoding and comparison with the Manchester/PWM encoding is shown in Fig. 3. In case of Manchester encoding (Fig. 3(a)), bit one is represented by a signal, which stays high for 50% of the period and low for the remaining 50%. Bit zero is represented by a signal, which is low 50% of the period and then goes high. In PWM encoding, the time for which the signal stays high and low can be varied from 0% to 50% depending on the channel loss. In the presence of CIDs, the Manchester/PWM encoding generate narrow pulses, which must be transmitted through pre-driver and output driver to be precisely reproduced at the channel. These narrow pulses necessitate very wide bandwidth in the high-speed data path, resulting in poor energy efficiency and difficulty in scaling the Manchester/PWM encoding to higher data rates.

The proposed iPWM encoding avoids inserting narrow pulses and instead reduces the pulse width of CIDs to achieve equalization, as shown in Fig. 3(b). Post cursor ISI is reduced by reducing the trailing edges of CIDs, while the pre-cursor ISI can be reduced by reducing the leading edges of CIDs.

It can observe from Fig. 3(b) that the number of transitions in the iPWM encoded data is same as that of NRZ data, and therefore, the bandwidth requirement on the high-speed data path of the output driver, in case of the iPWM encoding

technique, is the same as that of the NRZ encoding. This helps in increasing the data rates of iPWM encoded data to 56Gb/s and beyond, without exponentially increasing the switching power of the transmitter.

Furthermore, conventional Manchester encoding technique has a lower limit on the minimum pulse width that can be transmitted because of the bandwidth limitation on the data path, which often results in over equalizing of a low-loss channel. When over equalization occurs, ISI is added instead of being subtracted, resulting in incorrect detection at the receiver, and consequently, higher bit error rate. The proposed iPWM encoding can change the pulse width of CIDs with very high precision (1ps precision or better can be easily achieved in 65nm CMOS), which helps to equalize a wide range of channel loss. Since iPWM encoding is done before the pre-driver, the output driver can be implemented as an unsegmented source series terminated driver. This reduces the signaling and switching power of the transmitter, which makes the proposed iPWM an energy efficient equalization scheme. Moreover, the proposed iPWM also helps to decouple the 50Ω termination tuning with the encoding coefficient tuning in source series terminated output driver.

In summary, the proposed iPWM (1) does not generate narrow pulses, (2) can equalize a wide range of loss, (3) reduces transmitter signaling and switching power, (4) decouples 50Ω termination resistor tuning from coefficient tuning, and (5) uses technology scalable encoding architecture.

B. Comparison with FFE and PWM

The equalization ability of the proposed iPWM encoding is compared with traditional FFE and Manchester/PWM encoding through simulations, as shown in Fig. 4. Simulations were performed at 16Gb/s on a channel with a loss of 19dB at 8GHz with PRBS7 data. The proposed iPWM achieves a horizontal eye opening of 47.4ps and a vertical eye opening of 119.2mVpp. Compared to conventional FFE, the horizontal eye opening of iPWM is 12% lower and vertical eye opening is 4% lower. Compared to the Manchester/PWM encoding, the horizontal eye opening of iPWM is 10% lower but the vertical eye opening is 2% higher. These results demonstrate that the proposed iPWM encoding achieves comparable eye openings as compared to the traditional equalization and encoding techniques.

C. Mathematical Representation of iPWM

The proposed iPWM encoded data can be mathematically expressed in terms of conditionally pulse-width modulated Heaviside step functions as shown below:

$$D_{iPWM}(t) = \sum_n b_n [u(t - nT - \sigma) - u(t - (n+1)T + \Delta)] \quad (1)$$

where b_n is the n^{th} data bit, Δ is the post-cursor pulse width reduction in time, and σ is the pre-cursor pulse width reduction in time. The Δ and σ can be mathematically expressed as

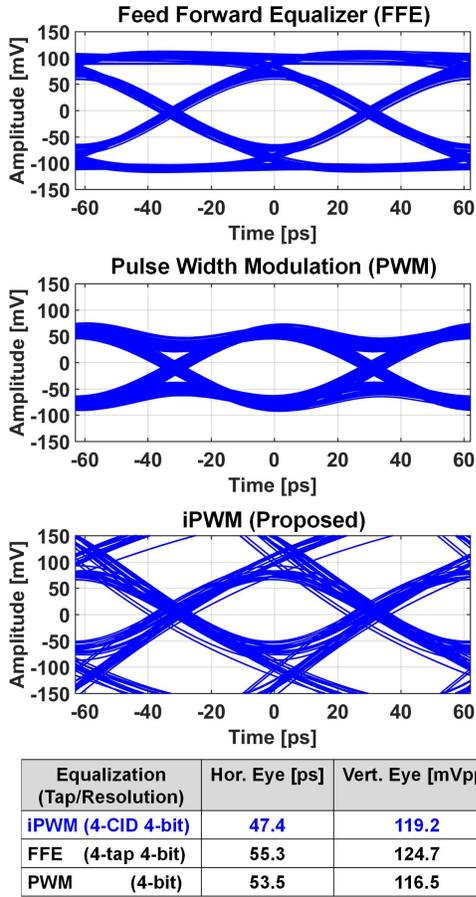


Fig. 4. Simulation results comparing feed forward equalizers (FFE), PWM and the proposed iPWM encoding.

follows:

$$\Delta = [b_n \oplus b_{n+1}] \times [\alpha_1 \times (b_n \odot b_{n-1}) + \alpha_2 \times (b_n \odot b_{n-1} \odot b_{n-2}) + \dots + \alpha_m \times (b_n \odot \dots b_{n-m})] \quad (2)$$

$$\sigma = [b_n \oplus b_{n-1}] \times [\beta_1 \times (b_n \odot b_{n+1}) + \beta_2 \times (b_n \odot b_{n+1} \odot b_{n+2}) + \dots + \beta_m \times (b_n \odot \dots b_{n+m})] \quad (3)$$

where m is the number of CIDs encoded, α and β are the post-cursor and pre-cursor scaling factors, respectively, such that $0 \leq \alpha_m \leq 1$ and $0 \leq \beta_m \leq 1$, \oplus is a logical XOR operation, and \odot is a logical XNOR operation. The encoding coefficients $\alpha_1, \alpha_2, \alpha_3, \dots$ and $\beta_1, \beta_2, \beta_3, \dots$ are functions of the communication channel and are estimated based on a given channel loss profile.

D. Effect of iPWM on Pulse Response

The effect of iPWM on ISI and comparison with FFE can be understood with a pulse response. For simplicity, the channel is represented as a single pole low-pass filter with a pole frequency of 'p' rads/sec. The channel frequency response can

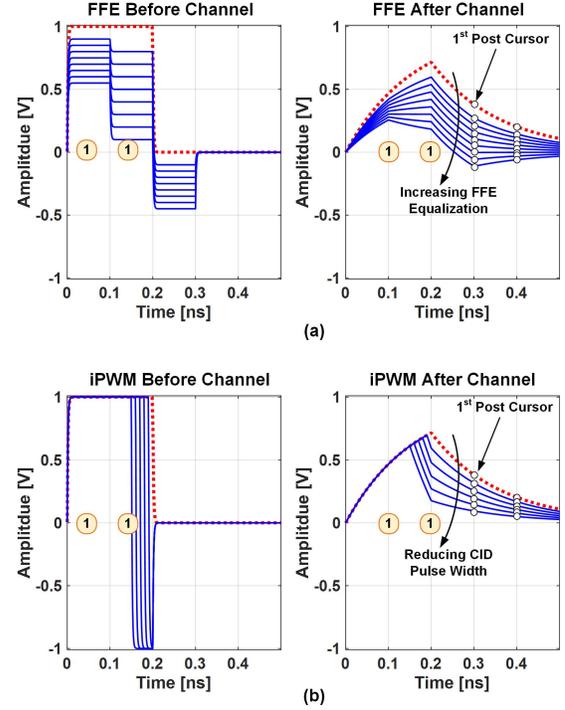


Fig. 5. (a) 2CID with 2-tap FFE before and after channel with increasing FFE tap coefficient. (b) iPWM encoded 2 CIDs before and after channel for increasing value of Δ .

be expressed as:

$$H(s) = \frac{1}{1 + s/p} \quad (4)$$

The channel response $h(t)$ can be expressed as:

$$h(t) = pe^{-pt} \quad (5)$$

A two-tap feed forward equalized NRZ in discrete time is written as $d[n] = a_1 \cdot x[n] + a_2 \cdot x[n-1]$, such that $|a_1| + |a_2| = 1$. In the continuous time domain, the output of the FFE with 2CID is written as:

$$d_{ffe}(t) = a_1\{u(t) - u(t-T)\} - a_2\{u(t-T) - u(t-2T)\} + a_1\{u(t-T) - u(t-2T)\} - a_2\{u(t-2T) - u(t-3T)\} \quad (6)$$

When FFE equalized 2CIDs is passed through this channel, the output of the channel $y(t) = d_{ffe}(t) * h(t)$, where $*$ denotes the convolution operation. A plot of FFE encoded data before and after the channel obtained by sweeping FFE coefficient a_2 is shown in Fig. 5(a). For these plots, the data rate is assumed to be 10Gb/s and pole frequency of the channel is assumed to be 1GHz. It can be observed that as the FFE coefficient a_2 is increased, the post cursor ISI is reduced.

Let an iPWM encoded data with 2CIDs (two ones followed by zeros) be represented as:

$$d_{ipwm}(t) = \{u(t) - u(t-2T + \Delta)\} - \{u(t-2T + \Delta) - u(t-2T)\} \quad (7)$$

For various values of Δ the iPWM encoded data is passed through the channel $h(t)$ and the output $y(t) = d_{ipwm}(t) * h(t)$ is

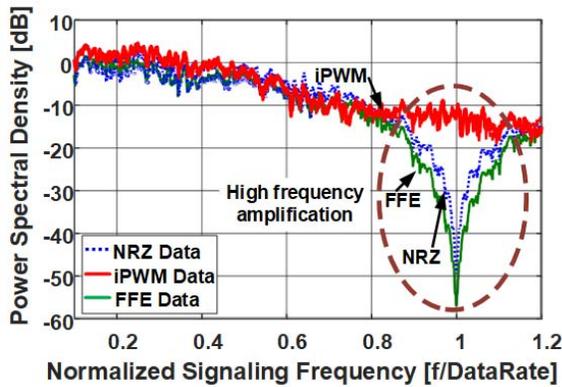


Fig. 6. Simulated power spectral density of NRZ, FFE and iPWM encoded data.

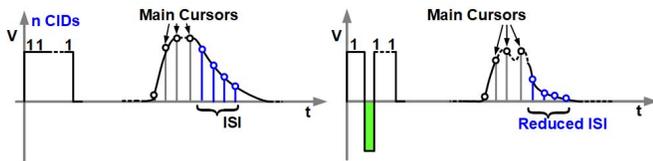


Fig. 7. Concept of the proposed consecutive digit chopping (CDC) encoding.

shown in Fig. 5(b). It can be observed that as the Δ increases, the post cursor ISI is reduced. This analysis demonstrates the mechanism with which iPWM can cancel ISI and achieve equalization.

E. Frequency Response of iPWM

The equalizing nature of the proposed encoding technique can be visualized from the power spectral density obtained from Matlab simulation of NRZ and 4-CID iPWM encoded PRBS13 data, as shown in Fig. 6. Compared to the NRZ encoded data, the proposed iPWM encoding technique has amplification in the high-frequency component of the power spectral density. This high-frequency amplification helps to compensate for the channel loss. The high-frequency amplification around $1/T_{UI}$ frequency (UI is the unit interval or time period of one bit) demonstrates the equalizing nature of the iPWM encoding. In the proposed iPWM encoding, the receiver does not need any decoder because the channel loss will attenuate the high-frequency component of the encoded data to bring it close to NRZ data pattern at the receiver input. Similar to the NRZ encoding, a sampler at the receiver is sufficient to recover the data.

III. CONCEPT OF THE PROPOSED CDC ENCODING

The concept of the proposed CDC encoding is shown in Fig. 7. The proposed CDC encoding is inspired by the magnetic recording systems, which introduced control transitions in the data stream to reduce the effect of pulse crowding [18]. In case of wireline communication systems, lower loss offered by the wireline channel to consecutive identical digits (111...) as compared to alternating data (1010...) is one of the major contributors to the inter-symbol-interference (ISI). Introducing

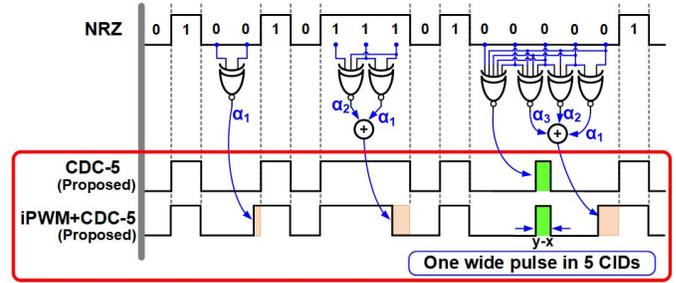


Fig. 8. Conceptual implementation of the proposed consecutive digit chopping (CDC) encoding.

a pulse of opposite polarity in the middle of CIDs introduces high-frequency component in the data stream, which helps to reduce the post-cursor ISI. The position and width of this pulse can be precisely controlled based on the channel loss profile. Compared to Manchester encoding, which requires insertion of multiple narrow pulses in a data stream, the proposed CDC encoding requires insertion of only one wide pulse in the data stream, which helps to relax the bandwidth requirement of the transmitter.

In the proposed encoding, a pulse of opposite polarity can be inserted in the data stream depending on the number of CIDs. For example, a pulse can be inserted in the presence 2 CIDs (we call it CDC-2), 3 CIDs (CDC-3) or N CIDs (CDC-N). The proposed CDC-N encoded data can be mathematically expressed in terms of conditionally pulse-width modulated Heaviside step functions as shown below:

$$D_{CDC-N}(t) = \sum_n b_n [u(t - nT) - u(t - (n + 1)T)] - \gamma b_n [u(t - nT - x) - u(t - nT - y)] \quad (8)$$

where b_n is the n^{th} data bit, γ is the logical condition for inserting pulse of width $y-x$ such that $\gamma \in \{0, 1\}$. The γ can be mathematically expressed as follows when N is odd (CDC-N):

$$\gamma = b_{n-\left(\frac{N-1}{2}\right)} \odot b_{n+1-\left(\frac{N-1}{2}\right)} \odot \dots \odot b_n \odot b_{n+1} \odot \dots \odot b_{n+\left(\frac{N-1}{2}\right)} \quad (9)$$

When N is even, the γ can be mathematically expressed as:

$$\gamma = b_{n-\left(\frac{N}{2}\right)} \odot b_{n+1-\left(\frac{N}{2}\right)} \odot \dots \odot b_n \odot b_{n+1} \odot \dots \odot b_{n+\left(\frac{N}{2}\right)} \quad (10)$$

where N is the number of CIDs encoded, \odot is a logical XNOR operation. The pulse width $x-y$ is a function of the communication channel and are estimated based on a given channel loss profile.

The iPWM encoding avoids narrow pulses and it equalizes the channel by modulating the edges of the CIDs. On the other hand CDC-N encoding equalizes the channel by inserting a wide pulse of opposite polarity in the middle of CIDs. Therefore, both these encoding techniques can be thought of as orthogonal encoding techniques, which are capable of equalizing the channel independently. Consequently, both iPWM and CDC-N encoding can be used together to equalize

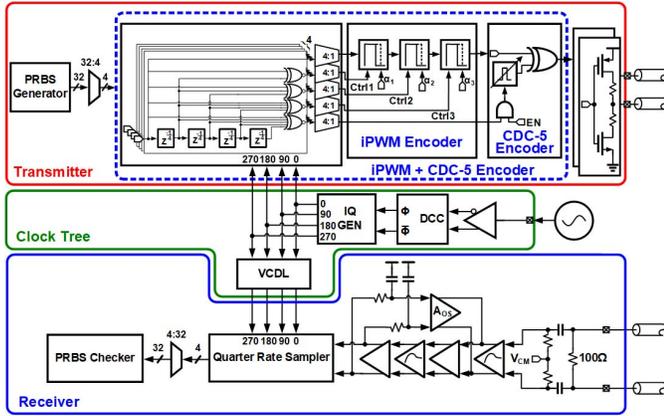


Fig. 9. Proposed iPWM based wireline transceiver architecture.

a channel with higher loss. To demonstrate the working of CDC-N encoding, in this work we present CDC-5 encoding, which introduce a pulse in the presence of 5 or more CIDs (CDC-5), as shown in Fig. 8. We also present how CDC-5 encoding together with iPWM can equalize a heavy channel loss.

IV. IMPLEMENTATION OF iPWM_CDC-5 WIRELINE TRANSCEIVER

The proposed iPWM and CDC-5 line-coding based equalization concept is validated by implementing it on a high-speed wireline transceiver. This section presents the implementation details.

A. Transceiver Architecture

The proposed transceiver architecture is shown in Fig. 9. The transceiver consists of a serializing transmitter, a deserializing receiver, and a clock tree. A high-frequency clock is provided externally to the chip, which is duty cycle corrected and then divided down into quarter-rate 4-phase clocks. This 4-phase clock is given to both the transmitter and the receiver. The transmitter consists of a 32-bit wide parallel PRBS generator, a 32:4 multiplexer, a 4-tap integrated pulse width modulator and CDC-5 encoder, and a source-series terminated output driver. The receiver consists of a continuous time linear equalizer (CTLE), amplifiers, quarter rate samplers, a 4:32 de-multiplexer, and a PRBS checker.

B. iPWM Encoder

The iPWM encoder is implemented in three steps. The first step is the detection of CIDs in the input bit stream, and it is achieved by the logic shown in Fig. 10(a). The XNOR logic is used to detect the presence of CIDs. Signals *Ctrl1*, *Ctrl2* and *Ctrl3* are asserted high in the presence of 2, 3 and 4 or more CIDs, respectively. These signals are subsequently used in the second step.

In the second step, the pulse width of CIDs is encoded based on the level of *Ctrl* signals, as shown in Fig. 10(b), with the associated timing diagram. When the *Ctrl* signal goes high, it limits the maximum output swing on the Dint node

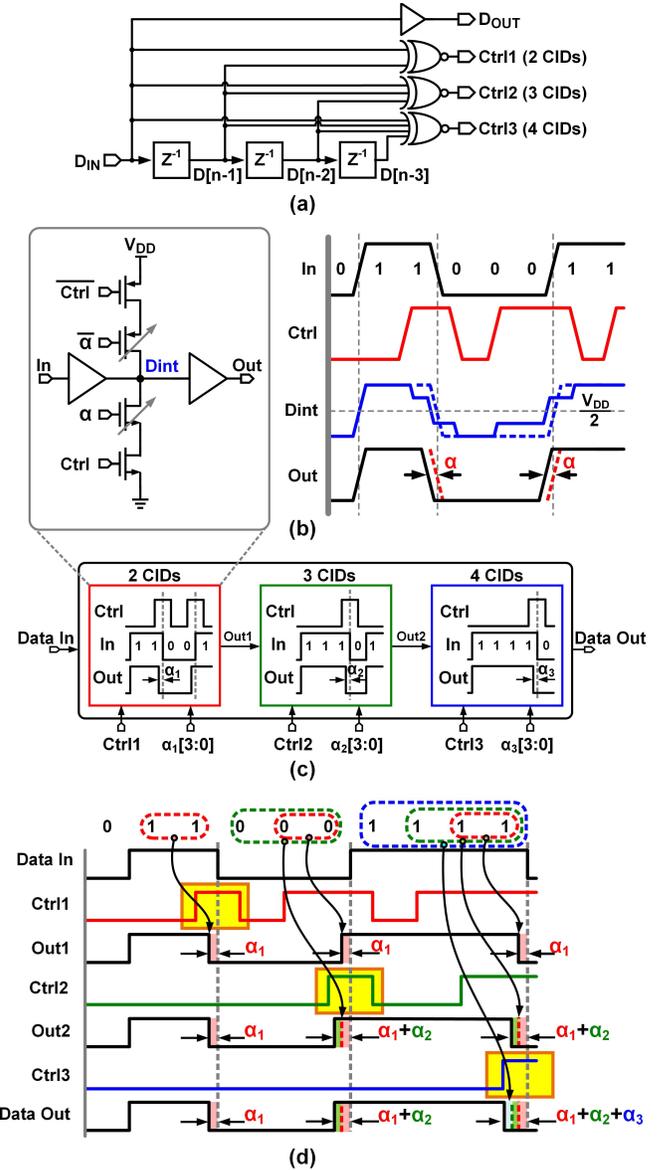


Fig. 10. (a) Logic for detecting consecutive identical digits in the data stream. (b) Pulse width encoder/modulator circuit implementation and timing diagram. (c) Cascading multiple iPWM encoders. (d) iPWM timing diagram.

by pulling it towards $V_{DD}/2$. For example, before transitioning from 1-to-0, the Dint node is loaded with the pull-down NMOS transistors and Dint starts to transition from $V_{DD} - \Delta V$ towards 0. Similarly, before transitioning from 0-to-1, the Dint node is loaded with the pull-up PMOS transistors and Dint starts to transition from ΔV towards V_{DD} . The lower swing on the Dint node reduces the time to transition from 1-to-0 ($V_{DD} - \Delta V \rightarrow 0$) and 0-to-1 ($\Delta V \rightarrow V_{DD}$), resulting in a reduced CID pulse width. The strength of the tunable transistors is controlled by encoding coefficient α , which helps to control the pulse width of CIDs (see Fig. 10(b)).

In the third step, the pulse width reduction of multiple CIDs is integrated. Integration is achieved by cascading multiple pulse width encoders, which successively reduce the pulse width of 2 CIDs, 3 CIDs, and 4 CIDs, as shown in Fig. 10(c).

The number of CIDs that can be encoded can be easily increased by cascading more pulse width encoders, which makes the proposed iPWM architecture highly scalable. Since only edges are encoded in the proposed iPWM, high encoding resolution can be achieved (3ps in our implementation). Moreover, a very large tuning range can be achieved by cascading multiple cells within an encoding coefficient α , allowing the proposed design to operate over a wide data-rate range (10-18Gb/s in this work).

The timing diagram in Fig. 10(d) illustrates the operation of the proposed iPWM. In the presence of 2 CIDs, the $Ctrl1$ signal is asserted high, and as a result, the pulse width of 2 or more CIDs is encoded with encoding coefficient α_1 . In the presence of 3 CIDs, both $Ctrl1$ and $Ctrl2$ signals are asserted high, which encodes the pulse width of 3 or more CIDs with encoding coefficient α_1 and α_2 . In the presence of 4 or more CIDs, all 3 signals, $Ctrl1$, $Ctrl2$ and $Ctrl3$ are asserted high. The pulse width of CIDs is first encoded by α_1 in the first stage, then by α_2 in the second stage and finally encoded by α_3 in the third stage. Consequently, the Data Out signal is encoded/modulated by an overall value of $\alpha_1 + \alpha_2 + \alpha_3$, thus achieving the integrated pulse width modulation (iPWM). In this work, as a proof of concept, the iPWM encoder is designed to equalize only the post-cursor ISI.

The sensitivity of the proposed encoder to voltage and temperature variation is estimated by performing the post layout simulations. With a supply voltage variation from 1.045V to 1.155V, the iPWM coefficient varies from -3.86% to $+3.33\%$. With a temperature variation from 0°C to 100°C the iPWM coefficient varies from $+6.49\%$ to -5.79% .

C. CDC-5 Encoder

The iPWM encoded data stream is further modulated by the proposed CDC-5 encoder, which inserts a pulse of inverted polarity in the presence of 5 or more CIDs. The position of the inserted pulse affects the pre and post-cursor ISI. The width of this pulse affects the amount of ISI correction. The block diagram of the proposed CDC-5 encoder and the associated timing diagram is shown in Fig. 11. The signal $Trig$ is generated in the presence of 5 or more CIDs in the bit stream. A voltage-controlled inverter delay chain is used to generate a pulse, triggered by the positive edge of the $Trig$ signal. The width of this pulse is controlled by $Vctrl$ signal. This short pulse is used to chop 5 consecutive bits in $DATA_{IN}$ to get $DATA_{OUT}$.

The sensitivity of the proposed encoder to voltage and temperature variation is estimated by performing the post layout simulations. With a supply voltage variation from 1.045V to 1.155V, the CDC pulse width varies from -7.66% to $+6.28\%$. With a temperature variation from 0°C to 100°C the CDC pulse width varies from $+3.07\%$ to -2.73% .

D. Receiver Front-End

The front-end of the proposed receiver architecture is shown in Fig. 12. It consists of a continuous-time linear equalizer (CTLE) interspersed with gain buffers. The CTLE

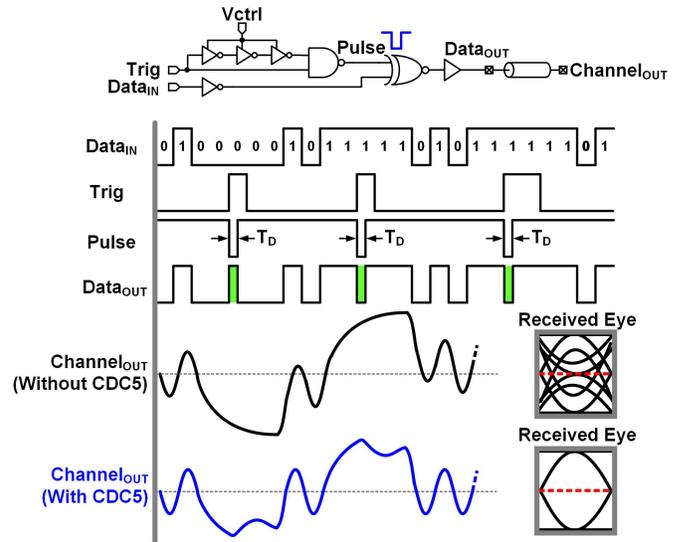


Fig. 11. Block diagram of the proposed consecutive digit chopping (CDC-5) encoder and timing diagram.

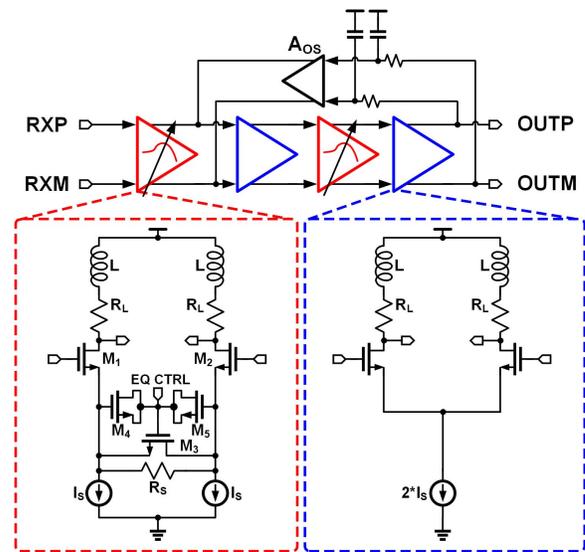


Fig. 12. Receiver front-end implementation.

provides a high-frequency boost by capacitive degeneration and the overall bandwidth is increased by inductive peaking achieved using 0.76nH of inductance. The amount of equalization is controlled by tuning MOS varactors (M_4 and M_5) and a variable resistor (M_3) [19]. The front-end also consists of a DC offset correction loop. Since the input data is DC balanced, in the absence of offset, the DC average of the output of the receiver front-end should be zero. DC offset detection is done by low pass filtering the differential output and the correction is done at the output of the first stage by applying a negative offset. According to simulations, the proposed receiver front-end achieves a maximum peaking of 6dB at a frequency of 12GHz when EQ_CTRL varies from 0.4V to 0V.

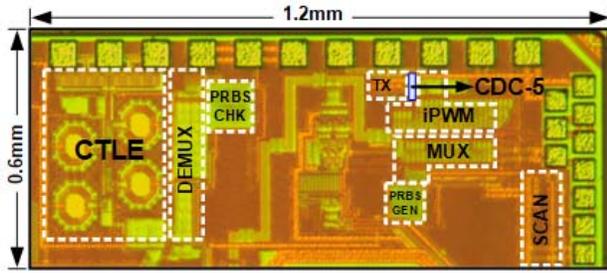


Fig. 13. Die micrograph of the proposed transceiver.

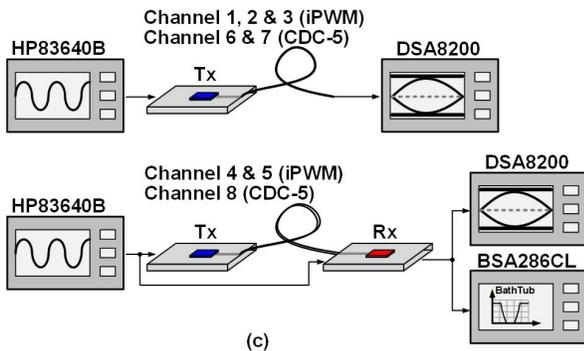
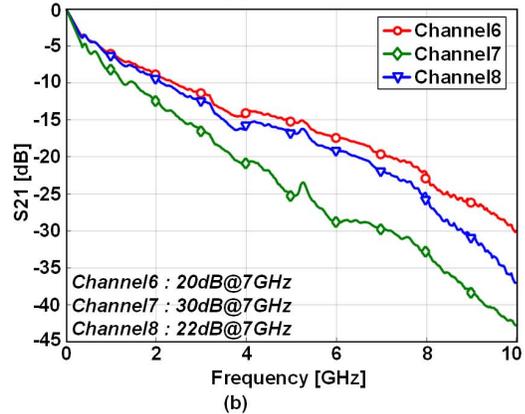
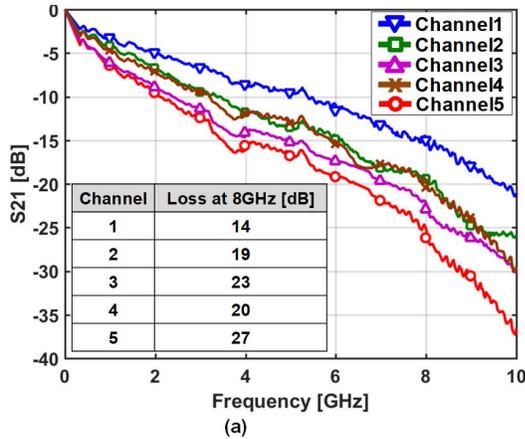


Fig. 14. (a) Loss profiles of channels used in iPWM measurements. (b) Loss profiles of channels used in iPWM+CDC-5 measurements. (c) Transmitter and transceiver measurement setup.

V. MEASUREMENT RESULTS

The proposed transceiver is fabricated in 65nm CMOS process and operates from a 0.9V/1.0/1.1V supply. The total active area of the proposed transceiver is 0.21mm², as shown

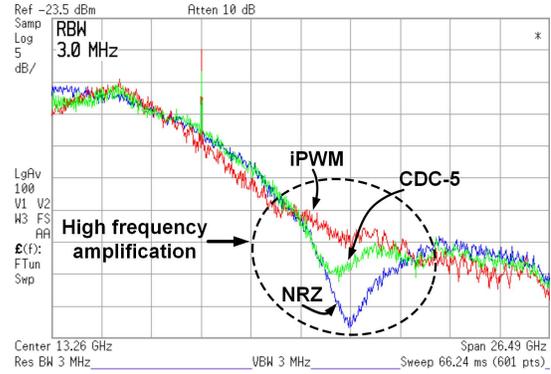


Fig. 15. Measured power spectral density of NRZ, iPWM and CDC-5.

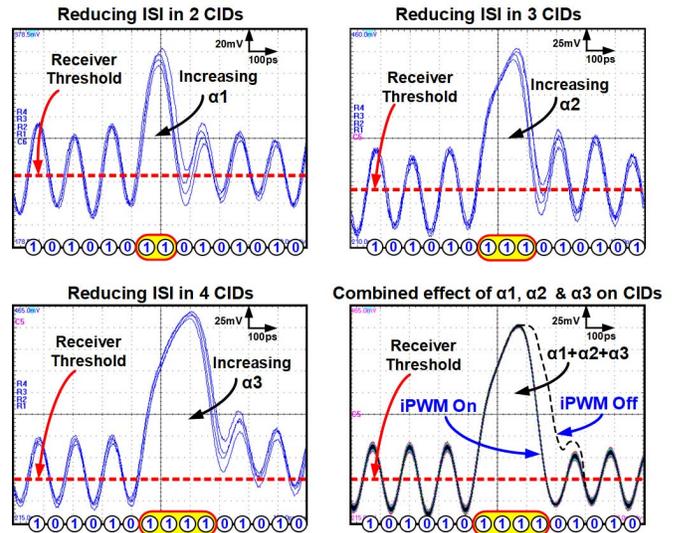


Fig. 16. Measured channel output demonstrating ISI reduction in the presence of CIDs as the iPWM is turned-on and coefficients are increased.

in the die micrograph in Fig. 13. Insertion loss profile of various channels used during the measurement is shown in Fig. 14(a) and (b). The channel loss at 8GHz ranges from 14dB to 27dB. The transmitter measurement and the transceiver measurement setup are shown in Fig. 14(c), respectively. An external clock source from HP83640B is used, which feeds clock directly to both the transmitter and the receiver. For the transmitter measurements, Channel-1, 2, 3 for iPWM and Channel-6, 7 for CDC-5 with different loss profiles are used and single-ended measurements are performed on an oscilloscope. For the transceiver measurement, the transmitter is connected to the receiver through three sets of channels, Channel-4, Channel-5 and Channel-8. The output of the receiver is measured on a bit error rate tester (BSA286CL) and an oscilloscope (DSA8200).

Equalizing nature of the proposed iPWM and CDC-5 in the frequency domain can be observed from the power spectral density measurement of NRZ, iPWM and CDC-5 encoded random data at 16Gb/s, as shown in Fig. 15. Encoding the data results in the high-frequency amplification near 16GHz, which shows the high-pass transfer characteristic of proposed iPWM and CDC-5 schemes.

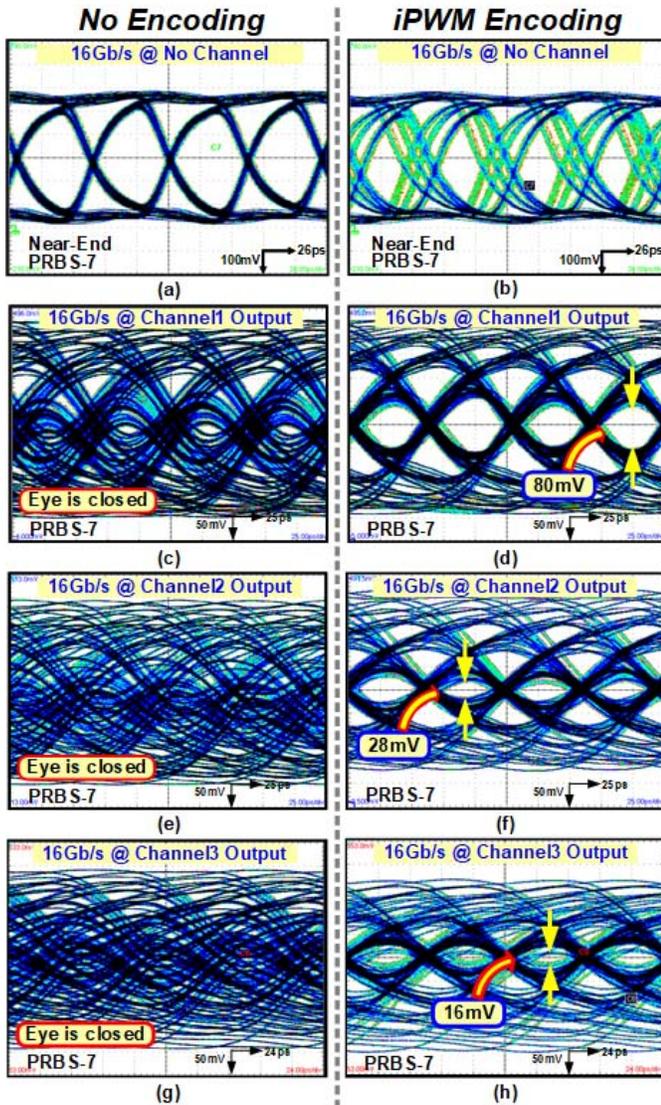


Fig. 17. Measured eye diagrams at 16Gb/s with PRBS-7 data: (a) Near-end NRZ. (b) Near-end iPWM encoded. (c) Channel-1 output NRZ (far-end). (d) Channel-1 output iPWM encoded (far-end). (e) Channel-2 output NRZ (far-end). (f) Channel-2 output iPWM encoded (far-end). (g) Channel-3 output NRZ (far-end). (h) Channel-3 output iPWM encoded (far-end).

A. iPWM Measurements

The effectiveness of the proposed iPWM encoding in the time domain is demonstrated by observing the effect of CIDs on ISI, with and without the proposed iPWM, as shown in Fig. 16. The red dotted line represents the receiver threshold. In the presence of 2 or more CIDs and in the absence of iPWM, the bits immediately following the CIDs are in error. As the encoding coefficients α_1 , α_2 and α_3 are increased, the pulse width of the CIDs decreases, which in-turn reduces the ISI, resulting in an improvement in both horizontal as well as vertical eye-opening of the bits following the CIDs.

The near-end and far-end single-ended measured eye diagrams without and with the proposed iPWM are shown in Fig. 17. The near-end eye diagrams of the NRZ PRBS-7

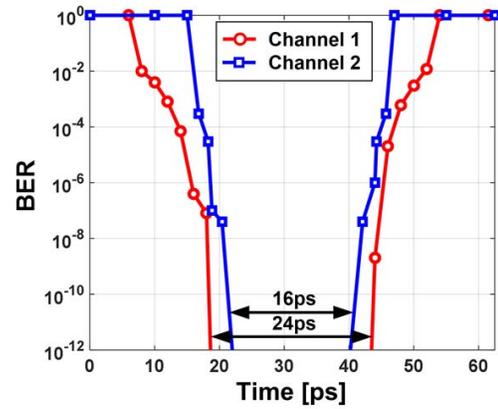


Fig. 18. Measured iPWM transmitter bathtub at 16Gb/s for Channel-1 and Channel-2 output.

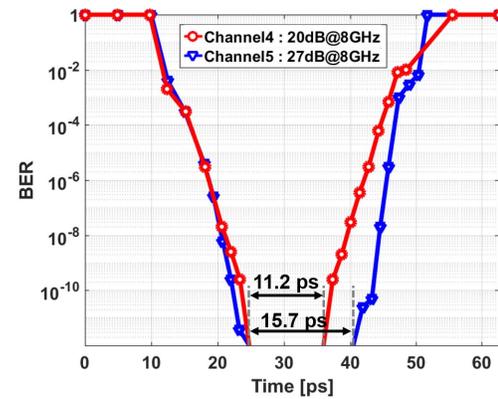


Fig. 19. Measured iPWM transceiver bathtub at 16Gb/s.

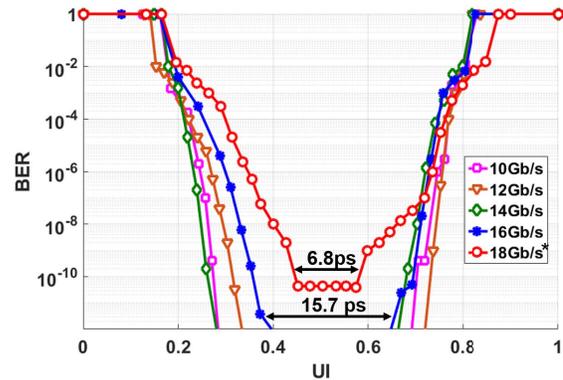


Fig. 20. Measured iPWM transceiver bathtub at 10Gb/s, 12Gb/s, 14Gb/s, 16Gb/s with Channel-5 and 18Gb/s with a lower loss channel.

data at 16Gb/s and encoded iPWM PRBS-7 data are shown in Fig. 17(a) and (b), respectively. The effect of pulse width reduction of the CIDs can be observed as distinct bands in the eye. In the presence of channel loss of 14dB, 19dB, and 23dB, the far-end eye of NRZ data is completely closed. After equalizing the data pattern with the proposed iPWM, the eye is open in all the 3 channels. Single-ended vertical eye openings in the case of Channel-1, Channel-2 and Channel-3 are 80mVpp, 28mVpp, and 16mVpp, as shown in Fig. 17(d), (f), and (h), respectively.

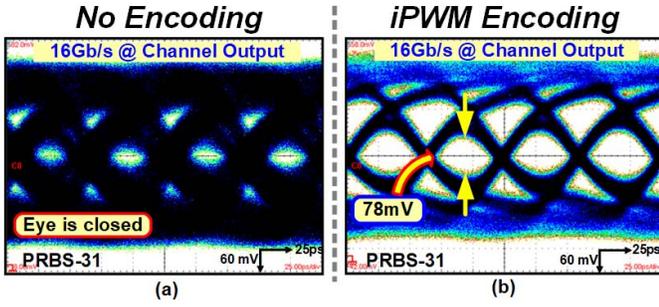


Fig. 21. Measured eye diagrams at 16Gb/s with PRBS-31 data and channel having 16dB loss at 8GHz: (a) Channel output NRZ. (b) Channel output iPWM encoded.

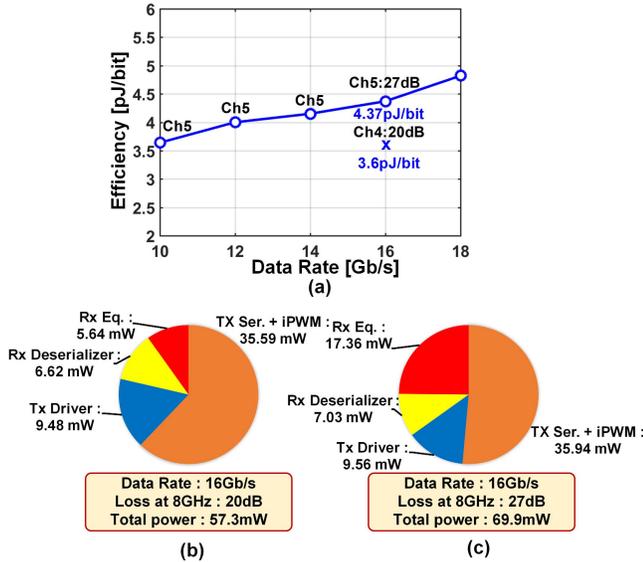


Fig. 22. (a) Measured iPWM energy efficiency vs data rate. (b) Measured iPWM transceiver power breakdown at 16Gb/s with 20dB loss. (c) Measured iPWM transceiver power breakdown at 16Gb/s with 27dB loss.

The BER bathtub curve for the transmitter at 16Gb/s is measured at the output of Channel-1 and Channel-2, which have an insertion loss of 14dB and 19dB at 8GHz, respectively, and the results are shown in Fig. 18. The horizontal eye openings at a BER of 10^{-12} are 24ps and 16ps for Channel-1 and Channel-2, respectively. The BER bathtub curve for the complete transceiver at 16Gb/s is measured at the output of Channel-4 and Channel-5, as shown in Fig. 19. The horizontal eye openings at a BER of 10^{-12} are 11.2ps and 15.7ps for Channel-4 and Channel-5, respectively. When the iPWM is disabled on the transmitter, the BERT could not achieve synchronization and the BER cannot be measured.

The scalability of the proposed iPWM implementation was demonstrated by measuring the BER bathtub of the complete transceiver using Channel-5 over multiple data rates, as shown in Fig. 20. The proposed transceiver was able to reliably operate from 10Gb/s to 18Gb/s. The 18Gb/s measurement was done using a low-loss channel (17dB @9GHz).

To test the effectiveness of the proposed iPWM with 4-CIDs on PRBS-31 data, measurement were done at 16Gb/s with and without the proposed iPWM encoding. The measured eye

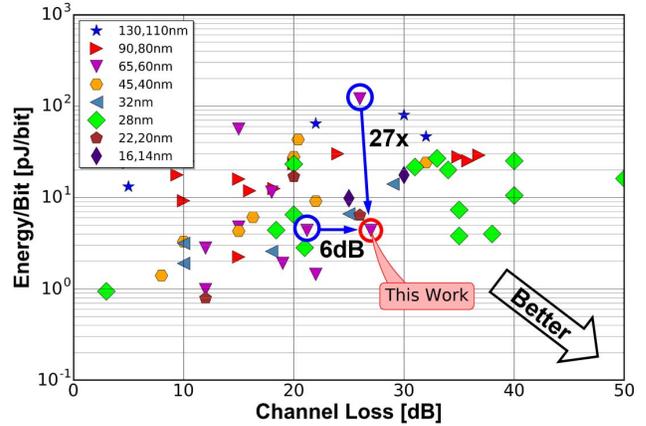


Fig. 23. Measured iPWM transceiver energy efficiency comparison with state-of-the-art transceivers.

diagram for the 16Gb/s PRBS-31 data at 16dB loss is shown in Fig. 21. It can be observed that without iPWM (NRZ alone), the eye is closed. The proposed iPWM opens the eye.

The measured energy efficiency of the transceiver across multiple data rates is shown in Fig. 22(a). The energy efficiency varies from 3.6pJ/bit at 10Gb/s to 4.3pJ/bit at 16Gb/s measured over Channel-5. At a lower loss of 20dB, the energy efficiency at 16Gb/s improves to 3.6pJ/bit.

Fig. 22(c) shows the transceiver power breakdown for two channel loss profiles. In the case of Channel-4 (loss of 20dB at 8GHz), the overall power consumption is 57.3mW while operating at 16Gb/s. The performance of the transceiver was improved further by using additional power in the receiver, to compensate a loss of 27dB. For compensating 27dB loss, the proposed transceiver consumed 69.9mW while operating at 16Gb/s. The proposed iPWM encoder causes insignificant addition to the noise of the transmitter. The phase noise of the transmitter output with 1010 data, in the presence and absence of iPWM, was measured. Without iPWM the phase noise is 0.163ps_{rms} and with iPWM enabled, the phase noise is 0.165ps_{rms} (integrated from 1kHz to 100MHz).

Table I shows the performance summary of the proposed transceiver and compares it with state-of-the-art transceiver designs. All of the compared designs consist of multi-tap FFEs and DFEs. While compensating a higher loss, the proposed iPWM based transceiver achieves better energy efficiency using 65nm technology and a higher mux-demux ratio (32:1).

A graphical comparison of the proposed iPWM transceiver with previously published state-of-the-art transceivers is shown in Fig. 23 [1]. Compared to prior-work in 65nm, for the similar loss, the proposed transceiver was able to achieve a 27× better efficiency [20] and at the similar efficiency, it was able to compensate 6dB higher loss [21].

B. CDC-5 and iPWM+CDC-5 Measurements

Due to bandwidth limitations of the CDC-5 encoding circuit, the transceiver measurements were made at 14Gb/s. The performance of the proposed CDC-5 encoding was measured using 3 different channels with loss profiles shown in Fig. 14(b).

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED IPWM TRANSCEIVER WITH STATE-OF-THE-ART DESIGNS

	This Work	This Work	ISSCC'14 [22]	JSSC'14 [4]	JSSC'11 [23]	JSSC'10 [21]
Technology [nm]	65	65	28	22	40	65
Data Rate [Gb/s]	16	16	20	4-32	1-14	20
TX Equalization	iPWM	iPWM	2-Tap FFE	3-Tap FFE	4-Tap FFE	3-Tap FFE
RX Equalization	CTLE	CTLE	CTLE + 2-Tap DFE	CTLE + 6-Tap DFE	CTLE + 10-Tap DFE	CTLE + 1-Tap DFE
Loss [dB]	20	27	20	24 [◊]	26 [†]	21.2
Mux-Demux Ratio	32:1	32:1	16:1	2:1	16:1	2:1
Power [mW]	57.3	69.9	130	73.6	102.5	87
Efficiency [pJ/bit]	3.58	4.37	6.5	4.6 [◊]	7.3 [†]	4.35
Supply[V]	0.9/1.0/1.1	1.0/1.1	0.9/1.35	0.9	1.1	1.2
Area[mm ²]	0.210	0.210	0.166	0.078	0.97 ⁺	0.070

◊ Reported for 16Gb/s data rate. † Reported for 14Gb/s data rate. + Includes PLL area.

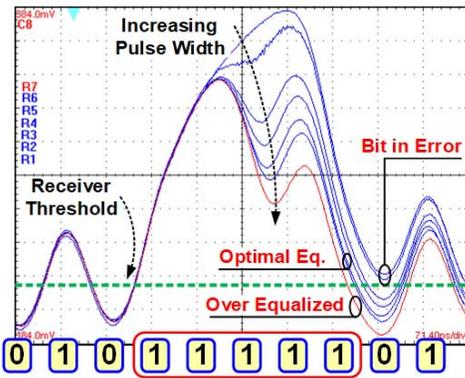


Fig. 24. Measured channel output demonstrating ISI reduction in the presence of CIDs as CDC-5 pulse width is increased.

The effectiveness of the CDC coding in the time domain is demonstrated by observing the effect of 5 CID's on ISI as the CDC-5 pulse width is increased, as shown in Fig. 24. The green dotted line shows the receiver threshold. Without CDC-5, the 0 bit adjacent to five 1s will be sampled incorrectly. As the pulse width is increased, the ISI starts to reduce. At an optimal pulse width, ISI in the bit adjacent to five consecutive 1s can be significantly corrected.

Figure 25 shows the measured far-end channel output with and without the proposed CDC encoding. In the case of Channel 7, with 30dB loss at 7GHz, the received eye at 14Gb/s is closed with iPWM encoding alone. The proposed CDC-5 + iPWM coding opens up the eye to 10mV_{pk-pk} (single ended).

Figure 26 shows the measured BER bathtub curve for the complete transceiver at 14Gb/s using Channel 8 with PRBS7 data. The horizontal eye opening with CDC-5+iPWM at a BER of 10⁻¹² improves from 34.8ps to 27.4ps. Fig. 27 shows the measured transceiver power and area breakdown. Operating at 14Gb/s, the proposed transceiver can compensate 22dB loss while consuming 64.3mW of power.

Table II shows the performance summary of the proposed CDC-5+iPWM, iPWM coding based transmitter and

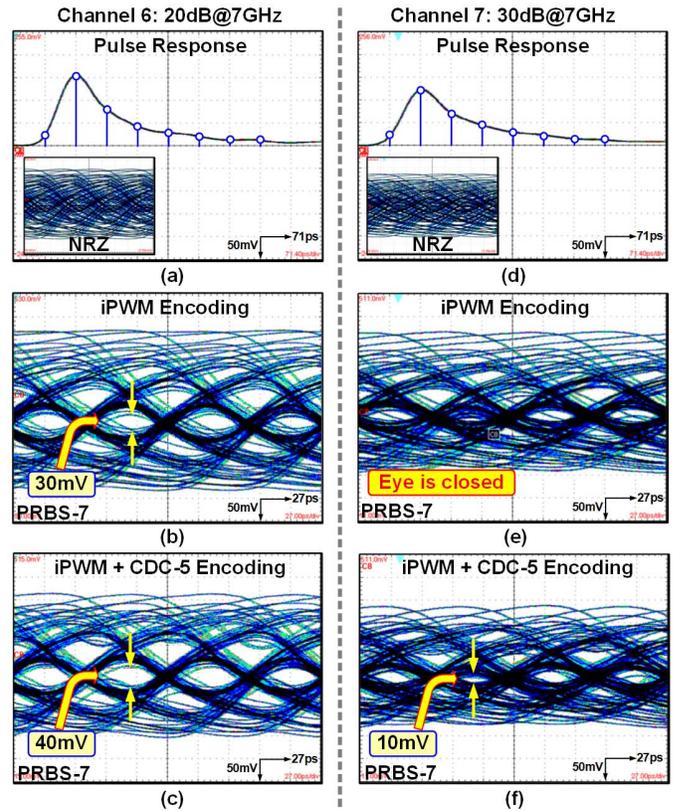


Fig. 25. (a) Measured impulse response of Channel 6 and NRZ eye (inset). (b) Received data with iPWM encoding at 14Gb/s. (c) Received data with CDC-5 + iPWM at 14Gb/s (d) Measured impulse response of Channel 7 and NRZ eye (inset). (e) Received data with iPWM encoding at 14Gb/s. (f) Received data with CDC-5 + iPWM at 14Gb/s.

compares it with the state-of-the-art encoding based equalizers. Compared to Manchester encoding (PWM), the proposed encoding achieves 34× better energy efficiency for similar channel loss and data rate [11], and 2.8× higher data rate for similar energy efficiency [12].

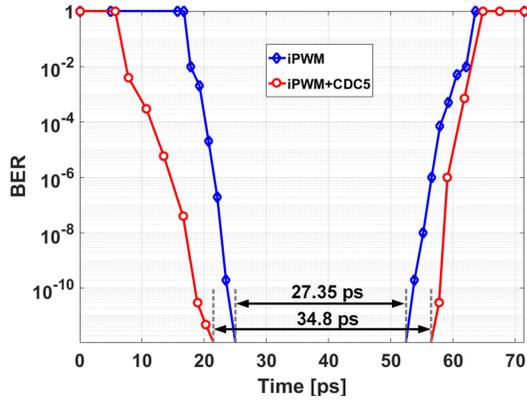


Fig. 26. Measured transceiver bathtub at 14Gb/s at the output of Channel 8.

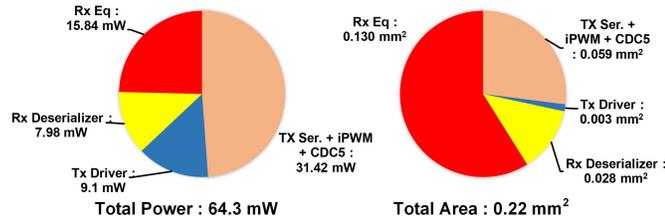


Fig. 27. Measured CDC-5+iPWM transceiver power and area breakdown at 14Gb/s with 22dB loss.

TABLE II

PERFORMANCE COMPARISON OF THE PROPOSED iPWM AND iPWM+CDC-5 TRANSMITTER WITH STATE-OF-THE-ART ENCODING BASED TRANSMITTERS

	This Work	This Work	JSSC'14 [12]	JSSC'06 [10]	CICC'08 [11]
Technology [nm]	65	65	90	90	130
Data Rate [Gb/s]	14	14	5	5	16
TX Encoding	iPWM +CDC-5	iPWM	PWM	PWM	PWM +PAM2
Loss [dB]	30	20	28	33	30
Horizontal Eye [UI]	0.3	0.32	0.3	0.75	0.25
Vertical Eye [mV]	10	30	8	15	30
TX Power [mW]	40.5	34.2	15.6	110	1578
TX Efficiency [pJ/bit]	2.89	2.44	3.1	22	98.6
Supply [V]	1.0	1.0	1.0/1.1/1.25	1.2	3.0/1.8

VI. OBSERVATIONS AND DISCUSSION

Based on the measured results, the following observations can be made regarding the two line-coding techniques.

- 1) The iPWM and CDC line-coding techniques are orthogonal and they have the capability to independently equalize a wireline channel.
- 2) When iPWM is used along with CDC coding, channel with higher loss can be equalized.
- 3) While iPWM+CDC-5 encoding helps to improve the horizontal eye opening by 7.4ps at 14Gb/s (BER 10^{-12}), it comes at a cost higher power consumption due to an additional 4:1 serializer and other high speed encoding logic in the transmitter.
- 4) The bandwidth requirement of inserting a wide pulse in CDC encoding limits the achievable data rate to be less than that achieved with iPWM encoding.

There are two factors that determine the optimal number of CID correction required in the proposed iPWM (a) channel

loss profile and (b) number of CIDs present in the data stream. These two factors are similar to the one used to determine the optimal number of taps in a feed forward equalizer (FFE). At higher channel loss (eg. >27 dB) and with long run-length of CIDs (eg. PRBS-31 data), we will need the iPWM to have more than 4-CID correction.

VII. CONCLUSION

This work introduces two new energy efficient line-coding schemes for equalization: integrated pulse width modulation (iPWM) and consecutive digit chopping (CDC). The proposed iPWM achieves eye openings, which are comparable to FFE and Manchester. A highly-digital encoder architecture is proposed to implement the iPWM and CDC scheme, which is scalable in nature and achieves wide-range high-resolution encoding coefficient tuning. A 10 to 18 Gb/s wireline transceiver implementation of the proposed scheme is demonstrated with measured results. The transceiver was capable of equalizing over 27dB of channel loss, while operating at 16 Gb/s, with an efficiency of 4.37pJ/bit.

The proposed line-coding techniques can co-exist and can also be employed along with other conventional equalization techniques such as CTLE (implemented in the receiver). In future, the proposed line-coding techniques can be further extended to operate with FFE and DFE based transceivers to make them backward compatible with existing receivers. While in this work, the proposed line-coding schemes were demonstrated to equalize a wireline channel, these coding techniques can be also be employed to equalize low bandwidth path in RF and optical communication systems.

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