Fully-Integrated 57 mV Cold Start of a Thermoelectric Energy Harvester using a Cross-Coupled Complementary Charge Pump

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***Abstract*—This paper presents a low-voltage cold-start architecture for battery-less thermoelectric energy harvesters that achieves fast start-up from an input voltage of 57 mV. The fully-integrated design uses a novel cross-coupled complementary charge pump with clocks generated using an ultra-low voltage ring oscillator to create a fast switching edge that assists in starting an inductive boost converter. The autonomous harvester implemented in a 180 nm CMOS process achieves start-up in 135 ms while consuming only 90 nJ of energy from the harvesting source to start the primary converter. This work demonstrates cold-start of a thermoelectric energy harvester at the lowest input voltage reported to date for a fully-integrated solution.**

I. Introduction

Thermoelectric energy harvesting is an intuitive approach for powering wearable devices, where the temperature difference between human skin and the ambient environment provides a constant source of energy. This small temperature gradient, however, generates only tens of millivolts using a thermoelectric generator, and a DC-DC boost converter is required to step up the source voltage to an output voltage level sufficient for powering integrated circuits. For true battery-less devices, the converter must self-start from the low-voltage output of the thermoelectric generator, presenting a significant challenge.

Several approaches have been recently demonstrated for autonomous cold start of thermoelectric harvesters. Mechanical switching with the assistance of vibrations from body movement [1] and off-chip transformers [2] can enable low-voltage start-up. To realize an integrated electrical start-up, a multi-stage charge pump can be used to boost the low-voltage input above the transistor threshold voltage before handing over to a high-efficiency inductive boost converter [3]–[7]. The start-up voltage is limited by the minimum input voltage required to generate clocks for the charge pump operation and inadequate output power of the charge-pump at this small input voltage to drive switches. LC oscillators with native transistors can generate clocks at lower supply, but require additional inductors [5], [6]. These can be eliminated using ring oscillators [3], [4], [7]; however, the ring oscillator in [4] requires post-fabrication tuning of V_{th} to achieve a cold-start at 95 mV, and Schmitt trigger inverter logic in [7] can't achieve cold-start below 70 mV. In all these fully integrated implementations conventional charge pump with ring oscillators makes the start-up process slower and restricted to 70 mV input voltage.

In this work, we present an integrated cold-start circuit architecture using an ultra-low-voltage ring oscillator, a cross-coupled complementary charge pump for enhanced drivability, and a low-power strobe generator to start up a downstream inductive boost converter. A fast start-up at an input voltage of 57 mV is achieved, which is the lowest fully-integrated cold start voltage reported to date. This approach enables autonomous cold start of thermoelectric energy harvesters from normal body temperature while minimizing the start-up energy, or 'joules to start'.

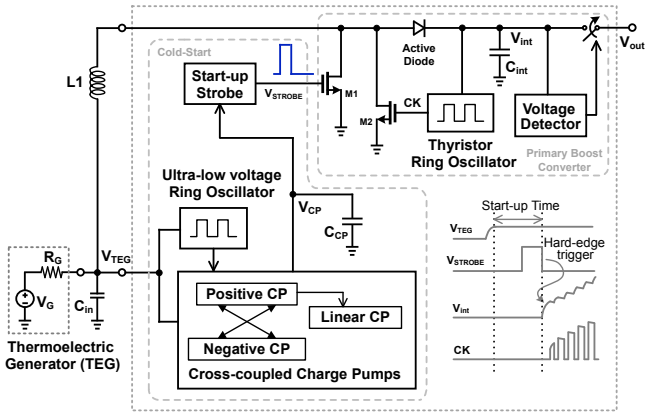

Fig. 1. Proposed circuit architecture for cold start of a thermoelectric energy harvester. The fully-integrated design provides the first, sharp switching edge needed to start the primary boost converter.

II. Proposed Cold Start Circuit Architecture

The proposed cold start architecture is illustrated as part of a larger thermoelectric energy harvester in Fig. 1. Instead of charging a large storage capacitor (>1 nF) as demonstrated in previous reported work [4], [7], a 120 pF capacitor (C_{CP}) is charged by a cross-coupled complementary charge pump with improved drivability. The charge pump clock is generated using an integrated ring oscillator designed with stacked-inverter delay elements that enable clock generation from a low voltage input. The boosted voltage output of the charge pump is used to generate a strobe pulse that drives the gate of M1. This strobe provides a sharp falling edge sufficient to kick-start the inductive boost converter and transfer energy to the output capacitor C_{int}. As soon as the energy transfer starts, a low-voltage thyristor-based ring oscillator (TRO) starts up to run the primary boost converter. Once the voltage across C_{int} crosses the threshold of the voltage detector, the final output V_{out} is enabled. The combined architecture enables low-voltage cold start and fast handover to the higher-efficiency inductive boost converter, thereby minimizing the energy consumed from the source for cold-start. Design of primary circuit blocks are discussed in the following sub-sections.

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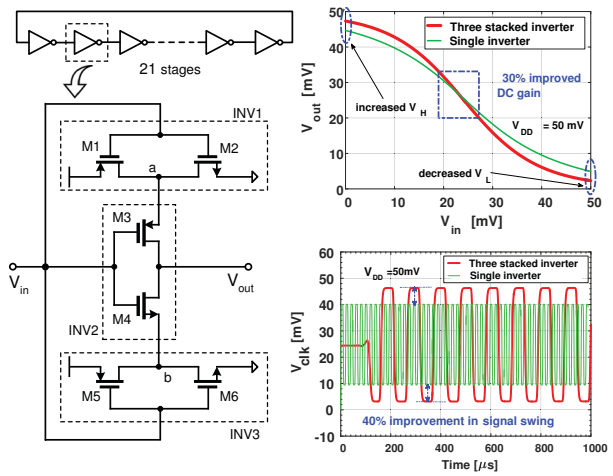


Fig. 3. Proposed ultra-low voltage ring oscillator using stacked-inverter delay stage. Higher stage gain enables oscillations at 50 mV supply and enhances swing.

A. Ultra-Low Voltage Ring Oscillator

Reduction of supply voltage reduces the DC gain of an inverter. At a voltage supply below 100 mV, the ratio of ON current i_{ON} to the OFF current i_{OFF} in an inverter is very low due to deep-sub-threshold transistor conduction. This results in flattening of the voltage transfer characteristics (VTC) of the inverter and low DC gain. Under this condition, a ring oscillator barely satisfies Barkhausen criteria of oscillation with a large number of stages and generates low clock frequency.

In order to improve the $i_{\text{on}}/i_{\text{off}}$ ratio of the ring oscillator delay stage, a stage element using three stacked inverters is used, as shown in Fig. 3. During charging (discharging) of output through M3 (M4) of INV2, the leakage current of M4 (M3) is minimized by the inverting action of INV3 (INV1); node b is pulled up by M5 when input is low and output is charging, which reduces drain-source voltage across M4 and reduces its leakage current. Similarly, node a is pulled down by M2, which reduces leakage current of M3 while discharging the output. This approach provides 30% improvement of DC gain compared to that of a single inverter at a supply of 50 mV, which is evident from the comparative VTC shown in Fig. 3. The improved $i_{\text{on}}/i_{\text{off}}$ ratio also enhances voltage swing of the output clock at a very low input supply. A 21-stage ring oscillator was implemented using stacked-inverter delay stages, providing a clock frequency of 9.25 kHz and 86% signal swing at 50 mV supply. A transient simulation of physical design with layout parasitics is shown in Fig. 3, which demonstrates 40% swing improvement using stacked-inverter stages. The ring oscillator fails to oscillate at a supply voltage below 40 mV.

B. Cross-Coupled Complementary Charge Pump

In a conventional Dickson charge pump, effective charge transfer through NMOS diodes is extremely small due to small $i_{\text{on}}/i_{\text{off}}$ ratio of the switch transistors at low input voltage [4]. To enhance charge transfer, gate-boosted or forward body-biased switches can be used [3], [6], [7], where voltage outputs from later stages are used to enhance switch conduction; these techniques improve output power of charge pump when the input voltage or clock swing is hundreds of millivolts. At sub-100 mV supply, voltage gain of each stage becomes so small that gate boosting from outputs of later stages is ineffective. Additionally, high switched-capacitor resistance (N/Cf), due to low clock frequency of the ring oscillator leads to high output resistance of an N-stage charge pump. As a result the open-circuit output voltage of the charge pump drops, providing only picowatts of power and impeding start-up. A larger stage capacitor can reduce the N/Cf resistance, but efficient boosting of switch gate voltage is still needed, which dominates the output resistance at this low voltage input.

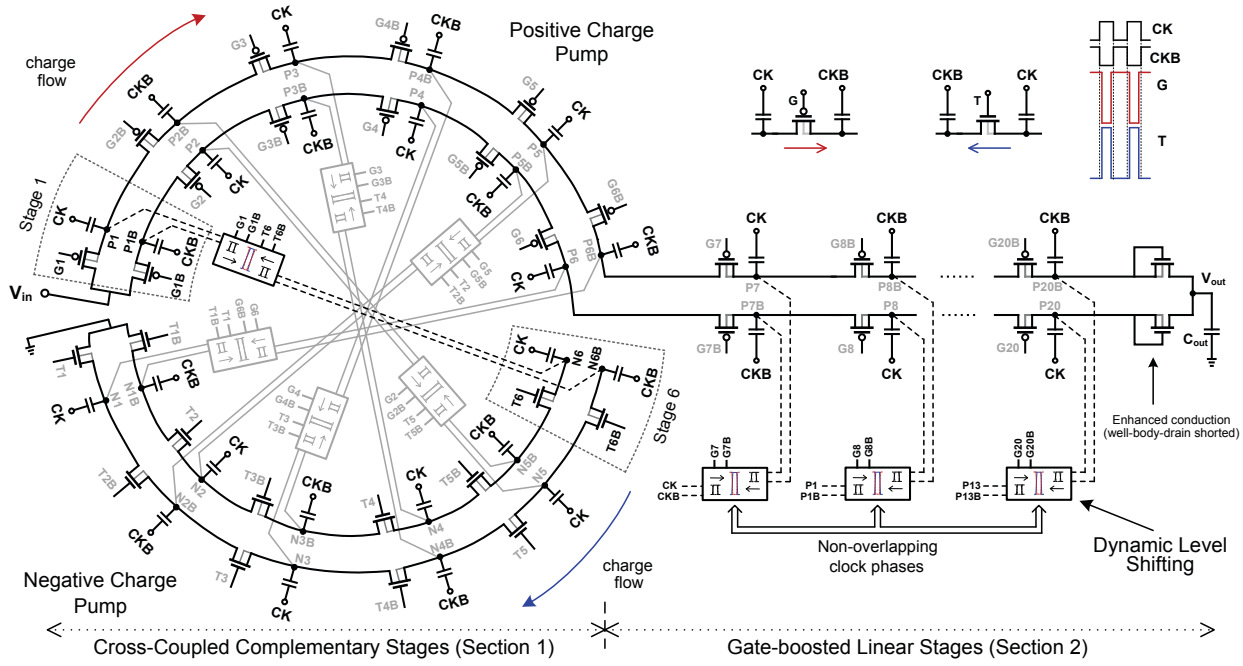


Fig. 2. Sub-100 mV charge pump architecture. Cross-coupled gate boosting using complementary charge pumps enhances conduction in Section 1. Boosted gate drive of later stages in Section 2 is achieved using outputs of preceding stages.

In the proposed charge pump gate boosting of switches is done with outputs of preceding stages. The charge pump consists of two sections as shown in Fig. 2. The first section comprises six-stage complementary dual phase charge pumps. The positive charge pump boosts the gate drive of the NMOS switches of the negative charge pump; the negative charge pump boost the gate drive of the PMOS switches of the positive charge pump. As illustrated in the figure for one pair of stages: dual phase outputs of the 1st stage of the positive charge pump, P1 and P1B, together with that of the 6th stage of the negative charge pump, N6 and N6B, are coupled together using a dynamic level-shifting circuit to generate boosted gate signals G1, G1B and T6, T6B for the PMOS and NMOS switches of the respective charge pump stages. The gate signal G1 (G1B) swings between high level of P1 (P1B) and low level of N6 (N6B) to enhances PMOS switch conduction. The gate signal T6 (T6B) swings between similar levels to increase the gate drive of the NMOS switch.

In a similar fashion, complementary outputs of the 2nd stage of positive charge pump is coupled with that of 5th stage of the negative charge pump, and so on, to create boosted gate drive for all stages (Fig. 2). Six stages are chosen for cross-coupling to create a boosted gate drive near threshold for the medium-V_t transistors used as switches. The cross-coupled complementary charge pumps enhance the switch conductivity, resulting in better charge transfer at low input voltage level compared with gate boosting from downstream stages in a single charge pump.

Careful design of dynamic level-shifting is required, as overlapped phases of gate drive signals will result in reverse charge flow. Four non-overlapping clock phases are generated using NAND gates and inverters, implemented with similar leakage mitigation to the stacked-inverter (Fig. 3) to operate at sub-100 mV supply. These clock phases, together with level-shifters and dynamic inverters, generate non-overlapping gate boosting signals as shown in Fig. 4. Triple-well MOS transistors are used in these circuits, as well as in the charge pump, to support both positive and negative voltages. Well and body of NMOS and PMOS transistors are connected properly to ensure reverse-bias of junctions in all conditions.

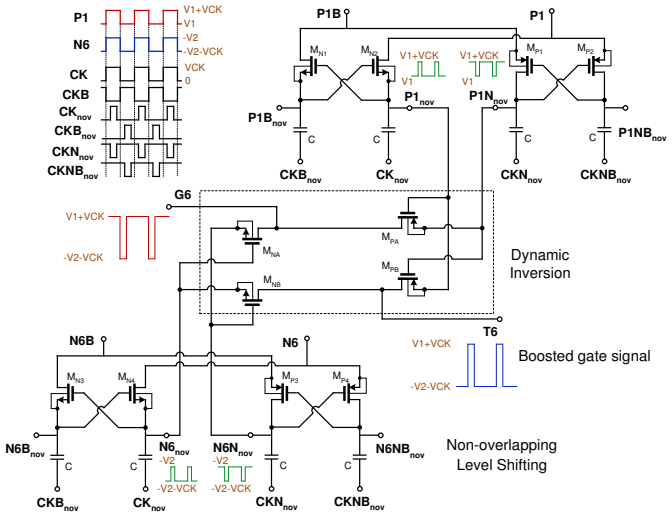


Fig. 4. Non-overlapping level-shifting and generation of boosted gate signals using dynamic inverters.

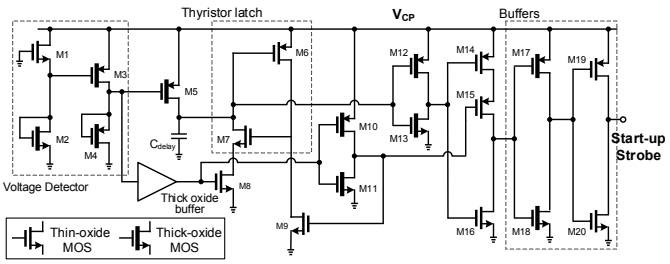


Fig. 5. Low-power, fast switching strobe generating circuit to start up the primary boost converter.

The second section of the start-up charge pump comprises a 14-stage linear positive dual-phase charge pump with PMOS switches, which uses positive outputs from the preceding stages to increase the gate drive voltage. As shown in Fig. 2, for enhanced overdrive of switches of the nth stage, complementary outputs of (n-7)th stages are used for gate boosting using dynamic level-shifting. Effective stage capacitance is 20 pF to reduce the N/Cf resistance. The final stage uses diode-connected NMOS transistors to avoid reverse charge flow when transient load currents create a drop in V_{CP}.

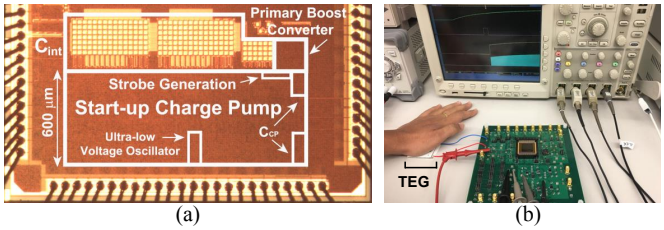
C. Strobe Generation for Starting Primary Boost Converter

A strobe pulse finally starts the primary boost converter. The falling edge of the strobe must be sharp enough to create sufficient inductive overshoot to turn on the active diode. Large inverters have high crowbar current that consume most of the output power of the charge pump. Instead, a thyristor-based latch circuit generates a pre-defined pulse width for the strobe, as shown in Fig. 5. An ultra-low power threshold detector is used to trigger the falling edge. Thick-oxide devices are used in intermediate buffers to minimize crowbar current, and final strobe pulse is driven with a regular-V_t inverter.

III. Test Setup & Measurements

The harvester was fabricated in a 0.18 μm CMOS process. The cold start circuit occupies 600 µm × 1600 µm, and the active area including the primary boost converter is 1.6 mm^2. The die micrograph and test set-up is shown in Fig. 6.

Measured output power of the charge pump with 55 mV input voltage is 3.5 nW at an output voltage of 720 mV (Fig. 7(b)). The charge pump draws a current of about 8 µA from the input. An 220 µH inductor is used for the primary boost converter. As shown in Fig. 7(c), cold start of the inductive boost converter is achieved with an input voltage of 57 mV within 135 ms. For these measurements, a source resistance of 4Ω is connected in series to replicate thermoelectric generator source impedance. A 1 µF capacitor is placed at the



(a) (b)

Fig. 6. (a) Die micrograph. (b) Measurement setup.

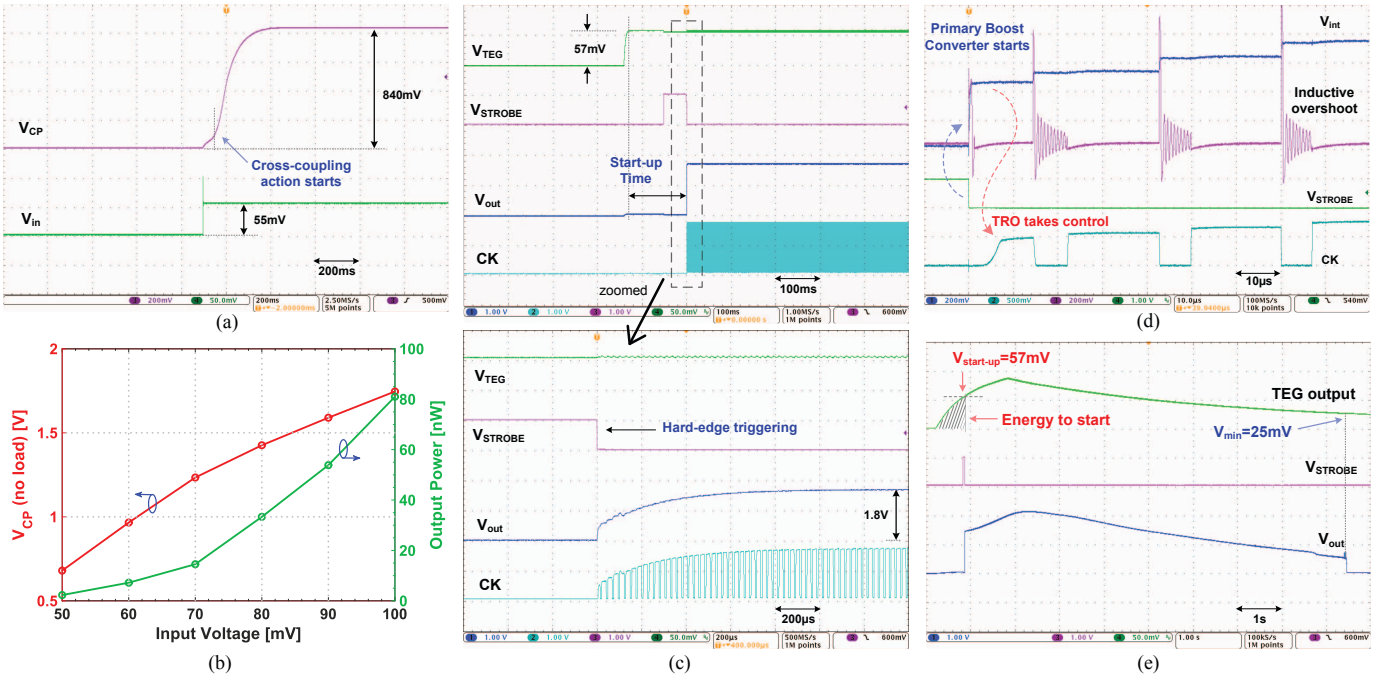


Fig. 7. Measured results: (a) Transient behavior of charge pump output with no load when V_{in}=55 mV. (b) Variation of open circuit output voltage and output power of charge pump with input voltage. (c) Full system functionality shows minimum voltage start-up. (d) Measurements show TRO can start at <500 mV. (e) Once started, the inductive boost converter can operate upto a minimum input voltage of 25 mV.

input to limit voltage ripple. The boost converter steps-up an input voltage of 57 mV to a 1.8 V unregulated output, and the maximum efficiency of the converter is nearly 20% at this small input. Fig. 7(d) shows that the TRO can start with a supply below 500 mV, which enables immediate hand-off to the primary boost converter following the cold-start strobe.

Measurement with a commercial Peltier-based thermoelectric generator (Marlow TG12-6-01L), shown in Fig. 7(e), validates the low-voltage cold-start of the complete energy harvester, and a minimum voltage of 25 mV keeps the boost converter operational once started. For this generator, 57 mV output corresponds to ΔT of about 1.6°C across the device. The start-up circuit consumes 90 nJ of energy to start, which is calculated by integrating the power over the shaded area in Fig. 7(e). The performance of the proposed cold start architecture is compared against state-of-the-art in Table I.

TABLE I. COMPARISON TABLE

Reference	Process	Start-up mechanism	Integration	Start-up voltage	Start-up time
ISSCC '10 [1]	0.35 µm	Mechanical	Off-chip	35 mV	-
ISSCC '11 [4]	65 nm	Ring osc. / CP	On-chip*	95 mV	262 ms
VLSI '12 [5]	65 nm	LC osc. / CP	Off-chip inductor	50 mV	-
ESSCIRC '15 [7]	0.13 µm	Ring osc. / CP	On-chip	70 mV	1.5 s
VLSI '15 [6]	65 nm	LC osc. / CP	On-chip	65 mV	-
This work	**0.18 µm**	**Ring osc. / CP**	**On-chip**	**57 mV**	**135 ms**

∗ Post fabrication tuning is required
CP - Charge Pump

IV. CONCLUSION

We have demonstrated a new approach for cold-start of thermoelectric harvesters using a low-voltage charge pump with integrated ring oscillators. The fabricated 0.18 µm CMOS test chip demonstrates start-up at an input voltage of 57 mV, representing the lowest cold-start voltage for a fully-integrated thermoelectric energy harvester reported to date. This approach can be extended to make high-efficiency, single-inductor autonomous thermoelectric energy harvesters.

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