

A Burst-Mode Digital Receiver With Programmable Input Jitter Filtering for Energy Proportional Links

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Abstract—A full-rate burst-mode receiver that achieves fast on/off operation needed for energy-proportional links is presented. By injecting input data edges into the oscillator embedded in a classical Type-II digital clock and data recovery (CDR) circuit, the proposed receiver achieves instantaneous phase-locking and input jitter filtering simultaneously. In other words, the proposed CDR combines the advantages of conventional feed-forward and feedback architectures to achieve energy-proportional operation. By controlling the number of data edges injected into the oscillator, both the jitter transfer bandwidth and the jitter tolerance corner are accurately controlled. The feedback loop also corrects for any frequency error and helps improve CDR's immunity to oscillator frequency drift during the power-on and -off states. This also improves CDR's tolerance to consecutive identical digits present in the input data. Fabricated in a 90 nm CMOS process, the prototype receiver instantaneously locks onto the very first data edge and consumes 6.1 mW at 2.2 Gb/s. Owing to its short power-on time, the receiver's energy efficiency varies only from 2.77 pJ/bit to 3.87 pJ/bit when the effective data rate is varied from 0.44 Gb/s to 2.2 Gb/s. Input sensitivity of the receiver is 36 mV for a BER of 10^{-12} .

Index Terms—Burst-mode receiver, clock and data recovery, digital CDR, edge injection, gated VCO, jitter transfer, jitter tolerance, phase noise.

I. INTRODUCTION

BURST-MODE communication is most commonly used in point-to-multipoint fiber access systems such as passive optical networks (PON) [1]. More recently, burst-mode communication has also been employed to save energy in memory interfaces [2], [3]. Because of wide variation in work load patterns of most practical computing systems, chip-to-chip links operate with very bursty data and their full data transfer bandwidth is seldom utilized. As a result, conventional techniques that improve power efficiency at peak data rate (maximum bandwidth) such as those reported in [4] and [5] do not necessarily

help achieve low-energy operation. Instead, turning the links on and off in accordance with the burst data can help maintain constant energy efficiency across a wide range of data bandwidth requirements. This behavior is referred to as *energy proportional* operation [6]. The effectiveness of burst mode communication to achieve *energy proportionality* greatly depends on how quickly the links can be turned on and off. Ideally, zero exit latency in transitioning between on and off states is desirable as it results in *energy proportional* operation from near-zero data throughput to the peak data throughput. However, in practice, circuits employing low-bandwidth feedback loops, especially phase-locked loops (PLLs) and clock and data recovery circuits (CDRs) pose the biggest challenge in reducing the exit latencies to nanosecond level. In [7], the problem of lowering the lock time of PLLs was addressed, but those techniques cannot be applied to lowering CDR lock time. Hence, the focus of this paper is the design of a burst-mode receiver that: (a) recovers data within few bits and (b) achieves nanosecond scale exit latency needed for energy proportional operation.

The rest of the paper is organized as follows. Section II reviews prior art on burst-mode CDRs and highlights the drawbacks of previously reported CDRs. The proposed CDR that uses a combination of feed-forward periodic data injection and feedback phase tracking is presented in Section III. In Section IV, the impact of periodic injection on the noise performance of the proposed CDR is analyzed. Section V describes the detailed circuit implementation of key building blocks. The measured results are shown in Section VI, followed by a conclusion of this work in Section VII.

II. CONVENTIONAL BURST-MODE CDRS

Fig. 1 shows a classical PLL-based digital CDR architecture in which the frequency and phase of the voltage-controlled oscillator (VCO) are accurately controlled to track the phase of input data [8], [9]. Because of the feedback loop, input data jitter is filtered by the CDR's low-pass jitter transfer function. However, limited bandwidth of the CDR causes phase acquisition to be very sluggish, which results in a large lock time of more than a thousand UIs. In other words, CDRs using a feedback loop suffer from a coupled tradeoff between input jitter filtering and lock time. This tradeoff was alleviated by speeding up the PLL locking process with the use of a programmable divider and loop filter configuration [10]. However, this technique is inadequate for burst-mode CDR applications, as it still requires several hundred UIs to lock depending on the initial phase error. As

Manuscript received August 15, 2014; revised November 08, 2014; accepted December 29, 2014. Date of publication February 13, 2015; date of current version February 25, 2015. This paper was approved by Associate Editor Ken Suyama. This work was supported in part by Intel Labs University Research Office, Semiconductor Research Corporation under task ID: 1836.129, and by the National Science Foundation (NSF) under CAREER Award EECs-0954969.

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Digital Object Identifier 10.1109/JSSC.2015.2390613

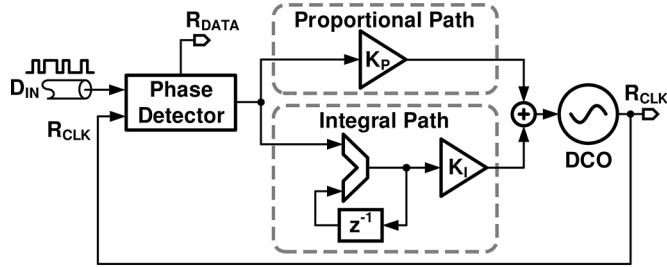


Fig. 1. Conventional phase tracking PLL-based CDR.

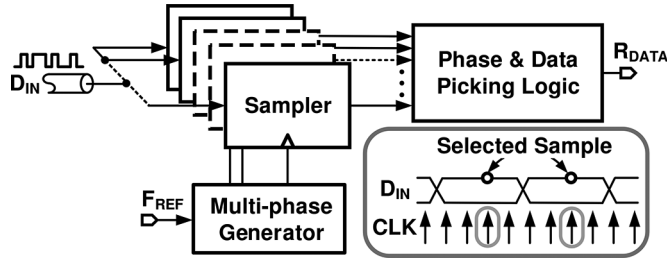


Fig. 2. Conventional blind oversampling CDR.

a result, the majority of burst-mode CDRs are based on feed-forward techniques.

One such feed-forward technique is blind oversampling, where data is recovered by sampling the input data (D_{IN}) several times (three or more) in a single UI using multiple phases of an asynchronous local clock, as illustrated in Fig. 2 [11]. By using oversampled data, bit boundaries are continuously estimated and the data sample farthest away from the boundary is considered the recovered data bit. The primary advantage of such CDR is its small lock time because of its feed-forward operation. However, it suffers from several disadvantages. First, multiple high-speed samplers and the digital data detection logic consume significant power, which severely degrades the CDR's power efficiency [12]. Second, achieving high jitter tolerance mandates increasing the oversampling ratio, which further deteriorates the power efficiency [11]. The need for closely spaced multiple phases also makes this architecture not suitable at high data rates. Finally, unlike the PLL-based CDR, the oversampled CDR architecture does not usually provide a recovered clock.

The gated-VCO (GVCO)-based CDR, shown in Fig. 3(a), provides a recovered clock and can also achieve fast locking [13], [14]. Compared to an oversampling CDR, the GVCO-based CDR consumes less power and occupies smaller area. Assuming GVCO frequency is equal to the data rate, instantaneous phase locking is achieved by aligning the GVCO phase with that of the input data by gating the GVCO edge with the data transition edge. Note that there is no actual phase locking between data and recovered clock in GVCO-based CDRs, but it is common to define *lock time* as the time taken to achieve error-free operation. In the presence of any frequency difference, phase error between the GVCO and input data accumulates, but it is reset every time a data edge is injected into the GVCO. However, in the presence of a large number of consecutive identical digits (CIDs) during which there are no input data transitions, the accumulated phase error exceeds 1/2 UI

and causes a bit error. In other words, frequency offset degrades CDR's tolerance to CIDs. To alleviate this, GVCO frequency is controlled by using a replica VCO that is embedded in a PLL as shown in Fig. 3(a). Assuming the GVCO and its replica are matched, the GVCO frequency is set within a few hundred parts per million (ppm) of the incoming data rate. However, the effectiveness of this replica biasing approach is limited by two factors: (a) mismatch between the GVCO and its replica VCO and (b) accuracy of the PLL reference clock frequency. The mismatch issue can be alleviated by directly setting the GVCO frequency as shown in Fig. 3(b) [15]. In this case, the frequency error is governed by the accuracy of reference clock frequency, which still limits CDR's tolerance to CIDs. Another important disadvantage of the GVCO-based CDR is that it cannot reject input jitter because of its feed-forward operation and hence exhibits an all-pass jitter transfer characteristic, which is undesirable in many applications. In view of these drawbacks, we present a digital burst-mode CDR that combines the advantages of feedback and feed-forward architectures. The proposed CDR achieves programmable input jitter filtering, instantaneous phase-locking and improved tolerance to CIDs by using a phase tracking feedback loop along with a GVCO in which only a controlled number of data edges are injected.

III. PROPOSED CDR ARCHITECTURE

The block diagram of the proposed fast power-on full-rate burst-mode receiver is shown in Fig. 4 [16]. It consists of a limiting amplifier, edge injection logic (EIL), and split-tuned digital CDR composed of a frequency-locking loop (FLL) and a Type-II digital PLL (DPLL). At initial start-up, the digital FLL drives the digitally controlled oscillator (DCO) frequency to within the pull-in range of the CDR. The FLL consists of a counter-based frequency detector (FD) and a 14-bit accumulator (ACC_F). After the FLL locks, both the data edge injection path and the DPLL are enabled. The DPLL employs a conventional architecture in which a bang-bang phase detector (BBPD) measures the sign of the phase error between the incoming data and the recovered clock. The BBPD output is decimated by a factor of 8 before it is fed to a 14 bit digital accumulator (ACC_I) that implements the integral control portion of the type-II response. Decimation lowers the operating speed and helps save power of digital circuits such as the accumulator and $\Delta\Sigma$ modulator. The second-order $\Delta\Sigma$ modulator truncates ACC_I output and drives the DCO using a simple current-mode digital-to-analog converter (DAC). An analog low-pass filter that is commonly used to suppress shaped truncation error of $\Delta\Sigma$ DACs is avoided because its low bandwidth increases frequency settling time. Instead, shaped noise is suppressed by leveraging the DPLL's loop bandwidth. Loop stabilizing proportional control is implemented by driving the DCO with BBPD output directly. This, as opposed to adding the proportional control in the digital loop filter, reduces loop delay and minimizes jitter caused by limit cycles [8].

In addition to the DPLL, the DCO is also controlled by the data-edge injection path to achieve fast locking. To this end, data transitions are detected by an edge detector and injected into the DCO much like in a conventional GVCO-based burst mode CDR [13], [15]. However, in contrast to [13], [15], where every

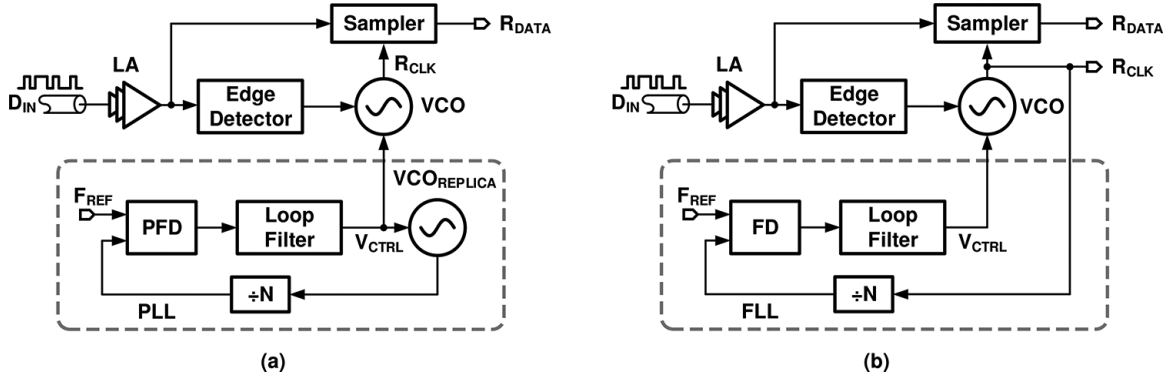


Fig. 3. Conventional GVCO-based burst-mode CDR: (a) with replica VCO [13], [14]; (b) without replica VCO [15].

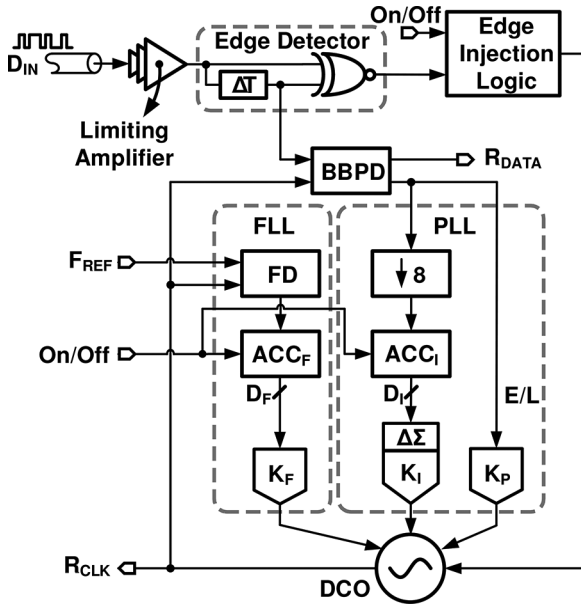


Fig. 4. Proposed fast power-on burst-mode receiver architecture.

data edge is injected into the DCO, only a limited number of data edges are injected in the proposed architecture. This selective edge injection in the proposed CDR is performed by the EIL, which measures the number of edges and controls the injection rate by injecting only a pre-determined number of data edges into the DCO. When the receiver enters off-state, EIL stops the DCO from oscillating, and accumulators in the FLL and integral path of the DPLL store the coarse and fine frequency control words, D_F and D_I , respectively. When the receiver is powered on, the DCO's frequency is accurately preset using D_F and D_I .

The proposed architecture offers two main advantages. (a) By virtue of using a single VCO, the mismatch issue that plagues conventional GVCO-based CDRs is mitigated. Furthermore, because the PLL locks DCO phase to input data, steady-state frequency error becomes zero, which improves immunity of the CDR to CIDs. (b) Selective injection of data edges ensures fast locking and helps control the jitter transfer (JTRAN) bandwidth. As will be shown in Section IV, injecting once every M data transitions causes the JTRAN bandwidth to scale in proportion to M . Intuitively, when $M = 1$, the proposed CDR simplifies to the GVCO-based architecture and

exhibits all-pass JTRAN characteristic. On the other hand, because there is no injection when $M = \infty$, JTRAN bandwidth is equal to that of the type-II DPLL. For values of M between one and infinity, JTRAN bandwidth scales with M . Note that phase-interpolator-based mixed-PLL/DLL architectures were reported for clock generation for controlling jitter transfer bandwidth in [17], [18] but it cannot be directly used in a CDR because of missing data transitions.

Another important aspect of the proposed architecture is that it can tolerate a larger amount of DCO frequency drift during the inactive time between data bursts. Voltage and temperature variations during the off-state cause the DCO frequency to drift and introduce a frequency error when the DCO is powered on with its preset control codes. This initial frequency error causes jitter accumulation and reduces timing margin during power-on transient. To quantify this effect, frequency tracking behavior of the proposed CDR and conventional PLL-based CDR is simulated in the presence of initial frequency error; the results are presented in Fig. 5. Note that conventional GVCO-based CDRs are not capable of correcting any frequency error and hence are not considered in this simulation. With an initial frequency error of 0.4% and PRBS31 input data, the PLL-based CDR exhibits a very nonlinear phase-locking response and takes nearly 3,000 ns to acquire lock, as illustrated in Fig. 5(a). Because of the use of a bang-bang phase detector, *half cycle slips* occur whenever the accumulated phase error exceeds π radians. This results in a bit error as shown in Fig. 5(b), and it also increases lock time. In contrast, data edge injection into the DCO resets the accumulated phase error and prevents the proposed architecture from cycle slipping. As a result, no bit errors occurred during the power-on transient and the lock time is nearly 3 times faster than that of the PLL-based CDR (see Fig. 5(a)). Thus, the proposed CDR exhibits better settling time and higher tolerance to DCO frequency drift during the off-state.

IV. ANALYSIS OF CDR JITTER FILTERING CHARACTERISTICS WITH PERIODIC DATA INJECTION

We now analyze the impact of periodic injection of the data edge on the jitter performance of the proposed CDR. By calculating autocorrelation of the random process describing the error in zero-crossing times of the recovered clock, we analyze the impact of input data edge injection on both the DCO and input phase noise filtering properties of the CDR.

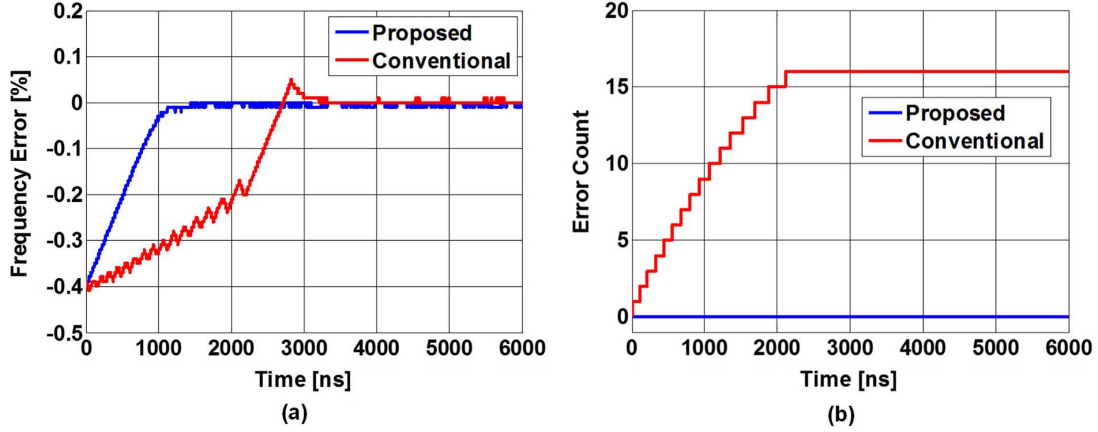


Fig. 5. Comparison between proposed CDR and conventional PLL-based CDR: (a) frequency-locking transient; (b) bit error response.

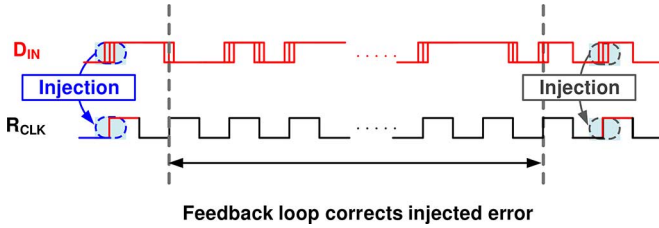


Fig. 6. Illustration of data edge injection and the impact of PLL feedback on R_{CLK} .

Before delving into mathematical analysis, we make the following observations. When the data edge is injected into the oscillator, input jitter at that instant is transferred to the recovered clock, as illustrated in Fig. 6. Because not every data edge is injected only the down-sampled input phase noise gets injected into the DCO. In the duration between data edge injections, the CDR acts as a conventional type-II PLL and suppresses the injected input phase noise. Hence, as the time between data injections increases, we expect the proposed CDR to behave much like a conventional PLL-based CDR. On the other hand, as the time between data injections decreases, the CDR's behavior approaches to that of a GVCO-based CDR. Note that injected input jitter remains in the recovered clock and is not filtered in a conventional GVCO-based CDR because of the absence of PLL feedback. As a result, the total phase noise power of the recovered clock is unaffected by the injection rate. These characteristics are derived mathematically in the following subsections.

A. Input Jitter Transfer Characteristics

We analyze input jitter transfer characteristics of the proposed CDR by first calculating DCO output noise power spectral density (PSD) in the presence of data injection and then apply jitter filtering provided by the PLL. To simplify the analysis, we derive closed-form expressions for *alternating data* and later scale the results with transition density to obtain the result for random input data. We also ignore intrinsic jitter of the DCO and only focus on the input jitter here. DCO phase noise shaping is addressed in the next section.

Let X denote the random process representing input jitter, i.e., zero-crossing timing error of the input data, where $X[i]$ is the error in zero-crossing time of the i th edge. We assume that

X is wide-sense stationary with zero mean and that its PSD is white. Therefore, its autocorrelation $R_X(i, j)$ is given by [19]

$$R_X(i, j) = E[X[i]X[j]] = \frac{\sigma_X^2}{2} \delta_{ij} = \begin{cases} \frac{\sigma_X^2}{2} & \text{if } i = j \\ 0 & \text{if } i \neq j \end{cases} \quad (1)$$

If every data edge is injected into the DCO like in a conventional GVCO-based CDR, the jitter sequence of the DCO output will be the same as the input data. This indicates, as expected, that the PSD of the DCO jitter is the same as input jitter, thus the input jitter transfer characteristic of a conventional GVCO-based CDR is all-pass. However, if only every N th edge is injected into the DCO, the data jitter remains in the DCO only until the next edge is injected and the DCO output jitter sequence, Y , will then be as follows:

$$Y = (X[1], X[1], \dots, X[1], X[N+1], \dots, X[N+1], X[2N+1], \dots, X[2N+1], X[3N+1], \dots) \quad (2)$$

Using (1), the autocorrelation function of Y , $R_Y(i, j)$, can be calculated to be:

$$\begin{aligned} R_Y(i, j) &= E[Y[i]Y[j]] \\ &= \begin{cases} \frac{\sigma_X^2}{2} & \text{if } -k \leq i - j < N - k \text{ and } j \equiv k + 1 \pmod{N} \\ 0 & \text{otherwise} \end{cases} \end{aligned} \quad (3)$$

where k is an integer from 0 to $N - 1$. Note that Y is cyclostationary and the PSD of Y , $S_Y(\omega)$ can be calculated by taking the Fourier transform of the average autocorrelation, $\bar{R}_Y(\tau)$, as follows:

$$\begin{aligned} \bar{R}_Y(\tau) &= \frac{1}{N} \sum_{j=0}^{N-1} R_Y(\tau, j) \\ &= \begin{cases} \frac{\sigma_X^2}{2} \frac{N-|\tau|}{N} & \text{if } |\tau| < N \\ 0 & \text{otherwise} \end{cases} \end{aligned} \quad (4)$$

$$\begin{aligned} S_Y(\omega) &= \sum_{\tau=-\infty}^{\infty} e^{-j\omega\tau} \bar{R}_Y(\tau) \\ &= \frac{\sigma_X^2}{2} \sum_{k=0}^{N-1} \frac{\sin(\omega k + \frac{\omega}{2})}{\sin(\frac{\omega}{2})} \end{aligned} \quad (5)$$

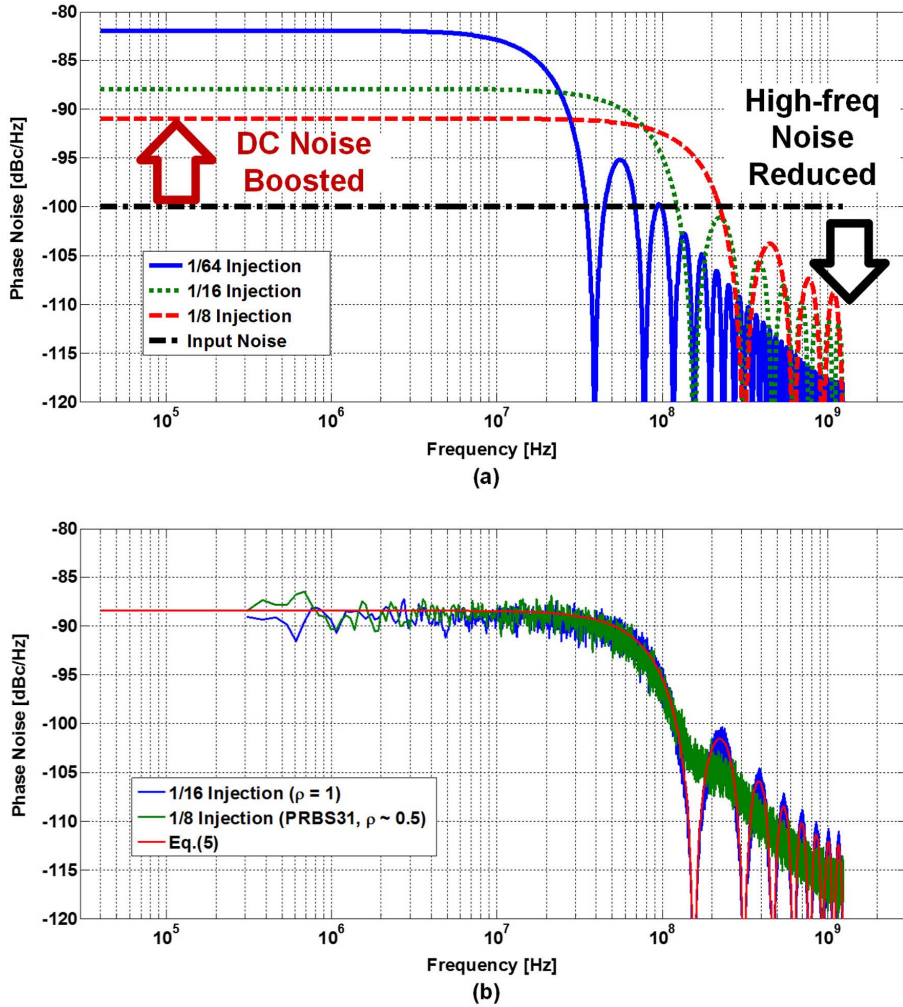


Fig. 7. Effect of noisy input injection on DCO output for different injection rates: (a) alternating input (5); (b) random input.

Plotting (5) as shown in Fig. 7 reveals some interesting properties. First, even if the input noise is white, the PSD of the injected DCO output clock exhibits a low-pass shape. As N increases, noise power at high frequencies is attenuated while the low frequency is amplified. By Parseval's theorem, the total phase noise power of the recovered clock (Y) is equal to that of the input (X) even if the shapes of their PSDs are different. This indicates that varying periodic injection rate alone does not help filter input noise. It merely shapes the noise profile while the total noise power remains the same. Thus, conventional GVCO-based CDRs cannot exhibit input jitter filtering function regardless of the data injection rate. On the other hand, the DPLL in the proposed CDR filters amplified low-frequency DCO phase noise within its bandwidth as shown in Fig. 8.

Hence, high- and low-frequency components of input noise injected into the DCO are filtered by the periodic injection path and the DPLL, respectively. The noise bandwidth for high-frequency noise is proportional to the injection rate ($1/N$). Thus, as the injection rate decreases, input noise gets filtered more and its contribution to recovered clock jitter reduces. This behavior is verified using simulations by feeding PRBS31 data with 1% UI_{rms} random jitter to the proposed and conventional PLL- and GVCO-based CDRs and plotting the recovered clock

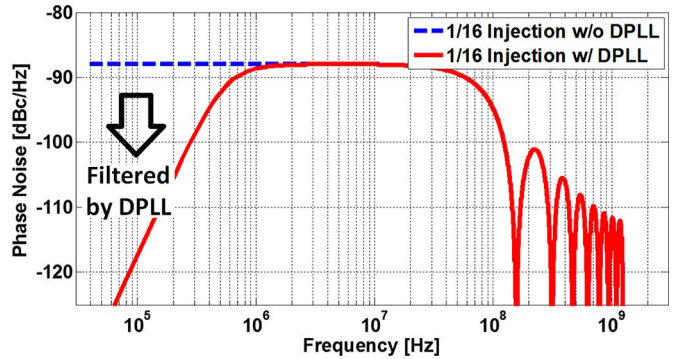


Fig. 8. Analyzed phase noise profile of periodically injected DCO in feedback loop.

jitter as a function of injection rate (see Fig. 9). As expected, the recovered clock jitter of the proposed CDR reduces when the injection rate is decreased and it converges to that of the PLL-based CDR as the data edge is injected less frequently into the DCO.

As mentioned earlier, the above analysis was performed for a transition density of 1 ($\rho = 1$). However, noting that only the

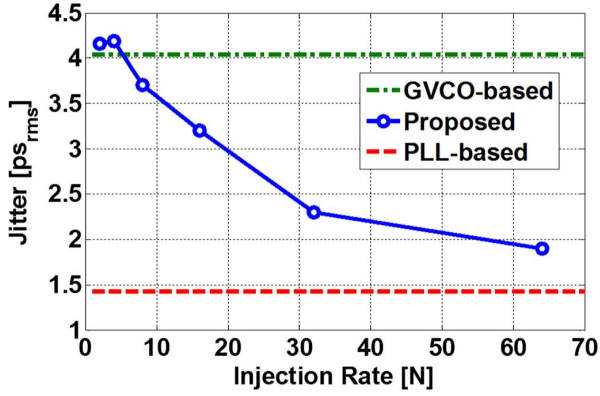


Fig. 9. Simulated jitter performance as a function of injection rate for PLL-based, GVCO-based, and proposed CDRs.

number of transitions are scaled by ρ , we expect scaling the injection rate ($1/N$) in the derived PSD expression provides the PSD for the case when $\rho \neq 1$. This conjecture is verified by behavioral simulations in which the DCO is injected with alternating data in one case and with PRBS31 random data ($\rho \approx 0.5$) in the other. The DCO output phase noise PSD for an injection rate of $1/16$ for alternating data and $1/8$ ($= 0.5 \times 1/16$) for PRBS31 data match well with the predicted PSD in (5) (see Fig. 7(b)).

B. DCO Phase Noise Rejection

Let Z denote the random process representing DCO period perturbation caused by thermal noise in DCO's delay stages and $Z[i]$ be the error in the period of i th cycle. For simplicity, let us ignore device flicker noise and assume that Z is wide-sense stationary with zero mean and that its power spectral density (PSD) is white. Therefore, its autocorrelation, $R_Z(i, j)$, is given by

$$R_Z(i, j) = E[Z[i]Z[j]] = \frac{\sigma_Z^2}{2} \delta_{ij} = \begin{cases} \frac{\sigma_Z^2}{2} & \text{if } i = j \\ 0 & \text{if } i \neq j \end{cases} \quad (6)$$

Because phase noise accumulates indefinitely in a stand-alone DCO, its output jitter sequence will be of the form $(Z[1], Z[1] + Z[2], Z[1] + Z[2] + Z[3], \dots)$. Now, if every N th edge is replaced by the data edge, the accumulated phase noise of the DCO is reset every time a new edge is injected. In that case, the output jitter sequence Y will be as follows:

$$Y = \left(Z[1], \dots, \sum_{i=1}^N Z[i], Z[N+1], \dots, \sum_{i=N+1}^{2N} Z[i], Z[2N+1], \dots, \sum_{i=2N+1}^{3N} Z[i], Z[3N+1], \dots \right) \quad (7)$$

Using (6), the average autocorrelation function of the cyclostationary random process Y , $\bar{R}_Y(i - j)$, can be calculated to be

$$\begin{aligned} \bar{R}_Y(i - j) &= \frac{1}{N} \sum_{j=0}^{N-1} E[Y[i]Y[j]] \\ &= \begin{cases} \frac{\sigma_Z^2}{2N} \sum_{k=1}^{N-|i-j|} k & \text{if } |i - j| < N \\ 0 & \text{if } |i - j| \geq N \end{cases} \quad (8) \end{aligned}$$

The PSD of Y , $S_Y(\omega)$, can be calculated by taking the Fourier transform of its autocorrelation function and is given by

$$\begin{aligned} S_Y(\omega) &= \sum_{\tau=-\infty}^{\infty} e^{-j\omega\tau} \bar{R}_Y(\tau) \\ &= \frac{\sigma_Z^2}{2} \sum_{k=0}^{N-1} \frac{N - k}{N} \frac{\sin(\omega k + \frac{\omega}{2})}{\sin(\frac{\omega}{2})} \quad (9) \end{aligned}$$

Equation (9) is plotted in Fig. 10 along with the output phase noise PSD of a stand-alone DCO. The phase noise of the DCO with periodic injection is similar to that of the DCO embedded in a PLL feedback loop with a bandwidth of $f_{\text{DCO}}/4N$, where f_{DCO} is the DCO oscillation frequency. Note that multiplying delay-locked loops (MDLLs) also employ similar periodic injection where the reference clock, in place of input data, is gated with the VCO edge [20], [21]. The gated reference clock resets VCO jitter accumulation and improves jitter performance compared to PLLs. The VCO phase noise suppression predicted by our analysis matches well with the result in [20]. The presented analysis can also be used to show VCO noise suppression bandwidth of the MDLL to be around $f_{\text{REF}}/4$, which was empirically verified in [20] and [21]. Since periodic injection prevents the DCO phase noise from accumulating indefinitely, the DCO in the proposed CDR was designed to have relatively poor phase noise (about -90 dBc/Hz at 1 MHz offset frequency, as opposed to -100 dBc/Hz or better phase noise in other architectures) to save power.

V. CIRCUIT IMPLEMENTATION

The circuit details of key building blocks of the proposed receiver, namely, the limiting amplifier, edge injection logic (EIL), and DCO, are presented in this section. Other blocks such as the full-rate bang-bang phase detector, decimator, $\Delta\Sigma$ modulator, and current-mode DACs are implemented using circuits similar to the ones described in [22].

A. Limiting Amplifier

The schematic of the limiting amplifier that converts low-swinging input data, D_{IN} , to CMOS levels is shown in Fig. 11. It is implemented using a cascade of two CML stages and a CML-to-CMOS converter similar to the one used in [23]. The combined gain and bandwidth of the two CML stages is about 22 dB and 2.6 GHz, respectively. A CML-to-CMOS converter serves the dual purpose of generating rail-to-rail CMOS outputs and more importantly, isolating the CML stages from kick-back noise of the edge detector. The input-referred noise and offset of the limiting amplifier directly impact the receiver sensitivity and therefore should be minimized. To that end, lengths of input differential pair transistors of the amplifier were chosen to be larger than minimum. The CML-to-CMOS converter is designed with minimum length devices to reduce self-loading because its offset is attenuated by the gain of the two-stage amplifier stages in front of it.

B. Edge Injection Logic (EIL)

Circuit implementation of the EIL and the associated timing diagram are shown in Fig. 12. An edge detector composed of a CMOS XNOR gate and an inverter-based delay line along with

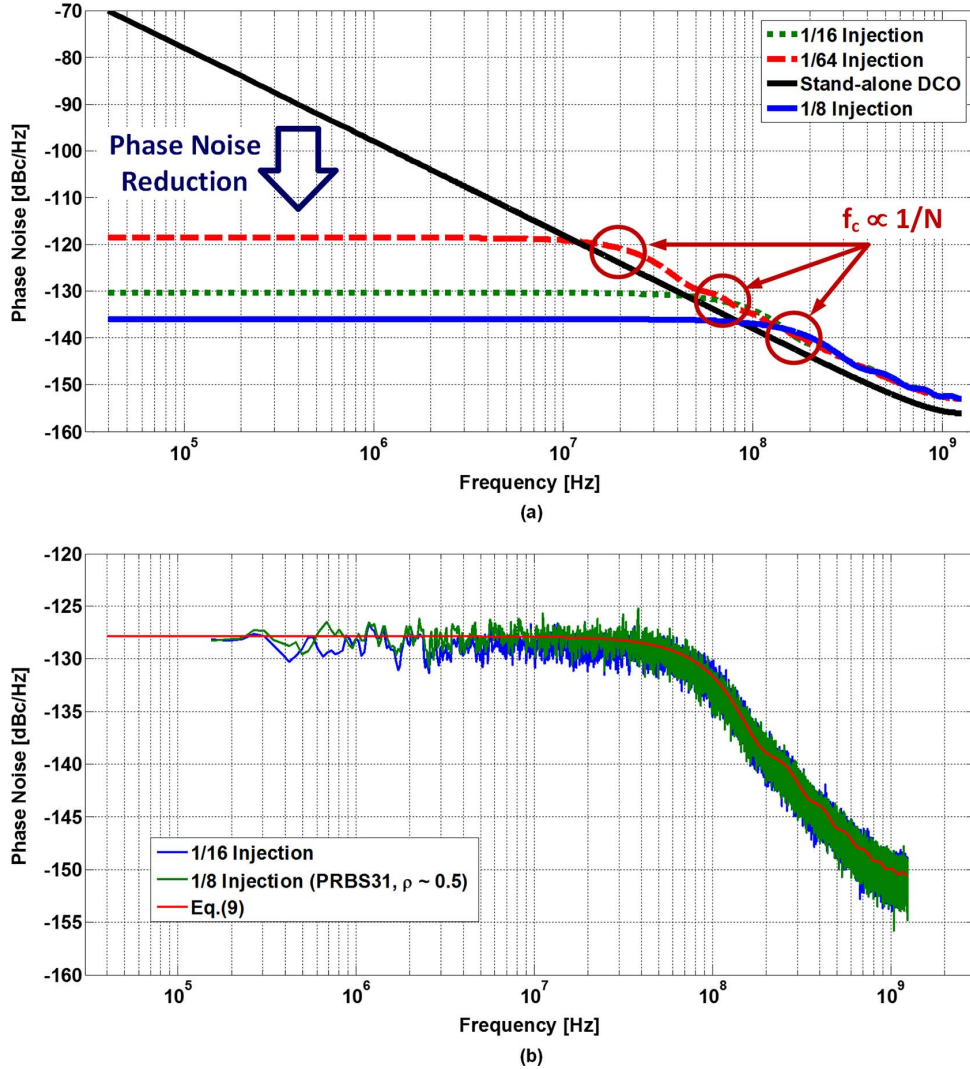


Fig. 10. Effect of injection on noisy DCO output for different injection rates: (a) alternating input (9); (b) random input.

the digital logic shown in Fig. 12(a) are used to inject the data edge into the oscillator. Edge injection instantaneously aligns DCO phase with the input data. The number of data transitions are counted using a ripple counter and the MUX select signal, CON, is asserted when the count reaches 2^N (see Fig. 12(b)). For simplicity, the timing diagram in Fig. 12(b) is drawn for the case when 2^N equals 4 (or $N = 2$), i.e., every fourth data edge is injected into the oscillator. In the prototype, N is controlled by an external digital code to have values from 3 to 6. When CON is high, the MUX passes the data transition edge, and the DCO edge is realigned to it. Right after this injection occurs, a reset pulse is generated to make the CON signal go back to low so that no data edge can be injected into the DCO until the counter counts 2^N more transitions in input data. Note that the edge injection is controlled by counting the number of data transitions instead of counting the number of clock cycles. This is because, during power-on transient when the DCO frequency is not settled, the timing relationship between the signals in the EIL (see Fig. 12(b)) becomes unpredictable, which may fail to inject the edge correctly and result in bit errors. In order to minimize the data-dependent jitter caused by the mismatch between

data edge injection and BBPD timing, delay of the data buffer driving the BBPD was manually controlled using their supply voltage as the delay-control knob instead of adding a low-bandwidth secondary compensation loop as in [24].

In order to facilitate power-cycling, in addition to burst-mode operation, an On/Off port is added to start/stop the DCO. When the receiver goes into the off-state (On/Off signal goes low), the MUX select signal is set to low and the EIL output stays low until On/Off goes high again, which forces the DCO to stop during the off-state. Note that since all the DPLL and FLL blocks are triggered by R_{CLK} , stopping the DCO from oscillating ensures no active power consumption in other blocks of the CDR. All the D-flip-flops' outputs in the ripple counter are reset during the off-state to ensure the first data edge is injected into the DCO (for fast locking) when powered on.

C. Digitally Controlled Oscillator (DCO)

The schematic of the DCO is shown in Fig. 13. It consists of a 4-stage gated current-controlled oscillator (GCCO) whose frequency is tuned by three DACs, denoted by DAC_F , DAC_I , and DAC_P . Data edge generated by the EIL is injected into the

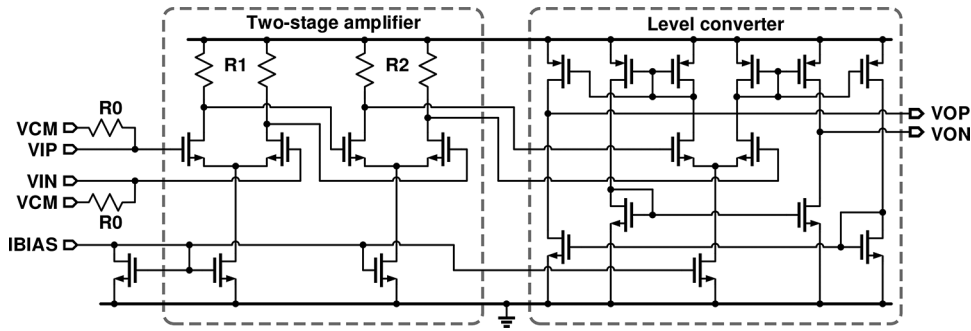


Fig. 11. Schematic of limiting amplifier.

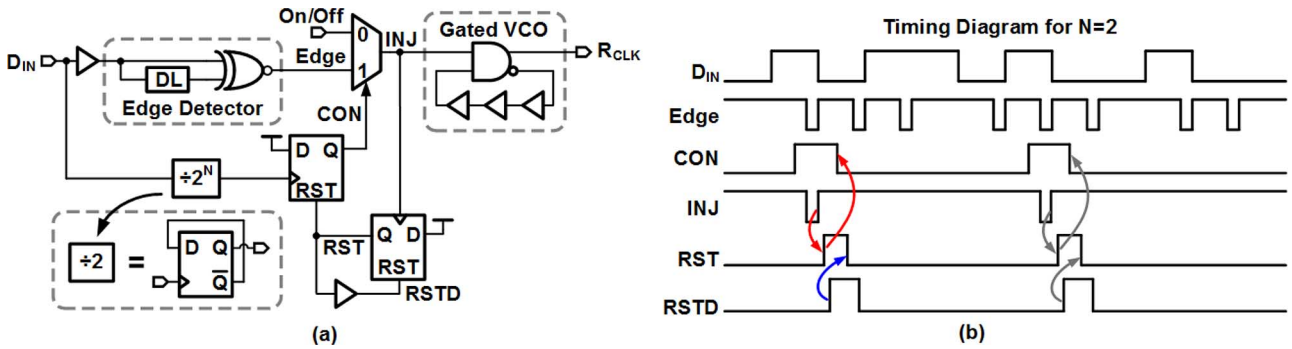


Fig. 12. Schematic of (a) edge injection logic and (b) its associated timing diagram.

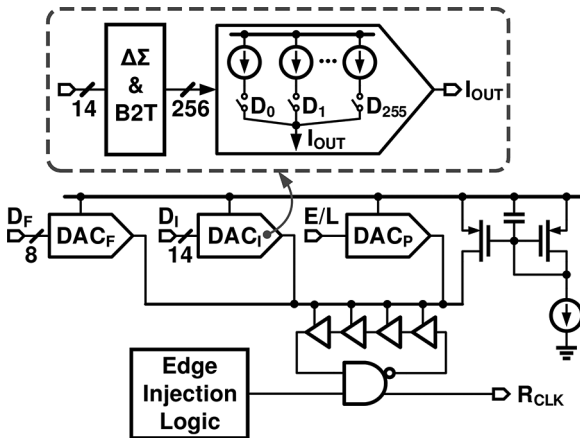


Fig. 13. Schematic of the digitally controlled oscillator.

GCCO using a NAND gate. The delay stages in the GCCO are implemented using current-controlled pseudo-differential delay cells (shown as single-ended in Fig. 13 for simplicity) similar to those reported in [22]. DAC_P converts 3-level early/late outputs of the BBPD into current and drives the GCCO to implement proportional control of the Type-II PLL. Input to the other two DACs, D_F and D_I , are generated by the FLL and the integral path of the DPLL, respectively. While DAC_F is directly driven by the 8 MSBs of accumulator output, DAC_I needs to have much higher resolution and is hence implemented as a $\Delta\Sigma$ DAC. The 14 bit D_I is first truncated to 8 bits by a second-order $\Delta\Sigma$ modulator and an 8 bit thermometer-coded current-mode DAC is used to generate the output current. Note that it is possible to ease the hardware complexity of the current-mode DAC by truncating the input control word to a lesser number of

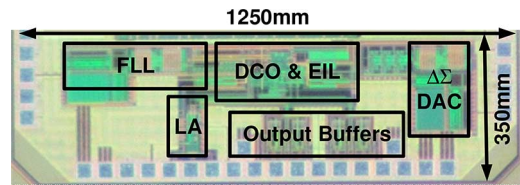


Fig. 14. Die micrograph.

output bits (say, 4 instead of 8). However, in that case, suppression of additional $\Delta\Sigma$ truncation error would require a low-pass analog post filter, which increases the frequency settling time of the DCO. Simulations indicate that adding an analog post filter decreases the recovered clock jitter by 5% (from 4.1 ps to 3.9 ps), while increasing the frequency settling time by more than 30 times (from 20 ns to over 700 ns). Hence, we chose 14 bit to 8 bit truncation to minimize the contribution of residual $\Delta\Sigma$ truncation error to recovered clock output jitter without using an analog post filter.

When the receiver is turned off, the EIL stops the DCO from oscillating by outputting a logic low as the gating signal into the GCCO. As a result, the oscillator does not draw any current and its virtual supply voltage, V_S , reaches V_{DD} in the off-state. When the DCO starts oscillating on the subsequent power-on cycle, node V_S starts to settle from its initial value of V_{DD} even if the frequency control words D_F and D_I are pre-set accurately. The time constant associated with this settling transient is inversely proportional to the impedance and capacitance at node V_S . In view of this, decoupling capacitor C_D is chosen to be about 5 pF to suppress the voltage ripple on V_S without increasing the settling time by more than 20 ns. Note that even

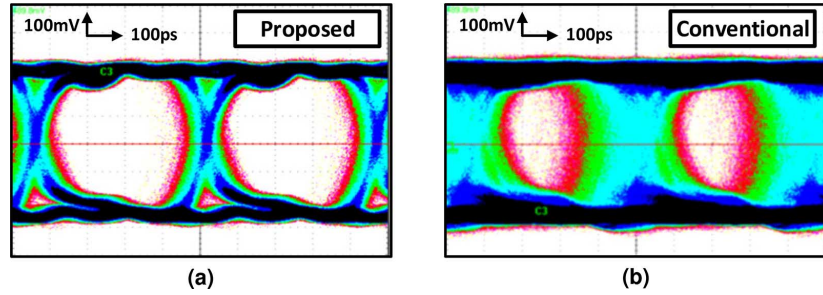


Fig. 15. Measured recovered eye diagram with an initial frequency error of 1%: (a) proposed CDR; (b) conventional GVCO-based CDR.

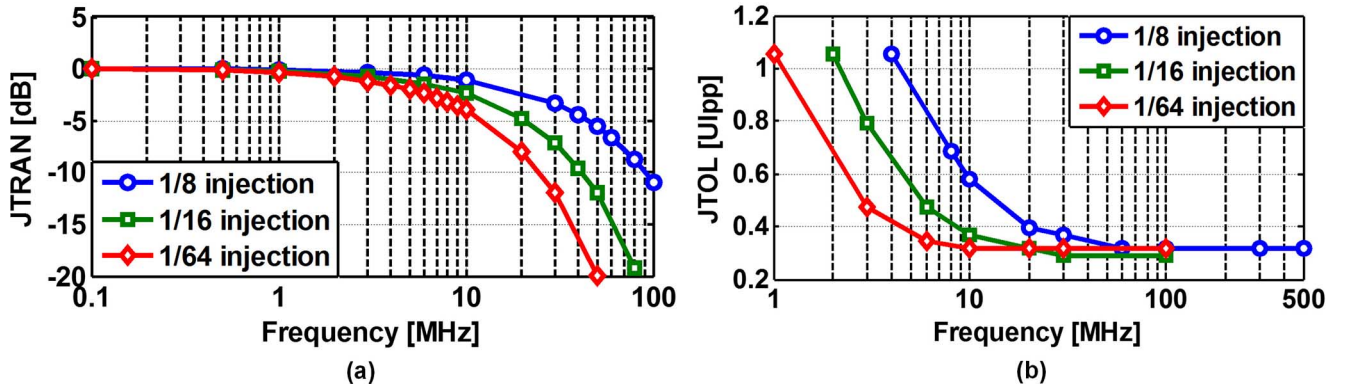


Fig. 16. Measured (a) jitter transfer function and (b) jitter tolerance plots for three different injection rates.

if the DCO settling time is about 20 ns, thanks to edge injection, the proposed CDR is able to recover the data correctly, i.e., achieve error-free operation even during the settling transient of the DCO.

VI. MEASUREMENT RESULTS

The prototype receiver was fabricated in a 90 nm CMOS process and occupies an active area of 0.44 mm². The die micrograph is shown in Fig. 14. At 2.2 Gb/s data rate, it consumes 6.1 mW from a 1.2 V supply and achieves error-free operation ($\text{BER} < 10^{-12}$) in both continuous and burst modes with PRBS23 data. To quantify the sensitivity of the proposed CDR to frequency error present at the beginning of receiving burst data, we introduce 1% frequency offset in the DCO and evaluate the recovered eye diagram and bit-error rate (BER). The measured recovered data eye diagram is shown in Fig. 15(a) and no bit errors were recorded during the power-on transient. For comparison, the PLL feedback loop was disabled to mimic the behavior of a conventional GVCO-based CDR and the resulting recovered data eye diagram is also shown in Fig. 15(b). The phase error accumulation caused by frequency offset manifests as increased jitter and degrades the timing margin as seen in Fig. 15(b). Because of the conventional GVCO-based CDR's inability to correct frequency offset, phase error accumulation persists. However, when the PLL loop was enabled, this frequency error is corrected and the jitter caused by phase drift reduces dramatically.

Fig. 16(a) shows the measured jitter transfer (JTRAN) plots of the proposed CDR for three different edge injection rates. The jitter transfer bandwidth scales in proportion to the injection rate as predicted by the analysis, illustrating the CDR's ability to

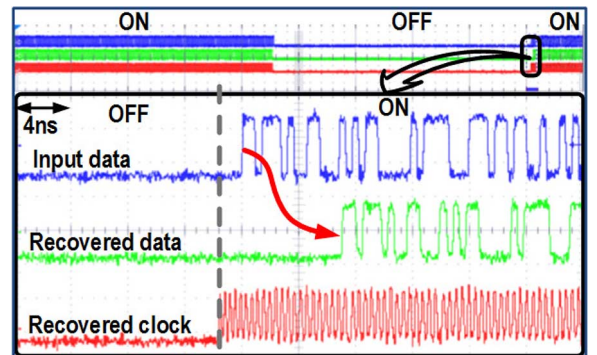


Fig. 17. Measured power-on transient response.

filter input jitter in a controlled manner. Jitter transfer bandwidth is measured to be around 30 MHz when the injection rate is 1/8, and it reduces to around 6 MHz when the injection rate is changed to 1/64. Fig. 16(b) shows the measured jitter tolerance curves for three different injection rates. They were measured with PRBS7 input data with a BER threshold of 10^{-12} . Similar to the JTRAN behavior, jitter tolerance corner frequency also scales in proportion to the injection rate. High-frequency jitter tolerance is limited by DCO phase noise, data ISI, and CIDs.

Power-on transient response when the CDR is power-cycled with 5 μs off-state time was captured by an oscilloscope and is shown in Fig. 17. It can be observed that the DCO stops oscillating during the off-state and that the CDR recovers the input data within 1 UI, i.e., the CDR can recover the data from the very first bit. The 8 ns latency was introduced by the delay in the data path (limiting amplifier and the delay line in the edge detector) and an SMA cable. The CDR's tolerance to CIDs is measured

TABLE I
BURST-MODE CDR PERFORMANCE SUMMARY AND COMPARISON

	[12]	[13]	[15]	[25]	[26]	This work
Technology	0.11 μm CMOS	0.13 μm CMOS	0.25 μm SiGe BiCMOS	40 nm CMOS	65 nm CMOS	90 nm CMOS
CDR Architecture	Oversampling	GVCO-based w/ replica	GVCO-based w/o replica	Injection-lock w/ replica	PI-based	EIL + DPLL
Data Rate	3.2 Gb/s	10 Gb/s	10.3 Gb/s	5.184 Gb/s	6 Gb/s	2.2 Gb/s
BER	$< 10^{-11}$	$< 10^{-12}$ (PRBS31)	$< 10^{-12}$ (PRBS23)	$< 10^{-10}$ (PRBS7)	$< 10^{-12}$ (PRBS7)	$< 10^{-12}$ (PRBS23)
Locking Time	N/A	5 bits	1 bit	< 20 bits	1 bit	1 bit
CID Tolerance	N/A	31 bits	160 bits	N/A	N/A	128 bits
JTOL	0.7 UI_{PP} @ 10 MHz	N/A	0.27 UI_{PP} @ 80 MHz	1.1 UI_{PP} @ 10 MHz	N/A	0.3-0.6 UI_{PP} @ 10 MHz
JTRAN BW	N/A	No rejection	No rejection	N/A	N/A	5 to 40MHz
Power [mW]	115 mW	1.2 W	544 mW	12.4 mW*	22 mW	6.1 mW*
Power efficiency	35.9 pJ/bit	120 pJ/bit	52.8 pJ/bit	2.39 pJ/bit*	3.67 pJ/bit	2.77 pJ/bit*
Chip Area	0.15 mm^2	6.25 mm^2	9 mm^2	0.017 mm^2	0.018 mm^2	0.44 mm^2
Input Tracking Ability	No	No	No	No	No	Yes

* Not including limiting amplifier power

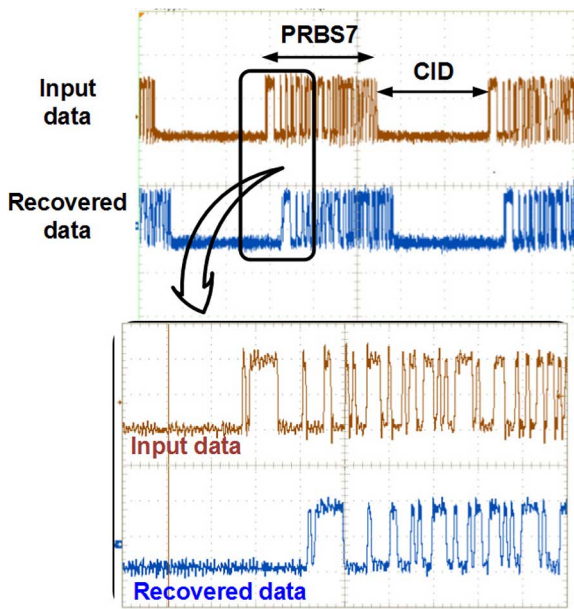


Fig. 18. Measured input and recovered data waveform in the presence of 128 CIDs.

by inserting 128 zeroes in between the PRBS7 sequence and the results are presented in Fig. 18. The CDR operated error-free even in the presence of this large number of CIDs and the BER

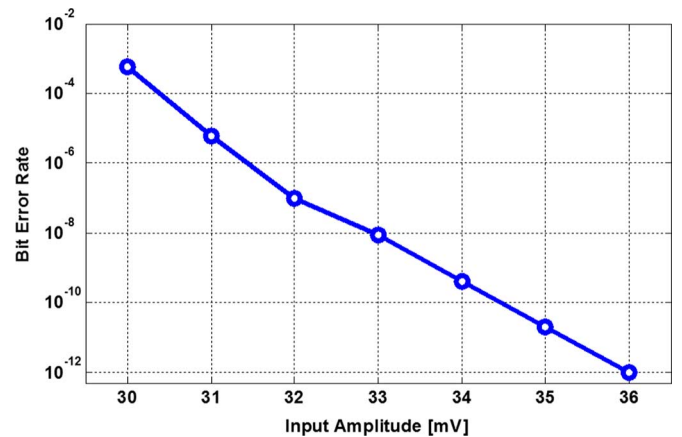


Fig. 19. Measured BER as a function of input data amplitude.

remained less than 10^{-12} . The input sensitivity of the CDR is evaluated by measuring the BER as a function of voltage swing of PRBS7 input data (see Fig. 19). The input sensitivity is measured to be about 36 mV_{PP} to achieve BER less than 10^{-12} .

The power-scaling behavior of the CDR is illustrated in Fig. 20 by plotting power consumption (normalized to the peak power) as a function of the effective data rate (normalized to the peak data rate). The effective data rate is changed by varying the duty cycle of the On/Off signal. Owing to the

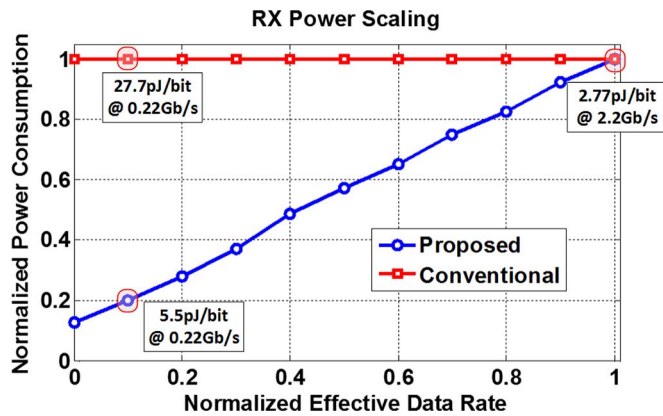


Fig. 20. Normalized receiver power vs. effective data rate.

short turn-on time, power scales almost linearly with data rate. Consequently, receiver energy efficiency varies only from 2.77 pJ/bit to 3.87 pJ/bit, even as the effective data rate is varied from 0.44 Gb/s to 2.2 Gb/s for 32 byte bursts. The off-state power of the receiver is larger than expected due to a design error, which caused some of the static currents to be ON even in the off-state. Correcting for the error lowers the total off-state power to 20 μ W, which extends the lower limit of the energy proportional range from 0.44 Gb/s to 0.02 Gb/s.

At 2.2 Gb/s, the CDR consumes 6.1 mW, and the limiting amplifier consumes an additional 5.5 mW of power. The performance summary and comparison of the proposed CDR with state-of-the-art designs are shown in Table I. Compared to other burst-mode CDRs, the proposed CDR shows very good CID tolerance and it is the only burst-mode CDR that exhibits much desirable programmable input jitter filtering characteristics. The power efficiency of the proposed receiver (5.27 mW/Gb/s) compares favorably in spite of using an on-chip limiting amplifier.

VII. CONCLUSION

A digital burst-mode receiver suited for energy proportional links is presented. By combining a feed-forward GVCO-based CDR with a phase-tracking feedback CDR, the proposed CDR achieves both instantaneous phase-locking and input jitter filtering. Furthermore, we demonstrated that the jitter transfer bandwidth can be altered in a controlled manner by varying the injection rate. Compared to conventional GVCO-based CDRs, thanks to the PLL feedback loop, the proposed CDR is also more immune to frequency error between the VCO and the input data at the beginning of the burst. In other words, the proposed CDR is robust to VCO frequency drift during the off-state. The PLL feedback also helps improve the CDR's tolerance to CIDs and reduce recovered clock jitter. Fabricated in a 90 nm CMOS process, the prototype receiver is able to recover input data from the very first bit and consumes 6.1 mW at 2.2 Gb/s. Owing to the short turn-on time, receiver energy efficiency varies only from 2.77 pJ/bit to 3.87 pJ/bit, when the effective data rate is varied from 0.44 Gb/s to 2.2 Gb/s. By varying the injection rate from 1/64 to 1/8, the JTRAN bandwidth was shown to vary from 5 MHz to 40 MHz. Using a limiting amplifier resulted in a measured input sensitivity of 36 mV_{pp} for a BER of 10^{-12} .

ACKNOWLEDGMENT

The authors thank Berkeley Design Automation for providing the Analog Fast Spice (AFS) simulator.

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