A Fast Power-on 2.2Gb/s Burst-mode Digital CDR with Programmable Input Jitter Filtering

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Abstract

A digital burst-mode CDR employs feed-forward data edge injection and a digital feedback loop to achieve instantaneous phase locking, data-rate tracking, and input jitter filtering. Fabricated in a 90nm CMOS process, the prototype receiver achieves instantaneous locking on the very first data edge and consumes 6.1mW at 2.2Gb/s. By controlling the edge injection rate, the proposed architecture allows variable JTRAN bandwidth from 5MHz to 40MHz.

Introduction

Traditionally burst-mode transmission is employed in point-to-multipoint fiber access systems such as passive optional networks. More recently, it also emerged as an effective means to achieve energy proportional operation in applications with dynamic bandwidth requirements such as memory interfaces and chip-to-chip links in mobile platforms and servers. By power cycling the link (turning on/off appropriately) this mode of communication can ideally achieve power scaling with the usage, thus maintaining excellent energy efficiency over a very wide range of effective data rates. This approach leads to larger power savings compared to links optimized only to operate at peak performance [1]. In this paper we address the design of a burst-mode receiver for this application.

A burst-mode CDR is the most critical building block in the receiver. Because of the sluggish phase acquisition of classical PLLs, burst-mode CDRs are commonly implemented using gated-VCO (GVCO) based architectures as depicted in Fig. 1. The GVCO frequency is set by a replica VCO embedded in a feedback loop and instantaneous phase locking is achieved by injecting the data edge into the oscillator [2]. While its simplicity is appealing, GVCO-based CDR suffers from two main drawbacks. First, the inevitable mismatch between the two VCOs due to PVT variations causes phase error between the data and sampling clock to accumulate over time which reduces timing margin and degrades jitter tolerance. Consecutive identical digits (CIDs) further exacerbate this issue. To mitigate the mismatch, an architecture using a single VCO whose frequency was set by an FLL was proposed [3] (see Fig. 1). In this case, mismatch between the input data rate and the local reference frequency causes jitter accumulation. Second and the most important drawback is that the GVCO-based CDRs cannot reject input jitter because of their feed-forward operation. In view of these drawbacks, we propose a digital CDR with programmable input jitter filtering and instantaneous phase-locking response. Thus the proposed architecture combines the advantages of the feed-forward GVCO-based CDRs and the feedback PLL-based CDRs.

Proposed Architecture

The block diagram of the proposed fast power-on burst-mode receiver is shown in Fig. 2. It consists of a limiting amplifier, and a split-tuned digital CDR consisting of a frequency-locking loop (FLL) and a Type-II digital PLL (DPLL). At start-up, the digital FLL consisting of a frequency detector (FD) and an accumulator drives the digitally controlled oscillator (DCO) frequency to within the pull-in range of the CDR. DPLL uses a bang-bang phase detector (BBPD) to drive the digital loop filter and achieves phase lock. Fast frequency settling is achieved by avoiding low-pass filters to suppress shaped truncation error in ΔΣ DACs. Instead, the shaped noise is suppressed by leveraging the DPLL's loop bandwidth.

An XNOR-based transition detector and the edge injection logic (EIL) are used to inject the data edge into the oscillator, which instantaneously aligns the DCO phase with the input data. Input jitter filtering is achieved by injecting the data edge only occasionally. It can be shown that injecting once every 2^N data transitions causes the jitter transfer (JTRAN) bandwidth to scale in proportion to N. Intuitively, when N=0 the proposed CDR simplifies to GVCO-based architecture and exhibits all-pass JTRAN characteristics. On the other hand, when N=∞, JTRAN is equal to the bandwidth of the type-II DPLL. For the values of N between zero and infinity, JTRAN scales with N. Note that conventional GVCO-based CDRs exhibit all-pass JTRAN regardless of the injection rate.

Fig. 3 shows the schematic of the DCO along with the EIL. The DCO consists of a NAND gate and four current-controlled delay cells. Its frequency is controlled by fast-settling 8-bit current-mode ΔΣ DACs. EIL counts the number of data transitions, asserts the MUX select signal, *CON*, every 2^N transitions, and passes the data transition edge instead of the DCO edge. Right after the injection, a reset pulse is generated to de-assert the *CON* signal. To facilitate power-cycling in addition to burst-mode operation, *On/Off* port is added to start/stop the DCO. When the receiver enters the off-state, the oscillator stops and the accumulators in the FLL and the integral path store the coarse and fine frequency control words, D_F and D_I, respectively. When the receiver is powered-on, the DCO's frequency is accurately preset using D_F and D_I.

Measured Results

The proposed receiver is fabricated in a 90nm CMOS process and occupies an active area of 0.44mm^2. At 2.2Gb/s, it consumes 6.1mW and achieves error-free operation (BER<10^{-12}) in both continuous and burst modes with PRBS23 data. To evaluate the sensitivity of the proposed CDR to initial frequency error, it is operated with about 1% error between the input data rate and the DCO frequency and the recovered eye diagrams are shown in Fig. 4. As expected, when the feedback loop is disabled to mimic the behavior of a conventional GVCO-based CDR, phase error accumulates between two consecutive data injections, which manifests as increased jitter in the recovered data eye. When the loop is enabled, this frequency error is corrected and the jitter reduces dramatically. Measured jitter transfer (JTRAN) and jitter tolerance (JTOL) plots for various injection rates are shown in Figs. 5 and 6, respectively. JTRAN bandwidth scales in proportion to the injection rate (6MHz @ 1/64 injection rate to 30MHz @ 1/8 injection rate), which illustrates the CDR's ability to filter input jitter in a controlled manner. Power-on transient response captured in Fig. 7 indicates the power-on time of the receiver is 1-bit period. The input buffers and the delay line in the edge detector introduce 8-ns latency. Performance of the proposed

CDR is compared with other state-of-the-art burst-mode CDRs in Fig. 8. The die micrograph is shown in Fig. 8.

Acknowledgement

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References

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[3] J. Terada, *et al*, "A 10.3125Gb/s burst-mode CDR circuit using a ΔΣ DAC," *in ISSCC Dig. Tech. Papers*, pp. 226–227, Feb. 2008.

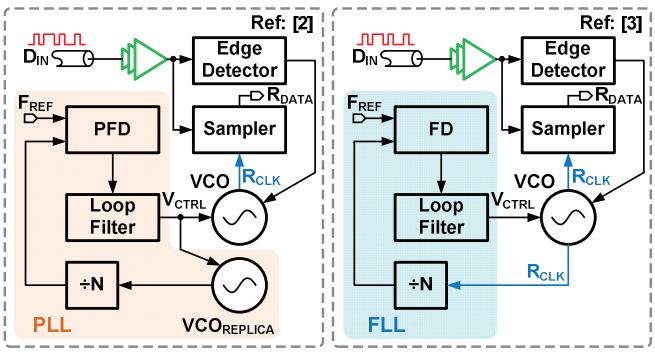

Fig. 1 Conventional burst-mode CDRs.

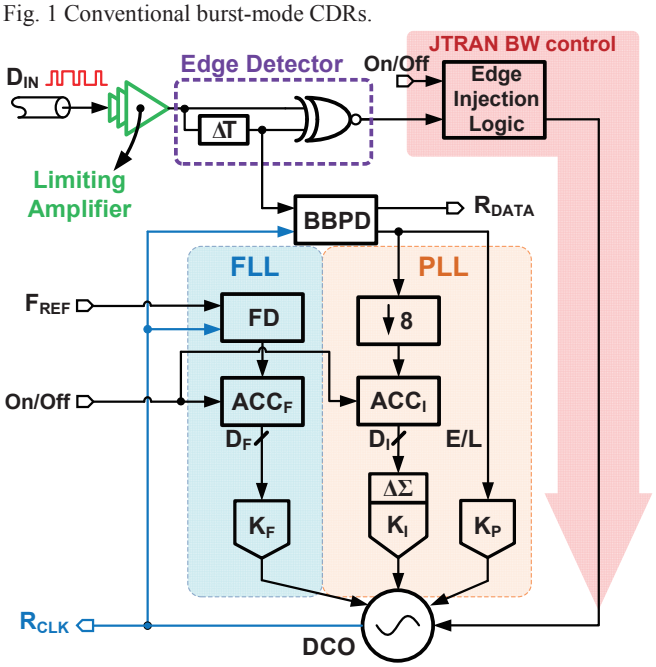

Fig. 2 Block diagram of the proposed receiver.

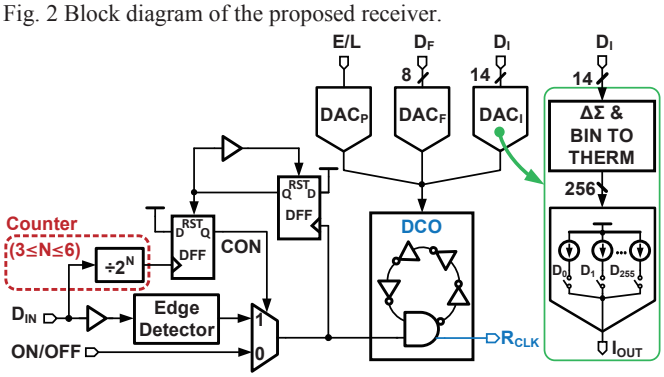

Fig. 3 Schematic of the DCO and edge injection logic.

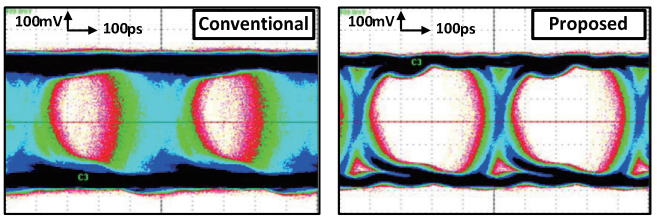

Fig. 4 Recovered PRBS23 eye diagrams measured with 1% frequency error between input data and DCO frequency.

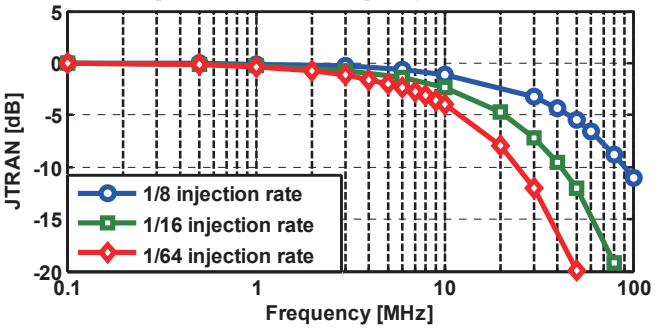

Fig. 5 Measured JTRAN curves with different injection rates.

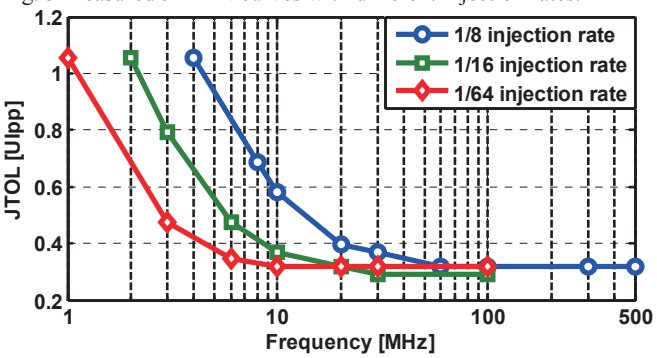

Fig. 6 Measured JTOL curves with different injection rates.

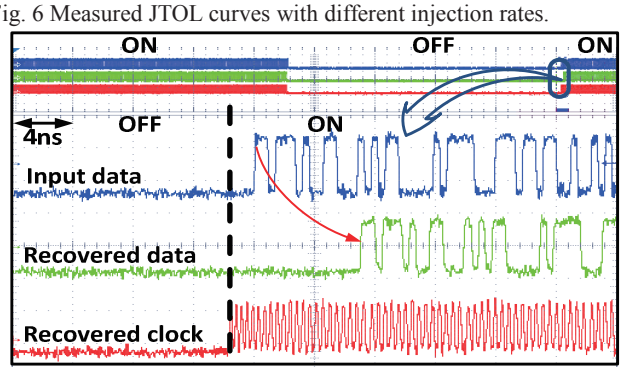

Fig. 7 Measured power-on behavior.

	This Work	ISSCC'05 12.5 [2]	ISSCC'08 11.4 [3]
Technology	90nm CMOS	0.13µm CMOS	0.25µm SiGe BiCMOS
Implementation	Single VCO Closed Loop	Multiple GVCO Open Loop	Single GVCO Open Loop
Data Rate	2.2 Gb/s	10 Gb/s	10.3125 Gb/s
BER	< 10^{-12} (PRBS23)	< 10^{-12} (PRBS31)	< 10^{-12} (PRBS31)
Power	6.1 mW	1200 mW	856 mW
Power / Gb/s	2.77mW/Gb/s	120mW/Gb/s	83mW/Gb/s
CID Tolerance	128 bits	31 bits	160 bits
JTOL	0.3 to 0.6UIpp @ 10MHz	N/A	0.27UIpp @ 80MHz
JTRAN BW	5 to 40MHz	No rejection	No rejection
Chip Area	0.44 mm²	6.25 mm²	9 mm²
Locking Time	1 bit	5 bits	1 bit
Fast Power-On	Yes	No	No

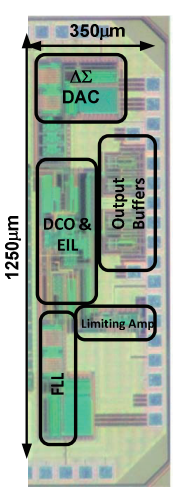

Fig. 8 Performance comparison table and chip micrograph.