A 13.6-16Gb/s Wireline Transceiver with Dicode Encoding and Sequence Detection Decoding for Equalizing 24.2dB with 2.56pJ/bit in 65nm CMOS

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***Abstract*—This work presents an alternative strategy for communicating on bandwidth limited wireline channels without using conventional equalizers (FFE, DFE, CTLE): Dicode encoding and sequence detection decoding technique for low-bandwidth FR-4 channels. The key observation is that dicode-encoded data have no consecutive 1s or -1s. With this known information, the sequence detector at the receiver can correct errors due to inter-symbol interference. Implemented in 65nm CMOS, the proposed highly digital encoding and decoding approach can compensate for up to 24.2dB and 21.4dB loss with 2.56pJ/bit and 2.66pJ/bit efficiency while operating at 13.6Gb/s and 16Gb/s, respectively.**

I. Introduction

Increasing the data rate through bandwidth-limited wireline channels requires equalization to cancel the inter-symbol interference (ISI). Since wireline channels have low-pass characteristics, equalization is typically achieved by leveraging high-pass filters/equalizers (FFE, DFE, and CTLE). Multiple taps are required to compensate for heavy channel loss, which results in high power consumption and reduced energy efficiency. Furthermore, increasing the number of taps gives a diminishing return on the maximum achievable data rate after a certain point [1].

To support the ever-increasing higher data rates and compensate for heavier channel loss while conventional equalizers start to give diminishing returns, data encoding and decoding techniques can be introduced. In upper layers of communication stack, techniques such as convolution codes and sequence detection based Viterbi decoding [2] can equalize channels and achieve low BER in the presence of ISI. However, they come at the cost of (a) low energy efficiency [3, 4], (b) low achievable data rate due to high complexity and feedback requirement in the decoder [4], (c) high latency in the decoding process (100s of UI), and (d) coding overhead which requires additional bits to be transmitted in the message.

In view of these limitations, we present a dicode encoding and sequence detection decoding concept to equalize ISI. This paper presents two types of all digital sequence detection based decoders, which can help to achieve BER < 10^{-12}. The proposed encoding/decoding approach has (a) high energy efficiency, (b) no feedback loops in the decoder (it is a feed-forward architecture), (c) small logic depth with a decoding latency of only 5 UIs (3 UIs from re-timers, 2 UIs from decoder logic), and (d) zero coding overhead. Operating at 13.6Gb/s, 14.4Gb/s, and 16Gb/s, the 65nm CMOS transceiver with the proposed encoding and decoding concept can compensate for 24.2dB, 21.6dB and 21.4dB with energy efficiency of 2.56pJ/bit, 2.38pJ/bit, and 2.66pJ/bit, respectively. Compared to the state-of-the-art Viterbi-based transceivers, the proposed transceiver achieves 4x better energy efficiency, 3x higher data rate, and 30x lower latency while equalizing 3dB higher channel loss [4].

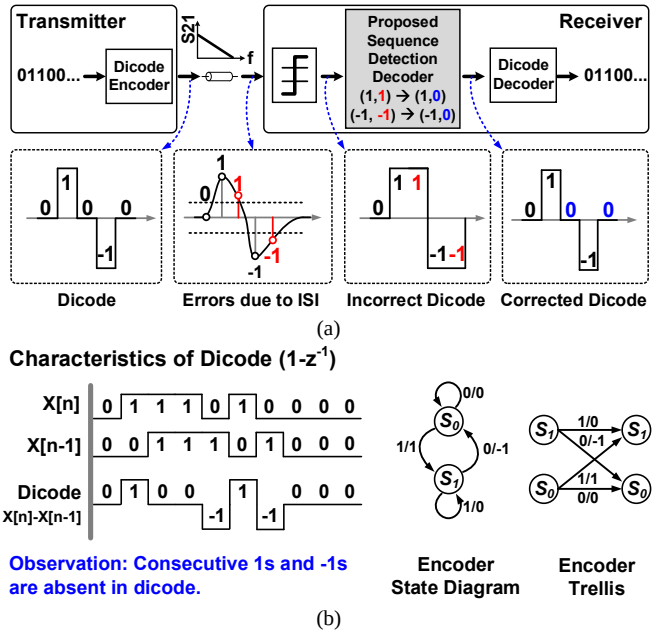


Fig. 1. (a) Concept of the proposed sequence detection decoder using dicode coding for detecting and correcting bit errors caused by ISI. (b) Characteristics of dicode with timing diagram, state diagram, and trellis of dicode encoder.

This paper is organized as follows: Section II presents the key observation in dicode encoding and compares with prior approach. Section III presents the proposed transceiver architecture. Measurement results are presented in Section IV followed by the conclusion in Section V.

II. Dicode Encoding & Sequence Detection Decoding

Sequence detection based decoding strategy leverages the fact that the data is transmitted with a known pattern and bit errors due to noise and ISI can be detected/corrected by the receiver by comparing the received data with the closest known pattern. In conventional sequence detection based transceivers, creating known patterns involves overhead bits that result in a reduction in the data rate. In the proposed approach, on the other hand, the receiver can perform sequence detection and correct errors due to ISI without additional overhead bits.

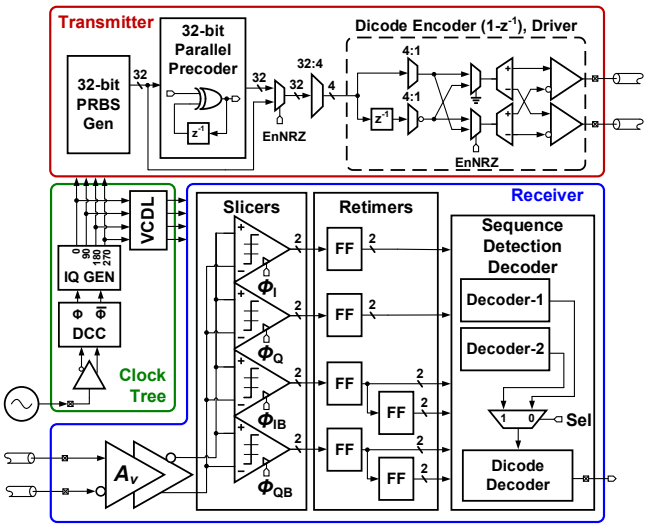


Fig. 2. Proposed transceiver architecture.

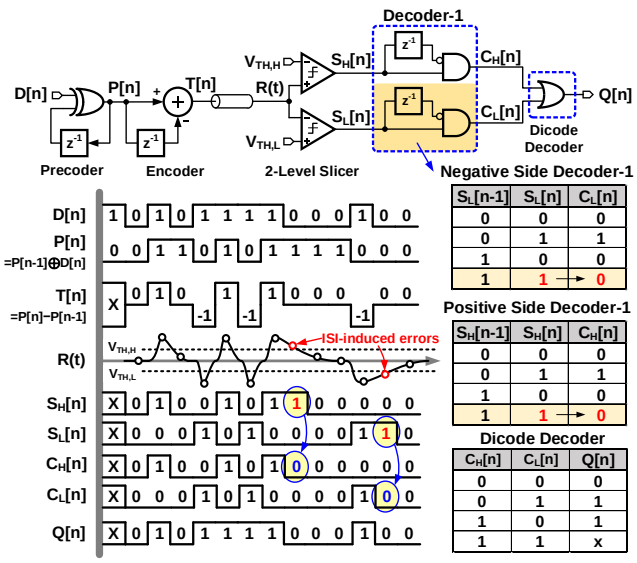


Fig. 3. Simplified full-rate representation of the proposed transceiver with a sequence detection decoder (Decoder-1) for a post-cursor dominant channel (top), timing diagram of error correction process (bottom left), and truth table of Decoder-1 and pre-coded dicode decoder (bottom right).

A. *Key Observation in Dicode-encoded Data*

Dicode-encoded data ($1-z^{-1}$) are generated by subtracting the delayed bit from the current bit and this creates 3 voltage levels (-1,0,1). A key characteristic of dicode-encoded data is that the encoded data do not have consecutive 1s and or -1s, as shown in Fig. 1. When the dicode-encoded data pass through a bandwidth-limited wireline channel, the symbol 1 and -1 spread out to their neighboring bits, creating ISI. Consequently, the receiver slicers incorrectly sample data and have patterns with two or more consecutive 1s or -1s which do not exist in dicode. Therefore, the receiver can detect them as errors due to ISI and correct them to the nearest possible valid sequence.

B. *Difference and Advantage over Duobinary, FFE, and DFE*

Partial response signaling such as duobinary generates controlled ISI by "absorbing" the channel loss in $1+z^{-1}$, which is canceled at the receiver to recover the data. Absorbing the channel loss requires multiple feed-forward equalizer (FFE) taps with several slices at the transmitter [5]. Multiple slices require multiple pre-drivers, which increases power consumption. Furthermore, the coefficients of these taps require adaptation through a backchannel, which can be expensive or often unavailable in some applications.

In the proposed work, the dicode encoder does not "absorb" channel in $1-z^{-1}$, and it does not require multiple slices, coefficient adaptation or backchannels. Unlike decision feedback equalizers (DFE) with tight timing constraints, the proposed decoder is a feed-forward architecture without feedback loops. Error propagation is avoided using a pre-coder.

C. *Difference and Advantage over Prior Dicode Works*

Power spectral density of dicode-encoded data has high energy at a higher frequency and low energy close to DC. Researchers have used this feature to achieve communication in high-pass channels (capacitive or transformer coupled channels) [6]. This work differentiates itself from prior works on the fact that this work leverages the feature of no consecutive 1s and -1s in the dicode-encoded data to cancel out ISI in low-pass channels (FR-4 backplanes or coaxial cables) using one of the proposed sequence detection based decoders.

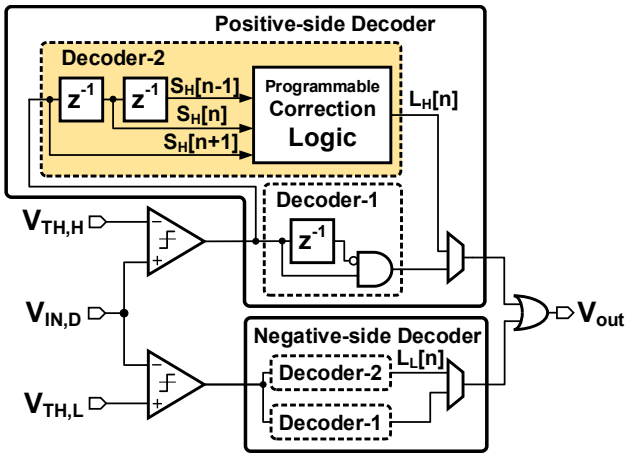
III. Proposed Transceiver Architecture

The proposed transceiver architecture is shown in Fig. 2. The transmitter consists of a 32-bit parallel PRBS generator, a 32-bit parallel dicode precoder (synthesized), which helps to avoid error propagation, a 32:4 serializer, and a 4:1 multiplexed source-series terminated output driver with a built-in dicode encoder. The receiver consists of two voltage amplifiers, quarter-rate two-level slicers, re-timers, and the proposed sequence detection decoders (Decoder-1, Decoder-2) followed by a pre-coded dicode decoder. Decoder-1 or Decoder-2 can be selected based on the channel loss profile. Decoder-1 (low complexity) can compensate for low-loss channels and Decoder-2 (high complexity) can equalize high-loss channels.

A. *Decoder-1 Architecture*

Proposed Decoder-1 architecture and timing diagram are shown in Fig. 3. When the dicode-encoded signal T[n] is transmitted through a channel, the 1 and -1 pulses spread out due to ISI. As a result, the received signal R(t) is sampled with errors. To detect and correct bit errors, the positive side and negative side of Decoder-1 independently compares the previously sampled bit with the current bit.

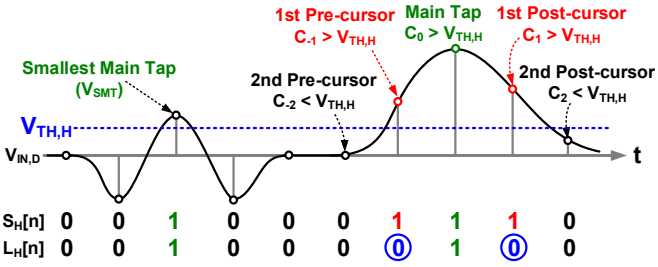
Example 1: If both previous and current bits are 1 ($S_H[n+1]=1$, $S_H[n]=1$), the decoder detects this as an error since two consecutive 1s and -1s do not exist in dicode. Decoder-1 assumes that the channel is post-cursor dominant, implying that the current bit 1 is actually the post-cursor of the previous bit 1. Therefore, the decoder corrects the current bit to 0 ($C_H[n]=0$). Dicode decoder (OR / XOR) takes the corrected $C_H[n]$ and $C_L[n]$ to generate the NRZ data Q[n]. There are no feedback loops in the proposed decoder which helps to avoid timing constraints. The latency of this decoding logic is 1 UI.



(a)

$S_H[n-1]$	$S_H[n]$	$S_H[n+1]$	$L_H[n]$ Pre-&Post-cursor Dominant Channels	$L_H[n]$ Post-cursor Dominant Channels	$L_H[n]$ Pre-cursor Dominant Channels
0	1	0	1	1	1
0	1	1	0	1	0
1	1	1	1	0	0
1	1	0	0	0	1
0	0	0	0	0	0
0	0	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1

(b)



(c)

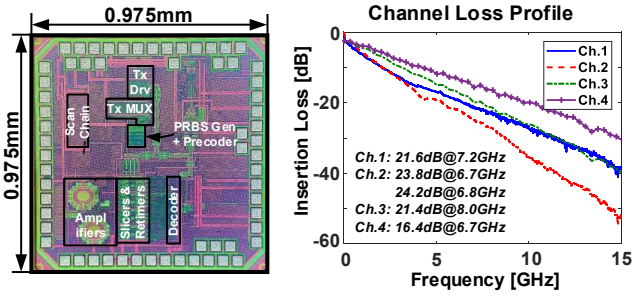
Fig. 4. (a) Simplified diagram of the full-rate decoder. (b) Truth table of positive-side Decoder-2 correction logic which can be programmed based on channel characteristics. (c) Example transient waveforms to set the slicer threshold voltage ($V_{TH,H}$) and to correct bit errors.

B. *Decoder-2 Architecture*

Proposed Decoder-2 architecture is shown in Fig. 4(a). It detects the patterns with consecutive 1s by observing three consecutive samples at the same time (S_H[n–1], S_H[n], and S_H[n+1]) instead of two in the Decoder-1 case. This allows Decoder-2 to handle larger and multiple pre-cursors and post-cursors. The outputs of Decoder-2 (L_H[n] for the positive side, and L_L[n] for the negative side) are programmable based on three types of channel profiles: (a) pre-cursor and post-cursor dominant, (b) post-cursor dominant and (c) pre-cursor dominant, as shown in the truth table in Fig. 4(b). Correct placement of the threshold voltage of the two slicers ($V_{TH,H}$ and $V_{TH,L}$) is critical in correctly estimating pre-cursors and post-cursors. An example of setting $V_{TH,H}$ for a pre-cursor and post-cursor dominant channel is illustrated in Fig. 4(c). $V_{TH,H}$ is placed below the smallest main tap (SMT) generated from the data pattern 0,-1,1,-1,0. The detailed operation of Decoder-2 for pre-cursor and post-cursor dominant channel can be understood with the following examples:

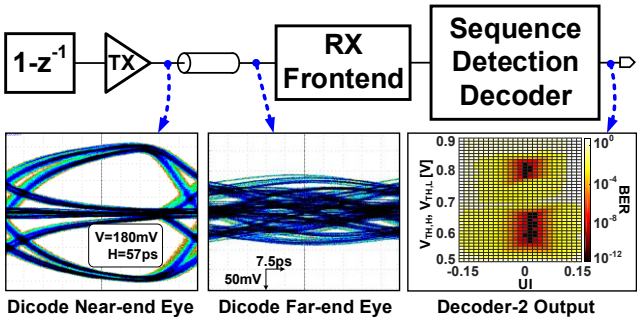
Example 1: The three consecutive slicer outputs for the positive side of the decoder are S_H[n–1]=1, S_H[n]=1, S_H[n+1]=1. The positive-side decoder detects that the only valid '1' corresponds to the main tap S_H[n]=1. S_H[n–1] and S_H[n+1] are a pre-cursor and a post-cursor, respectively, and should be '0'. Consequently, the output of Decoder-2, L_H[n], is '1'.

Example 2: The three consecutive slicer output for the positive side of the decoder are S_H[n–1]=1, S_H[n]=1, S_H[n+1]=0. The positive-side decoder detects S_H[n–1] as the main bit whereas S_H[n] as the first post-cursor. Therefore, the output of Decoder-2, L_H[n], is '0'.

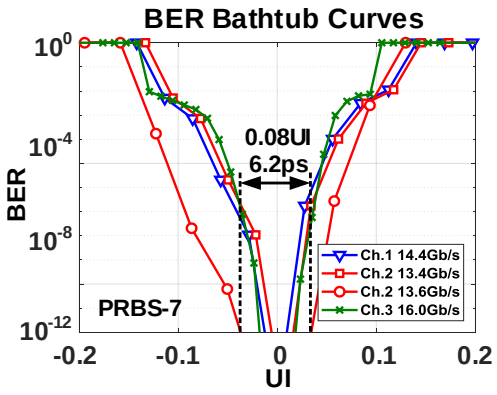


(a) (b)

Fig. 5. (a) Die micrograph. (b) Measured loss profile of channels.



(a)



(b)

Fig. 6. (a) Transmitted near-end and far-end dicode eye diagram of PRBS-7 on channel 4 at 13.4Gb/s, in-situ eye diagram of corrected output of Decoder-2 with 13.4Gb/s PRBS-7 on channel 2. (b) BER bathtub curves with PRBS-7 on channel 1, 2 and 3.

TABLE I. COMPARISON WITH STATE-OF-THE-ART TRANSCEIVERS

	This Work			[4]	Lee JSSC'08	Jeon ISSCC'18	Ramachandran ISSCC'18	Balan ISSCC'14	Musah JSSC'14	Zhong JSSC'11	Wang JSSC'10
Process [nm]	65			65	90	40	65	28	22	40	65
Encoding / Modulation	Dicode			8b10b	Duobinary	Framed-Pulsewidth	iPWM	NRZ	NRZ	NRZ	NRZ
Decoding	Sequence Detection			Viterbi	-	-	-	-	-	-	-
Decoding Latency [UI]	5			150	-	-	-	-	-	-	-
Equalization	X			X	3-tap FFE	3-tap FFE CTLE	Passive EQ	2-tap FFE CTLE 2-tap DFE	3-tap FFE CTLE 6-tap DFE	4-tap FFE CTLE 10-tap DFE	3-tap FFE CTLE 2-tap DFE
Data Rate [Gb/s]	14.4	13.6	16.0	5	20	20	16	20***	16	14.025	20
Power [mW]	34.3	34.8	42.5	44	195	90.6	50.2	130	73.6	103	87
Efficiency[pJ/bit]	2.38	2.56	2.66	10.9	9.5	4.53	3.14	6.5	4.6	7.3	4.35
Loss@Nyquist [dB]	21.6	24.2	21.4	21	10, 13	12	22	20	24	26	26
Area [mm^2]	0.135			0.35	0.32	1.056	0.13	0.166	0.079	0.97	0.07
Supply [V]	0.7/0.9/1			0.75/0.95	1.5	0.9	0.9	0.9/1.35	0.9	1.1	1.2

*: 12dB loss at 7.5 GHz. **: Includes Tx+Rx+Clock power. ***: Per lane.

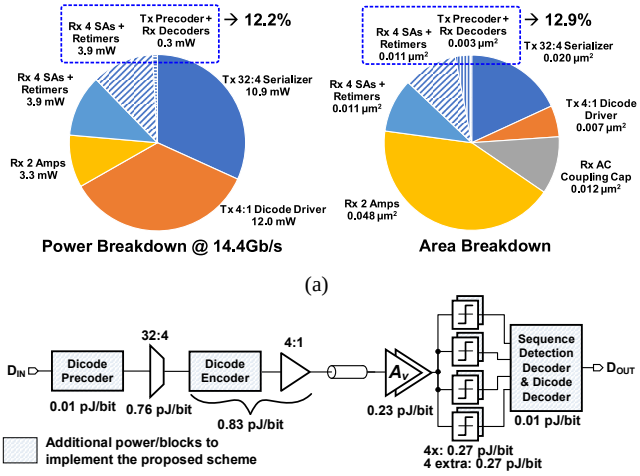


Fig. 7. (a) Power breakdown at 14.4Gb/s and area breakdown of the transceiver. (b) Transceiver architecture with additional blocks to implement the proposed encoding and decoding scheme.

IV. MEASUREMENT RESULTS

The chip was fabricated in 65nm CMOS and occupies active area of 0.135mm^2. The die micrograph is shown in Fig. 5(a). Multiple channels are used in the measurement, and their insertion loss profiles are shown in Fig. 5(b). Measured near-end, far-end, and in-situ eye diagrams of the proposed transceiver operating at 13.4Gb/s with channel 4 are shown in Fig. 6(a). Eye diagram at the receiver is completely closed due to ISI. The proposed sequence detection based decoder opens the eye as presented in the in-situ eye diagram. The BER-based in-situ eye diagram is achieved by sweeping the threshold voltage of the slicer and the clock phase of the sampler at the output of the decoder stage.

BER bathtub curves are shown in Fig. 6(b). At BER=10^{-12} the proposed transceiver achieves an eye opening of 6.2ps, operating at 13.6Gb/s compensating for 24.2dB channel loss of channel 2 by Decoder 2. Measured performance at different data rates and different channels are also presented. Operating at 14.4Gb/s on channel 1, the proposed transceiver employs Decoder 1 and achieves the best energy efficiency of 2.38pJ/bit. Operating at 16Gb/s on channel 3 the proposed transceiver can compensate for 21.4dB loss with 2.66pJ/bit efficiency. Table 1 compares the performance of the proposed transceiver with the state-of-the-art. Compared to the Viterbi-based transceiver [4], this work provides 3x higher data rate, 30x smaller decoding latency, 4x better power efficiency while compensating for 3dB more loss. The area overhead of the proposed encoder and decoder is 12.9% and the energy overhead at 14.4Gb/s is only 12.2% in addition to conventional transceiver blocks, as shown in Fig. 7.

V. CONCLUSION

This work proposed a new dicode encoding and sequence detection decoding approach as an alternative to conventional equalizers. The proposed sequence detection and correction approach has been demonstrated to be more efficient than the previously reported Viterbi decoders. The prototype wireline transceiver is fabricated in 65nm CMOS with active area of 0.135mm^2. The maximum data rate is 16Gb/s with the energy efficiency of 2.66pJ/bit with 21.4dB loss. The best efficiency is 2.38pJ/bit at 14.4Gb/s compensating for 21.6dB loss. The highest loss compensated is 24.2dB at 13.6Gb/s with 2.56pJ/bit efficiency.

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