A Switched Capacitor Multiple Input Single Output Energy Harvester (Solar + Piezo) Achieving 74.6% Efficiency With Simultaneous MPPT

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***Abstract*— This paper presents an inductor-less switched capacitor based energy harvester, which can simultaneously harvest from 2 energy sources (Solar + Piezo). The proposed harvester employs maximum power point tracking algorithm, by changing the conversion ratios of the charge pumps for piezo and solar sources, and output voltage control by varying the switching frequency. The proposed MPPT algorithm can match the input impedance of two sources simultaneously. Implemented in 65nm CMOS, the proposed harvester can generate a fixed output between 1.8 and 2.5 V output while delivering 35 μW to 70 μW power with a peak power conversion efficiency of 74.6%.**

***Index Terms*— Energy harvester, MISO, switched capacitor, MPPT, solar, piezoelectric.**

I. Introduction

HARVESTING energy from ambient energy sources is essential in extending the life of wireless sensor nodes. Ambient energy sources such as solar, thermal, vibration, and RF are not steady in nature. For instance, as the light intensity reduces, the amount of power that can be extracted from solar cells also reduces. Battery or supercapacitors are typically employed in energy harvesters to store the unused harvested energy and use it when the energy from the ambient source is absent. However, due to form factor limitation, the battery capacity is limited, as a result, during the long absence of energy from the ambient source, the battery can run out of charge, which could compromise the sensing node operation. Harvesting energy from more than one ambient source can help to increase the reliability of wireless sensors. Furthermore, harvesting from multiple ambient sources has a potential to achieve near perpetual operation of wireless sensor node even without using batteries.

To harvest from multiple energy sources, researchers have proposed several inductor based energy harvester architectures [1]–[7]. While these state-of-the-art harvesters provide good energy efficiency, they are not fully integrated. This is because the inductor used in these architectures is of the order of several 10s of micro-henry, and therefore, cannot be integrated on silicon. Switched capacitor based architectures can harvest energy without the need of an external inductor [8]–[17], and therefore, they can be fully integrated on silicon. In [18] an array of Thermo-electric generators (TEG) have been used and reconfigured to harvest energy, although this method achieves very high efficiency the two harvesting sources are of the same type (TEG). In [19] researchers proposed a fully integrated solution to harvest two energy sources, but the solutions has limited peak efficiency of 10%. Other switched capacitor architecture can only harvest from one ambient energy source at a time [13], [20], [21]. In view of this limitations, this work presents a fully integrated switched capacitor based multiple-input-single-output (MISO) energy harvester that supports maximum power point tracking (MPPT), which can simultaneously harvest from two ambient energy sources.

Source impedance and open circuit voltage of different ambient energy sources are different. This creates impedance matching and energy combining challenges for a MISO harvesting system. The two key contributions of this work are: (1) Achieving simultaneous impedance matching of two different energy sources, whose impedance could be different by more than 4×. (2) Achieving the output voltage $V_{OUT} \geq V_{REF}$ while simultaneously boosting voltage from one ambient source, attenuating the voltage from the other ambient sources and combining energy from both of them. Designed in 65nm CMOS, the proposed harvester can track the input impedances, which are apart by 4.3× (96 kΩ) and can perform maximum power point tracking on both ambient energy sources simultaneously while achieving peak power conversion efficiency of 74.6% at an output voltage range of 1.8 V to 2.5 V.

This paper is organized as follows: Section II presents an overview of the proposed energy harvester architecture and the mathematical modeling of a switched capacitor MISO system. Section III presents the proposed dual input MPPT algorithm. Section IV presents the implementation details. Measured results are presented in Section V followed by conclusion in Section VI.

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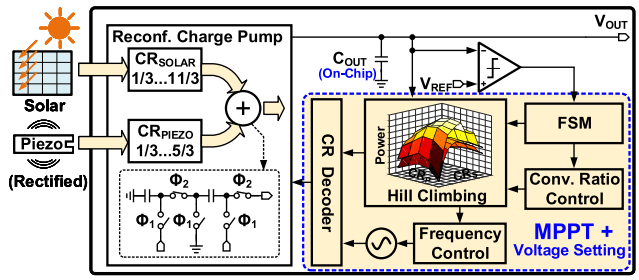

Fig. 1. Proposed multiple-input-single-output (MISO) switched capacitor based energy harvester concept with no external inductor or an external output capacitor.

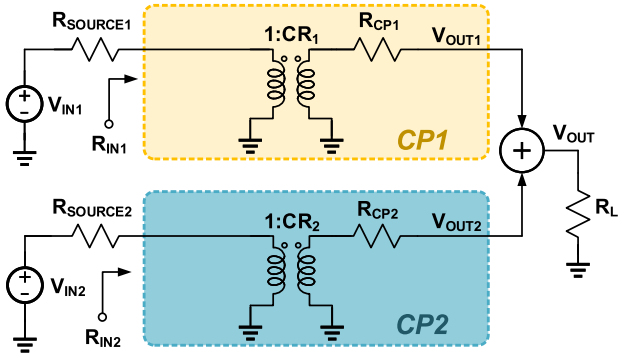

Fig. 2. Pseudo-static model of the proposed switched capacitor with dual input single output.

II. Harvester Architecture and Mathematical Model

Conventional multiple-input-single-output (MISO) energy harvester employs a buck-boost architecture with an external inductor [1]–[5]. The shared external inductor is time multiplexed among different energy sources. Maximum power transfer in a conventional inductor based harvester is achieved by adjusting the duty cycle of the clock at different time instances and energy is combined in an output capacitor.

The proposed switched capacitor based energy harvester architecture is shown in Fig. 1. The proposed harvester consists of two-phase reconfigurable charge pump, an MPPT circuit and output voltage setting logic, an oscillator, and a finite state machine. The two energy sources are independently boosted or bucked to achieve maximum power transfer at the desired output voltage. Energy from solar and piezo sources are combined by summing the voltages on to an on-chip capacitor.

A. MISO Switched Capacitor Mathematical Model

Dual input switched capacitor architecture can be mathematically modeled with the help of a pseudo-static model as shown in Fig. 2. The dual-input-single-output pseudo-static model is an extension of a single-input-single-output (SISO) switched capacitor pseudo-static model [22], [23]. The load in the proposed model is assumed to be digital logic load. The switching power of the digital logic is given as:

$$P_{OUT} = V_{OUT}^2 C f \alpha \tag{1}$$

where C is the total parasitic capacitance switched in the digital logic, f is the switching frequency of the digital logic load, α is the activity factor, and V_{OUT} is the harvester output voltage. Since C, f and α are independent of harvester output voltage, the load resistance can be written as:

$$R_L = \frac{1}{Cf\alpha} \tag{2}$$

In this model, the R_{CP1} and R_{CP2} represents the recombination loss of the charge pump 1 (CP1) and charge pump 2 (CP2) respectively, and is expressed by the following equation:

$$R_{CP1} = \sum_i \frac{(a_{c1,i})^2}{C_{1,i} f_{SW}}; \quad R_{CP2} = \sum_i \frac{(a_{c2,i})^2}{C_{2,i} f_{SW}} \tag{3}$$

where $a_{c1,i}$ represent the charge multipliers and, $C_{1,i}$ represents the unit capacitance of charge pump 1. Similarly, $a_{c2,i}$ represent the charge multipliers and, $C_{2,i}$ represents the unit capacitance of charge pump 2. Information on obtaining charge multipliers in a switched capacitor architecture can be found in [23]. The f_{SW} represents the switching frequency, and R_L is the load resistance. R_{IN1} and R_{IN2} represents the looking in impedance of the harvester. Other sources of losses are also present in any switched capacitor energy harvester. Unlike charge redistribution losses, conduction losses occur when charge transfer is incomplete, therefore it is dependent on the resistance of the switch. However, in energy harvesting applications, switching frequencies are very low and incomplete settling does not occur. Parasitic and top and bottom plate switching losses are also dependent on switching frequency. Therefore, there is an optimum frequency where charge redistribution loss and switching loss are balanced. For simplicity the model will take into account charge redistribution loss only as the switching frequency in such applications are low.

The proposed reconfigurable charge pump employs series-parallel architecture. We observed an interesting property of series parallel architecture, that is in case of series parallel architecture, the sum of squares of the charge multipliers is equal to the conversion ratio. Mathematically this can be written as:

$$\sum_i a_{c1,i}^2 = CR_1; \quad \sum_i a_{c2,i}^2 = CR_2 \tag{4}$$

where CR_1 and CR_2 are the conversion ratios of charge pump 1 and charge pump 2, respectively. Following two examples help to explain this observation:

Example 1: Fig. 3 shows the charge-pump architecture with 4/3 conversion ratio. The charge flow is shown in Fig. 3 (b) and (c) during phase Φ_1 and Φ_2, respectively. The charge multiplier vector during the phase Φ_2 can be written as

$$a_{c,i} = [1 \quad 1/3 \quad 1/3 \quad 1/3] \tag{5}$$

The values of the vector are calculated as the ratio between the charge at each capacitor and the total output charge [23]. Therefore, the sum of squares of charge multipliers is calculated as

$$\sum_i a_{c,i}^2 = 1 + \frac{1}{9} + \frac{1}{9} + \frac{1}{9} = 4/3 = CR \tag{6}$$

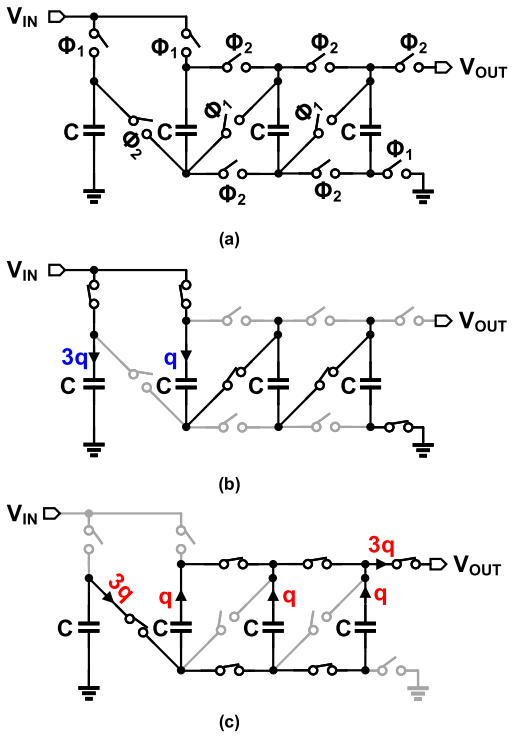

Fig. 3. (a) Series-parallel charge pump architecture with 4/3 conversion ratio. (b) Charge pump configuration during phase Φ_1. (c) Charge pump configuration during phase Φ_2.

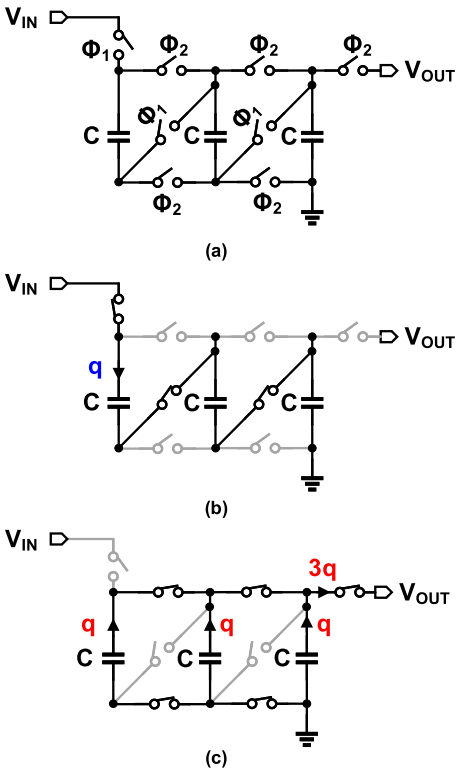

Fig. 4. (a) Series-parallel charge pump architecture with 1/3 conversion ratio. (b) Charge pump configuration during phase Φ_1. (c) Charge pump configuration during phase Φ_2.

Example 2: Fig. 4 shows the charge-pump architecture with 1/3 conversion ratio. The charge flow is shown in Fig. 4 (b) and (c) during phase Φ_1 and Φ_2, respectively. The charge multiplier vector during the phase Φ_2 can be written as

$$a_{c,i} = [1/3 \quad 1/3 \quad 1/3] \tag{7}$$

Therefore, the sum of squares of charge multipliers is calculated as

$$\sum_i a_{c,i,1/3}^2 = \frac{1}{9} + \frac{1}{9} + \frac{1}{9} = 1/3 = CR \tag{8}$$

It can be observed that in both examples equation (4) holds true. Since the unit capacitance for the charge pump 1 and charge pump 2 are same, that is $C_{1,i} = C_{2,i} = C$; $\forall$ i, Using (4), the equation (3) can be rewritten as:

$$R_{CP1} = \frac{CR_1}{C.f_{SW}}; \quad R_{CP2} = \frac{CR_2}{C \cdot f_{SW}} \tag{9}$$

B. Condition for Maximum Output Power

The proposed switched capacitor architecture operates on 2 clock phases Φ_1 and Φ_2 also known as charge and discharge phase, respectively. The energy harvested from both the ambient sources is added by connecting the capacitors of charge pump 1 in series with the capacitors of charge pump 2 during the discharging phase Φ_2. This results in the output voltage of CP1 and CP2 to be added together to create the final harvester voltage, that is $V_{OUT} = V_{OUT1} + V_{OUT2}$, where V_{OUT1} is the output voltage of charge pump 1 and V_{OUT2} is the output voltage of charge pump 2.

Since CP1 and CP2 are connected in series during Φ_2, the current flowing out of both the charge pumps is equal to I_L, where $I_L = V_{OUT}/R_L$. As a result, the effective load resistance seen by individual charge pumps are: $R_{L1} = V_{OUT1}/I_L$ for CP1 and $R_{L2} = V_{OUT2}/I_L$ for CP2. We can write V_{OUT1} and V_{OUT2} as

$$V_{OUT1} = V_{IN1} \cdot \frac{R_{IN1}}{R_{SOURCE1} + R_{IN1}} \cdot CR_1 \cdot \frac{R_{L1}}{R_{L1} + R_{CP1}} \tag{10}$$

$$V_{OUT2} = V_{IN2} \cdot \frac{R_{IN2}}{R_{SOURCE2} + R_{IN2}} \cdot CR_2 \cdot \frac{R_{L2}}{R_{L2} + R_{CP2}} \tag{11}$$

where $R_{SOURCE1}$ and $R_{SOURCE2}$ represents the source resistance of ambient source 1 and ambient source 2, respectively. For the above expression the looking in impedance of the harvester, R_{IN1} and R_{IN2}, can be expressed as:

$$R_{IN1} = \frac{R_{CP1} + R_{L1}}{CR_1^2} \tag{12}$$

$$R_{IN2} = \frac{R_{CP2} + R_{L2}}{CR_2^2} \tag{13}$$

By substituting equation (12) and (13) in equation (10) and (11), respectively, we can get the expression for R_{L1} and R_{L2}, which will be used to calculate the maximum power point. The R_{L1} and R_{L2} can be mathematically written as:

$$R_{L1} = \frac{V_{IN1}CR_1}{I_L} - R_{CP1} - CR_1^2 R_{SOURCE1} \tag{14}$$

$$R_{L2} = \frac{V_{IN2}CR_2}{I_L} - R_{CP2} - CR_2^2 R_{SOURCE2} \tag{15}$$

Using equation (10), (11), (12) and (13), the harvester output power P_{OUT} can be written as:

$$P_{OUT} = \frac{R_{L1}.(CR_1.V_{IN1})^2}{\left(R_{CP1}+R_{L1}+CR_1^2.R_{SOURCE1}\right)^2} + \frac{R_{L2}.(CR_2.V_{IN2})^2}{\left(R_{CP2}+R_{L2}+CR_2^2.R_{SOURCE2}\right)^2} \quad (16)$$

where V_{IN1} and V_{IN2} represents the voltage of ambient source 1 and ambient source 2, respectively. To estimate the condition for harvesting maximum output power, the equation (16) is partially differentiated with respect to CR_1, CR_2 and equated to zero to get the condition for the optimal CR_1 and CR_2. Expression of R_{L1} and R_{L2} from (14) and (15) are substituted in equation (16) before partial differentiation. The optimal value of CR_1 and CR_2 for achieving maximum power point can be written as:

$$CR_{1:OP} = \frac{V_{IN1} - \frac{I_L}{f_{SW}C}}{2I_L R_{SOURCE1}} \quad (17)$$

$$CR_{2:OP} = \frac{V_{IN2} - \frac{I_L}{f_{SW}C}}{2I_L R_{SOURCE2}} \quad (18)$$

At the optimal CR values, the looking in impedance of the energy harvester is closely matched with the ambient source impedance, which results in the maximum output power.

C. Condition for Maximum Output Voltage

The harvester output voltage V_{OUT} can be mathematically written as:

$$V_{OUT} = \frac{R_{L1}.CR_1.V_{IN1}}{R_{CP1}+R_{L1}+CR_1^2.R_{SOURCE1}} + \frac{R_{L2}.CR_2.V_{IN2}}{R_{CP2}+R_{L2}+CR_2^2.R_{SOURCE2}} \quad (19)$$

To achieve maximum output voltage for a given combination of CR_1 and CR_2, the equation (19) can be partially differentiated with respect to CR_1 and CR_2 and equated to zero to get the optimal CR_1 and CR_2 values. Using equations (12), (13), (14) and (15), the optimal value of CR_1 and CR_2 for achieving maximum power point can be mathematically derived as:

$$CR_{1:OP} = \frac{V_{IN1} - \frac{I_L}{f_{SW}C}}{2I_L R_{SOURCE1}} \quad (20)$$

$$CR_{2:OP} = \frac{V_{IN2} - \frac{I_L}{f_{SW}C}}{2I_L R_{SOURCE2}} \quad (21)$$

It can be observed that the optimal values of CR_1 and CR_2 for the maximum output voltage in equations (20) and (21) are exactly same as that for maximum output power in equations (17) and (18). Therefore, in the proposed switched capacitor architecture, the optimal CR_1 and CR_2 values for maximum output power are obtained by measuring the output voltage instead of measuring the output power. This design insight helped us in achieving maximum power point operation without actually sensing for the output power. Avoiding the use of expensive power sensors [24]–[26], helped us to improve the power efficiency of the harvester.

III. MISO Maximum Power Point Tracking and Output Voltage Control

The proposed harvester architecture employs 3 degrees of freedom (CR_{SOLAR}, CR_{PIEZO}, and f_{SW}) to simultaneously achieve 2 design constraints or requirements (1) maximum power point operation and (2) desired output voltage setting. The proposed MPPT algorithm searches for the optimal CR_{SOLAR}, CR_{PIEZO}, and switching frequency which achieves both these design requirements.

In this work, optimal values of conversion ratios for maximum power transfer is achieved using a hill-climbing approach. The proposed MPPT control loop and timing diagram are shown in Fig. 5(a) and (b), respectively. The MPPT consists of a clocked comparator to estimate local and global maximum power point, a hill-climbing finite state machine, CR_{SOLAR} and CR_{PIEZO} registers to digitally load/save the maximum power points during the search, and a decoder. The voltage control loop consists of a clocked comparator, frequency control, and a ring oscillator.

The pseudo code of the proposed MPPT algorithm is shown in Fig. 5(c). The algorithm searches for the peak power point for various CR_{SOLAR} and CR_{PIEZO} values. The algorithm starts by initializing the oscillator frequency and the conversion ratios to 1/3. In the first step, CR_{SOLAR} is incremented while keeping the CR_{PIEZO} fixed. The output voltage is monitored on each step. Once the output voltage reaches its maximum value, CR_{PIEZO} and CR_{SOLAR} are saved. This operating point is called the first local maximum ($Local_{MAX1}$) (see Fig. 5(b)).

In the second step, CR_{PIEZO} is incremented to the next value and CR_{SOLAR} is swept again. Once the output voltage reaches its maximum value we call that operating point as second local maximum ($Local_{MAX2}$). Since $Local_{MAX1} < Local_{MAX2}$, it can be concluded that the global maximum has not been reached so far and, therefore, CR_{PIEZO} is incremented again to next value and the procedure of incrementing CR_{SOLAR} is repeated to find the third local maximum ($Local_{MAX3}$).

If $Local_{MAX3} < Local_{MAX2}$, the algorithm concludes that the $Local_{MAX2}$ is the first global maximum ($Global_{MAX1}$). At this point, the output voltage (V_{OUT}) is compared with the reference voltage (V_{REF}). If $V_{OUT} < V_{REF}$, the algorithm is repeated by incrementing the switching frequency and reinitializing both CR_{PIEZO} and CR_{SOLAR} values to 1/3. As shown in the timing diagram, at $Global_{MAX2}$, the $V_{OUT} \geq V_{REF}$, which meets both the objectives: MPPT and desired output voltage setting. It should be noted that in the proposed harvester the range for CR_{PIEZO} and CR_{SOLAR} are 1/3 to 5/3 and 1/3 to 11/3 respectively. However, the timing diagram (Fig. 5) is using range for CR_{PIEZO} and CR_{SOLAR} to be 1/3 to 1 and 1/3 to 4/3 for simplified graphical demonstration of the algorithm.

A simulated 3D plot demonstrating power and output voltage variation with solar and piezo conversion ratio is shown in Fig. 5(d). The simulation was done using Matlab for the mathematical model shown in Fig. 2. In this simulation, the output voltage was maintained at 2.5 V to deliver a power output of 35 μW and the source impedance of the solar energy cell was 38 kΩ and the source impedance of the piezo energy cell was 94 kΩ. From the figure, it can be observed

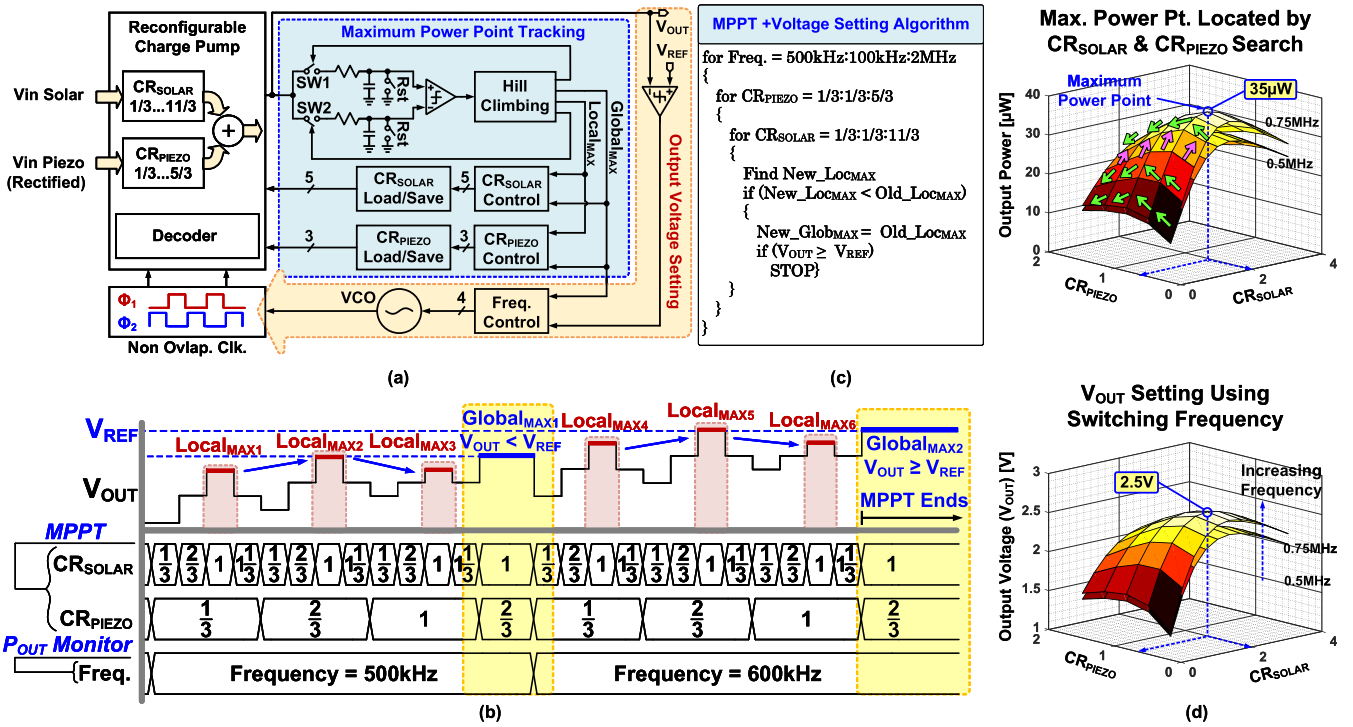

Fig. 5. (a) Proposed MPPT and output voltage control architecture. (b) Timing diagram of the proposed algorithm. (c) Pseudo code of the proposed algorithm. (d) Simulated output power and voltage versus CR_{PIEZO} and CR_{SOLAR} for two switching frequencies 0.5 MHz and 0.75 MHz.

that the global maximum are observed at CR_{SOLAR}=2 and CR_{PIEZO}=0.667. If the environmental conditions change (source power) or the load conditions (R_L) change, the MPPT must be initiated again to make sure the system is operating at its optimum efficiency point.

IV. Circuit Implementation

The implementation details for the proposed energy harvester are presented in this section.

A. Reconfigurable Switched-Capacitor Charge Pump

The detailed implementation of the two-phase reconfigurable switched capacitor architecture is shown in Fig. 6. The proposed architecture consists of two charge pumps: piezo charge pump and a solar charge pump. Both these charge pumps consist of two stages: Stage 1 and Stage 2 which provides the integer multiplication and fractional multiplication, respectively. For the solar charge pump, the first stage provides the integer conversion ratio of 1, 2, 3 and the second stage provides the fractional conversion ratio of 1/3 and 2/3. By combining both stages, the solar charge pump can have a total conversion ratio from 1/3 to 11/3. Similarly, the piezo charge pump provides a total conversion ratio from 1/3 to 5/3. Energy from solar and piezo are combined together by summing the voltages. Thanks to the voltage summation, a higher boosted output voltage can be achieved despite using smaller solar and piezo conversion ratios, which translates to fewer capacitors and small chip area. To achieve voltage summation, both solar and piezo charge pumps operate at the same frequency. Same frequency operation limits the harvester's ability to independently match the harvester impedance with the sources impedances in order to achieve maximum power point. A total of 10 MiM capacitors (50 pF each) are employed in this architecture.

An example of switch connections for $CR_{SOLAR} = 8/3$ and $CR_{PIEZO} = 4/3$ in two clock phases is shown in Fig. 6(b) and (c). During the charging phase (Φ_1), the solar fractional stage capacitors are charged to $2V_S/3$ and solar integer stage capacitors are charged to V_S. Piezo fractional stage capacitors are charged to $V_P/3$ and piezo integer stage is configured to charge to voltage V_P.

During the discharging phase (Φ_2), the solar integer and fractional stages are connected in series to get 8 $V_S/3$ ($2V_S + 2V_S/3$), as shown in Fig. 6(c). Similarly, the piezo integer and fractional stages are connected in series to get $4V_P/3$ ($V_P + V_P/3$). During this phase, the switches are configured to generate 8 $V_S/3 + 4V_P/3$ at the output.

In order to maintain good efficiency of the harvester, rail-to-rail non-overlap two-phase clocks were used to make sure switches turn on and off properly with minimum charge loss.

B. Oscillator

A five-stage digitally controlled ring oscillator is shown in Fig. 7(a). The VCO has 4-bit control (16 codes), which is decoded into coarse and fine control. The first 12 codes are used for coarse control and remaining 4 codes are used for fine control. The oscillator frequency is controlled by digitally adding or removing the capacitors at the output of inverters. In the proposed MPPT algorithm, the oscillator starts with the

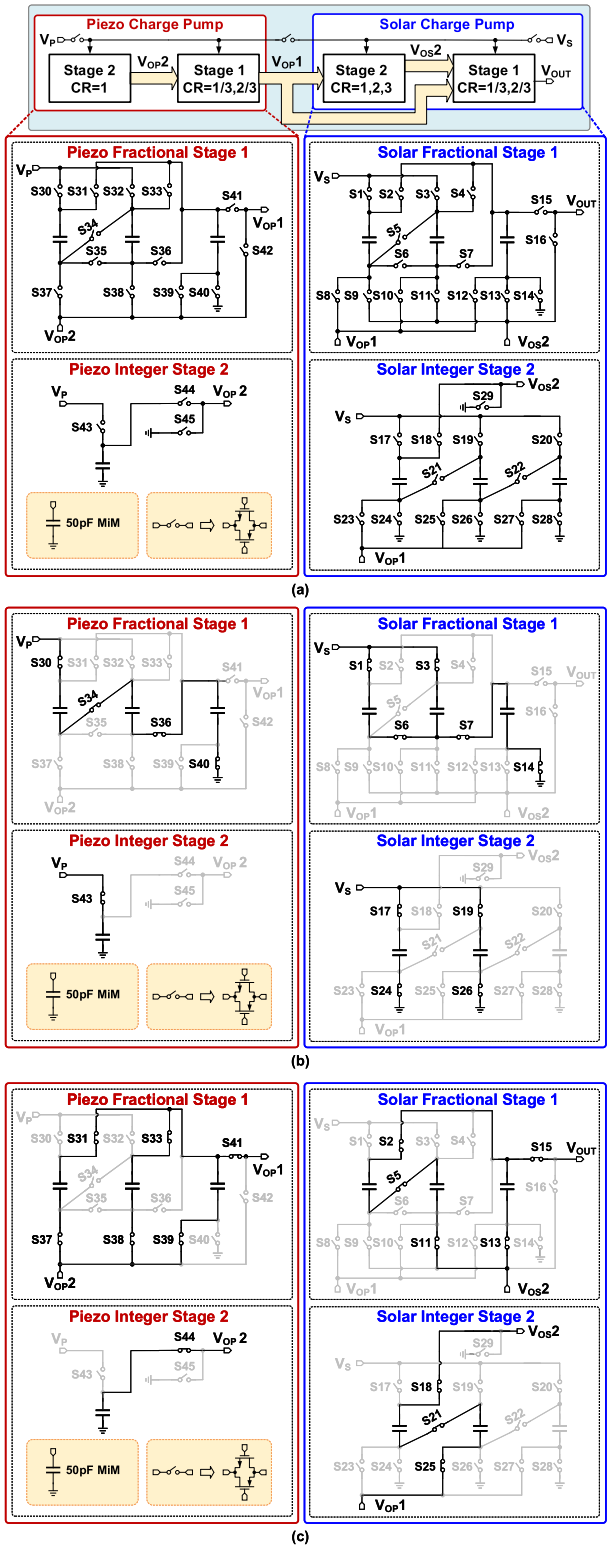

Fig. 6. (a) Proposed charge pump architecture with integer and fractional stages. (b) Charging phase (Φ_1) configuration for CR_{SOLAR} = 8/3 and CR_{PIEZO} = 4/3. (c) Discharging phase (Φ_2) configuration for CR_{SOLAR} = 8/3 and CR_{PIEZO} = 4/3.

lowest frequency of 500 kHz by connecting all the coarse and fine caps to the output of the inverters.

The coarse and fine control caps are implemented with the help of MOS capacitors. The coarse and fine caps are removed

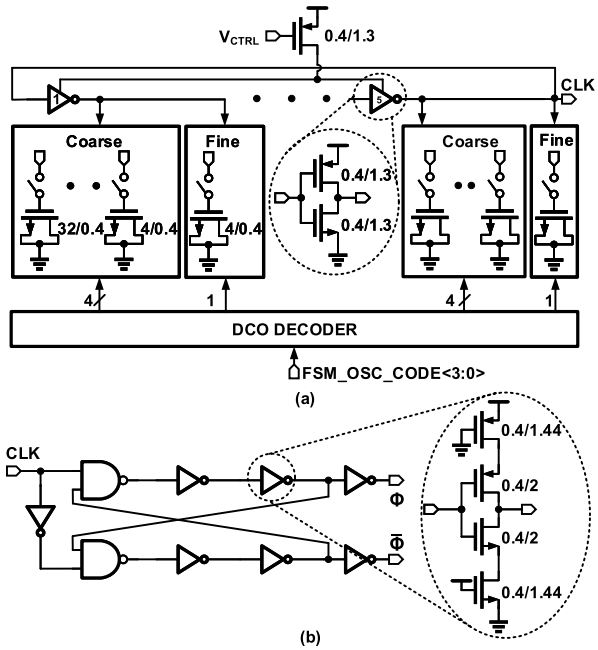

Fig. 7. (a) Digitally controlled ring oscillator. (b) Non-overlapping clock generator.

such that the frequency increases monotonically by approximately 150 kHz with each increase in code. In this work, the oscillator frequency can vary from 0.5 - 2.3 MHz (measured). A non-overlapping clock generation circuit is used to generate two clock phases, as shown in Fig. 7(b). The non-overlap time between two clock phases is approximately 2 ns (simulated).

C. Maximum Power Point Tracking Circuit

The Fig. 8 shows the schematic diagram of the maximum power point transfer circuit and the corresponding timing diagram, respectively. The MPPT circuit consists of clocked comparators to compare harvester output voltage based on current conversion ratios and previously saved conversion ratios to determine the presence of local and global maximum. A low pass R-C filter helps to filter out switching frequency ripples from the harvester output. A D-FF with the negation of output connected as a feedback to the input of the FF helps to alternate the harvester output voltage to the input of the comparator [27].

At the start of FSM, default CR_{PIEZO} and CR_{SOLAR} are loaded in the charge pump. Once the charge pump reaches steady state. The V_{OUT} is sampled on Node A or Node B to be compared with the previous steady state harvester output voltage. The sampling switches SW1 and SW2 operate in a ping-pong fashion, i.e. V_{OUT} is alternatively sampled on Node A or Node B. The comparator is enabled using CMP1 signal (from the state machine discussed in the next subsection). The output of the comparator goes to a combinational logic to generate $Local_{MAX}$ and $Global_{MAX}$ signals. If the local maximum is detected (i.e.$V_{OUT}(N) < V_{OUT}(N-1)$), the previously saved CR_{PIEZO} and CR_{SOLAR} values corresponding to the last local maximum ($Local_{MAX,N-1}$) is loaded into the charge pump to check for the existence of a global maximum.

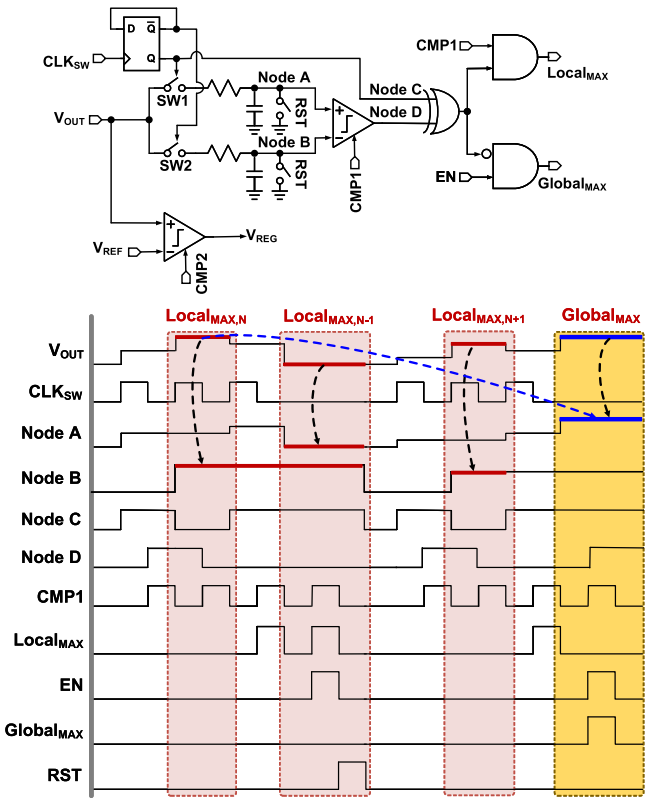

Fig. 8. Maximum power point tracking circuit and timing diagram.

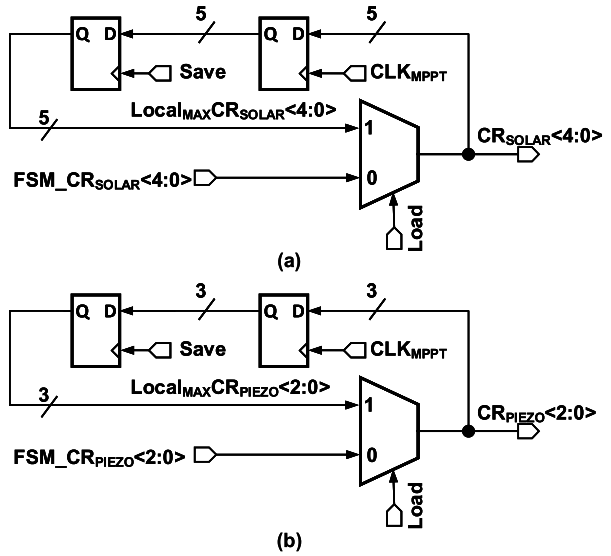

Fig. 9. Schematic of load and save registers for (a) solar conversion ratio and (b) piezo conversion.

Global maximum is detected when the output from the new local maximum is less than the output from the previous local maximum (i.e. $\text{Local}_{\text{MAX,N+1}} < \text{Local}_{\text{MAX,N}}$).

The CR_{SOLAR} and CR_{PIEZO} values for the local maximum are saved to and loaded from the registers as shown in Fig. 9 (a) and (b). The FSM_CR_{SOLAR} and FSM_CR_{PIEZO} are generated by the FSM logic and they are given to the charge pump. In the absence of global maximum, the current

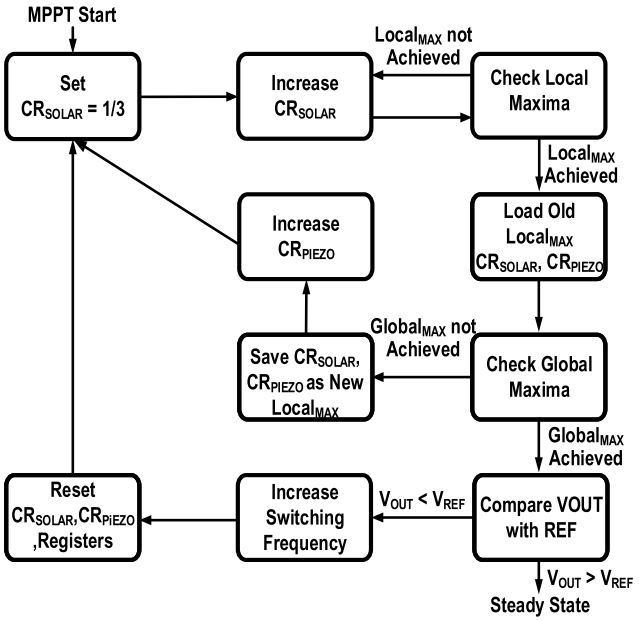

Fig. 10. Proposed finite state machine (FSM) for MPPT and output voltage setting.

conversion ratios corresponding to the local maximum are saved as Local $_{\text{MAX}}\text{CR}_{\text{SOLAR}}$ and Local $_{\text{MAX}}\text{CR}_{\text{PIEZO}}$, respectively. Control signals for the MPPT circuit and the CR_{SOLAR} and CR_{PIEZO} registers are generated by the FSM.

D. Maximum Power Point Tracking Finite State Machine

A finite state machine provides (Fig. 10) control signals for the MPPT circuit. The FSM is initiated by MPPT Start signal. The FSM starts by initializing the conversion ratios CR_{SOLAR} and CR_{PIEZO} to 1/3. In the next state, the conversion ratio CR_{SOLAR} is incremented and V_{OUT} is measured. Then the FSM checks for the presence of local maximum. Local maximum is achieved when the new harvester output voltage is less than the previous one. If a local maximum doesn't occur then the FSM jumps back to the previous state where CR_{SOLAR} is incremented. This process continues until a local maximum is observed. Once a local maximum is observed, the FSM loads the CR_{SOLAR} and CR_{PIEZO} from digital registers corresponding to the last local maximum and checks for the global maximum. Global maximum is achieved when harvester output voltage from the new local maximum is less than that of the previous local maximum. If global maximum is not detected, the FSM moves to the next state where it stores CR_{SOLAR} and CR_{PIEZO} corresponding to the current local maximum in digital registers, increase CR_{PIEZO} and repeat the whole algorithm again till global maximum is detected. Once global maximum is detected, the harvester output voltage is compared with the reference voltage to check if the desired voltage level has reached. If the output voltage is less than the reference, the FSM moves to the next state where the switching frequency is increased and it starts from the first state. This state machine stops when the desired output voltage level is achieved at the global maximum. Once a global maximum is achieved while providing an output voltage that

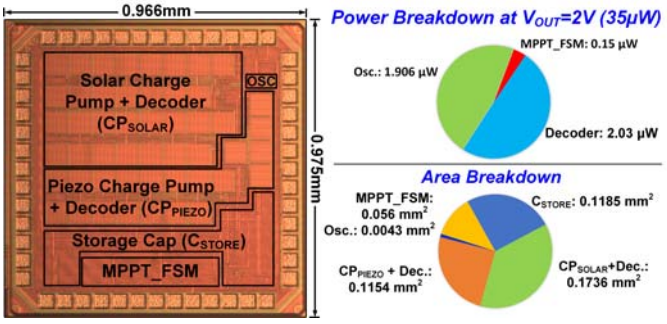

Fig. 11. Die micrograph of the proposed energy harvester, measured power breakdown at V_{OUT}=2V and area breakdown.

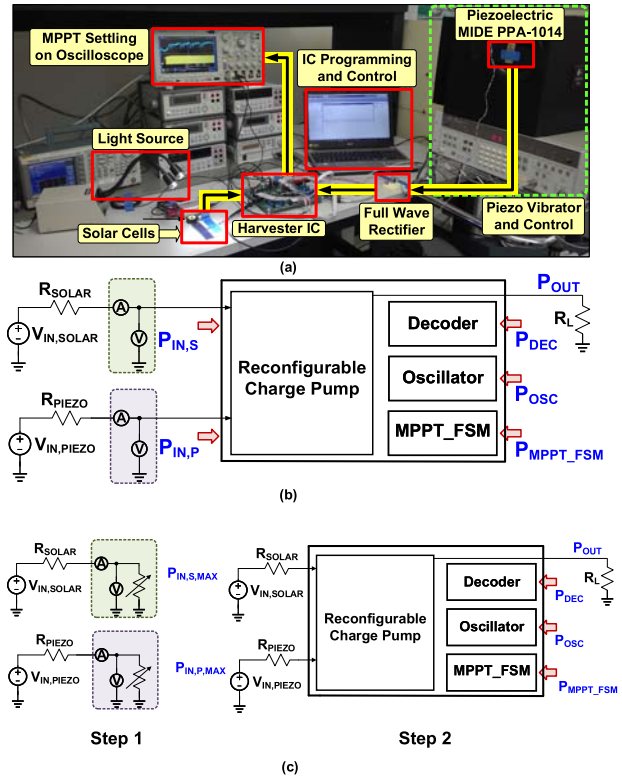

Fig. 12. (a) Energy harvester measurement setup. (b) Power measurements for power conversion efficiency (PCE) calculations. (c) Power measurements for end-to-end power efficiency ($PE_{END-to-END}$) calculations.

is larger than V_{REF}, MPPT is complete and FSM jumps to the end state.

V. Measurement Results

The proposed energy harvester was fabricated in a 65nm CMOS process and can deliver an output power from 35 μW to 70 μW, achieving peak power conversion efficiency (PCE) of 74.6%. The die micrograph, area breakdown, and power breakdown are is shown in Fig. 11. The minimum quiescent power (P_Q) dissipated in the harvester is 2.34 μW. The active area of the proposed harvester is 0.47 mm^2. The solar and piezo charge pump occupies a majority of the area. A 500 pF on-chip MOS capacitor is connected to V_{OUT}.

The measurement test setup is shown in Fig. 12 (a). Solar energy is generated by solar cells under controlled

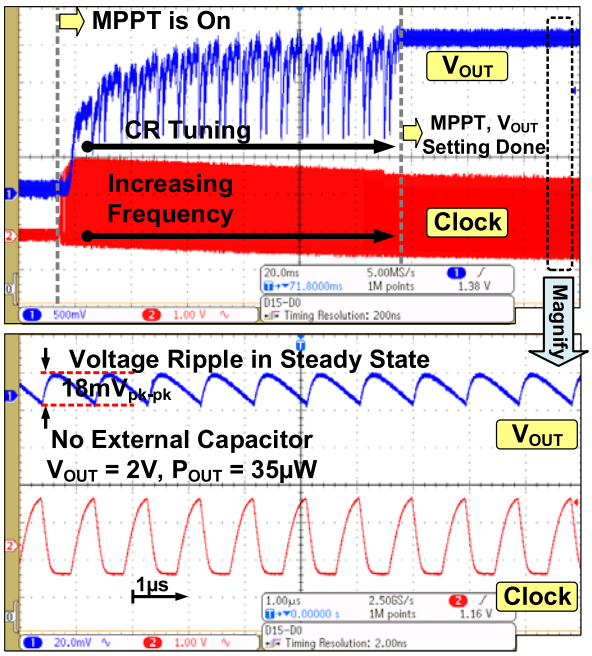

Fig. 13. Measured MPPT transient and steady state output voltage ripple.

illumination. Piezo energy is generated by vibrating an off-the-shelf piezo crystal MIDE PPA-1014 [28]. The piezo crystal is vibrated close to its resonant frequency (66 Hz) and output of piezo voltage is rectified off-chip. The rectified output is provided to the energy harvester. Due to the absence of cold start in this chip, we used an external voltage source, whose voltage is equal to the harvester output voltage (V_{OUT}) to power the oscillators, decoders, MPPT_FSM, and switch driving power. Power consumption of the external source is counted in for the calculation of power conversion efficiency.

Fig. 12 (b) shows various harvester blocks used in the power conversion efficiency (PCE) calculation. The PCE is calculated as:

$$PCE = \frac{100 * P_{OUT}}{P_{IN,S} + P_{IN,P} + P_Q}\% \quad (22)$$

$$P_Q = P_{OSC} + P_{MPPT\_FSM} + P_{DEC} \quad (23)$$

where P_{OUT} is the power dissipated in the harvester load, P_Q is the quiescent power. P_{OSC} represents the power consumed by the oscillator, P_{MPPT_FSM} represents the power consumed by the MPPT_FSM and P_{DEC} represents the power consumed by the decoders involved in the switching of the reconfigurable charge pump and it includes the power to drive the switches. $P_{IN,S}$ and $P_{IN,P}$ represents power from the solar and piezo energy sources, respectively.

Another important metric of the harvester is the end-to-end efficiency. It measures how matched is the harvester impedance to the ambient source along with the conversion efficiency of the harvester. The test setup for measuring the end-to-end efficiency is shown in Fig. 12 (c). the Power Efficiency $_{End-to-End}$ is defined as:

$$PE_{END-to-END} = \frac{100 * P_{OUT}}{P_{IN,S,MAX} + P_{IN,P,MAX} + P_Q}\% \quad (24)$$

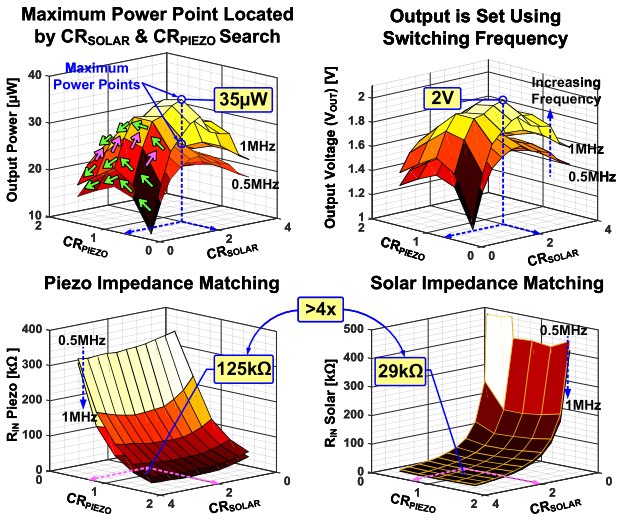

Fig. 14. Measured output power, CR_{SOLAR} and CR_{PIEZO} for $V_{OUT} = 2$ V, R_{INT} Solar $= 32$ kΩ and R_{INT} Piezo $= 82$ kΩ.

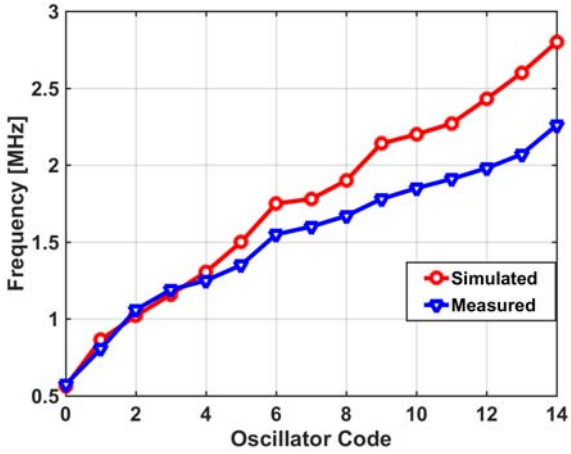

Fig. 15. Measured and simulated oscillator frequency versus oscillator digital code.

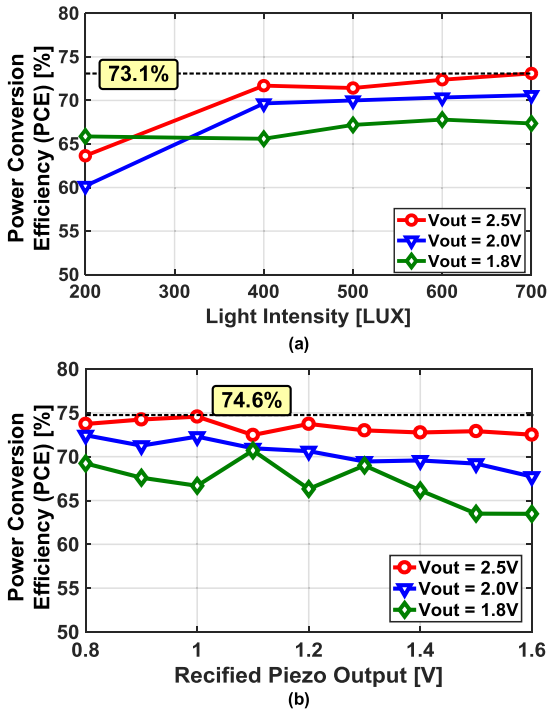

Fig. 16. (a) Measured power conversion efficiency versus light intensity. (b) Measured power conversion efficiency versus rectified piezo voltage.

where $P_{IN,S,MAX}$ is the maximum power that can be harvested from the solar energy source and $P_{IN,P,MAX}$ is the maximum power that can be harvested from the piezo energy source. P_Q is obtained from equation (23). It should be noted that due to the absence of cold-start, P_Q is externally supplied.

Measured MPPT transient during harvester start-up and during the steady state is shown in Fig. 13. The oscillator frequency starts at 500 kHz and it settles to 1 MHz after achieving maximum power transfer and setting the output voltage to 2 V. The transient dips in the V_{OUT} during the initial start-up is due to the search for local and global maximum by the MPPT logic. In the steady state, the proposed harvester achieves an output ripple of 18 mV (without using an external capacitor) while delivering 35 μW at 2 V.

Output power and the output voltage of the harvester is measured by sweeping CR_{PIEZO} and CR_{SOLAR} for 0.5 MHz and 1 MHz switching frequency and the results are shown in Fig. 14. In this experiment, the harvester achieves the maximum power output of 35 μW for $CR_{PIEZO} = 0.66$, $CR_{SOLAR} = 2$ and at a switching frequency of 1 MHz. For the same conversion ratios, the harvester achieves a peak voltage of 2 V. This result demonstrates the existence of a maximum power point as the conversion ratios are swept. This also validates the assumptions made in the proposed MPPT algorithm that the optimal conversion ratios for maximum output voltage coincides with the maximum power transfer (proved in equations (17), (18), (20) and (21))

Bottom two graphs of Fig. 14 shows the measured harvester looking-in input impedance from solar and piezo input ports. At maximum power point, the looking in impedance for piezo is 125 kΩ and looking in impedance for solar is 29 kΩ. In these measurements, the proposed harvester can match the impedance of the sources, which are apart by more than 4x. The measured input impedance of the solar and piezo source is 22 kΩ and 96 kΩ, respectively. Therefore, at the maximum power point, the proposed harvester was able to match the solar input impedance by 78% and piezo input impedance by 77%. The voltage available at the input of the solar and piezo charge pump is 1.1 V and 1.6 V respectively. The impedance matching efficiency can be improved by reducing the granularity of conversion ratios.

Oscillator frequency range is measured and simulated by digitally sweeping the oscillator frequency code and the results are shown in Fig. 15. The minimum oscillator frequency is 500 kHz at an input code of 0. The frequency can reach a maximum value of 2.3 MHz at an input code of 14. The oscillator frequency increases monotonically with the digital code.

The power conversion efficiency of the proposed harvester is measured for various light intensities and different rectified

TABLE I

PERFORMANCE COMPARISON OF THE PROPOSED HARVESTER WITH THE STATE-OF-THE-ART DESIGNS

	MISO Energy Harvesters (Different Ambient Sources)						SISO Energy Harvesters		
	This Work	Inductor Based Harvesters					Switched Capacitor Harvesters		
		JSSC'12 [1]	ISSCC'09 [3]	JSSC'16 [2]	CICC'18 [19]	JSSC'18 [7]	JSSC'16 [13]	ISSCC'16 [20]	JSSC'14 [21]
Topology	**Sw. cap**	Inductor	Inductor	Inductor	Inductor (on chip)	Inductor	Sw. Cap.	Sw. Cap	Sw. Cap.
External Inductor	**No**	Yes	Yes	Yes	No	Yes	No	No	No
Power Conversion Efficiency (%)	**74.6**	58 - 83	74.5	90	25	75	81	72	50
Power Efficiency End-to-End (%)	**70.8**	56-79.7*	N/A	87	10	N/A	N/A	68.8*	50*
Ripple (mV)	**18**	25	9.8 - 50	N/A	N/A	N/A	>100	N/A	N/A
MPPT	**Yes**	Yes	Yes	Yes	No	Yes	Yes	Yes	No
Quiescent Power/Current	**2.34 µW**	N/A	5.4 µW	N/A	N/A	240 nA	N/A	N/A	<3 nW
Min. Input (V)	**0.55**	0.02	0.068	0.05	0.085	0.1	0.45	0.5	0.14
Output Range (V)	**1.8-2.5**	1.8	0.6 - 2	1.5	N/A	3-4	3.3	1.8	2.2 - 5.2
Output Power (µW)	**35-70**	200 - 2500	78	0.025 - 100	520	450	<50	<35	5
Technology	**65nm**	350nm	250nm	180nm	28nm	180nm	180nm	180nm	180nm
Area (mm^2)	**0.47**	25	0.22	1.1	0.46	1.5	4	0.552	0.86

* Calculated from peak tracking efficiency

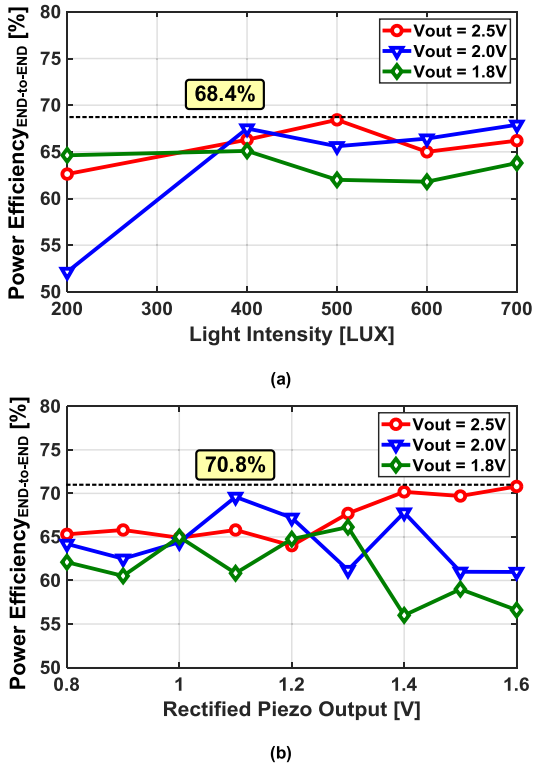

Fig. 17. (a) Measured end-to-end efficiency versus light intensity. (b) Measured end-to-end versus rectified piezo voltage.

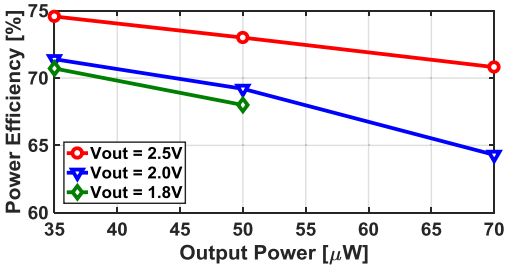

Fig. 18. Measured power conversion efficiency versus output power.

piezo (MIDE PPA-1014) voltages at three different harvester output voltage settings (1.8 V, 2 V, and 2.5 V), as shown in Fig. 16 (a) and (b). When the light is varied from 200 lux to 700 lux for fixed harvester output power of 35 μW (by varying the piezo power) and fixed output voltage of 1.8 V, 2 V and 2.5 V, the proposed harvester achieves a peak power conversion efficiency of 73.1%. When the rectified piezo voltage is varied from 0.8 V to 1.6V for a fixed output power of 35 μW (by varying solar power), the proposed harvester achieves a peak power conversion efficiency of 74.6%. We also measured the end-to-end efficiency for various light intensities and different rectified piezo voltages at three different harvester output voltage settings (1.8 V, 2 V, and 2.5 V), as shown in Fig. 17. The peak end-to-end efficiency is 70.8%.

The power conversion efficiency of the energy harvester is measured using equation (22) for different output power and output voltage settings, as shown in Fig. 18. The power conversion efficiency shown here is the peak efficiency achieved by the harvester while maintaining the necessary output voltage. At 2.5 V, the harvester can achieve a peak efficiency of 74.6%-to-70.8% while delivering an output power of 35 μW-to-70 μW. The reason power conversion efficiency is higher at 2.5 V because at 2.5 V output, less current is required to deliver the same amount of output power. Therefore, at 2.5 V we have smaller recombination loss. Moreover, when the output current is small, the switching

frequency required is less than what is needed for higher output currents, which reduces the switching losses further. Both these factors help to achieve higher efficiency at 2.5 V output. The efficiency is low for higher power levels (70 μW) because more current is delivered to the load at higher output power. Therefore, this results in higher recombination loss (due to higher current) and higher switching loss (due to higher frequency), which results in the lower efficiency. Due to constraints in the test bench to accurately measure the power conversion efficiency at lower output power, we simulated the harvester to deliver lower output power. Simulation results shows that the harvester achieves peak power conversion efficiency while delivering approximately 10 μW of output power and the power conversion efficiency drops to below 70% for output power $<$10 μW.

The performance of the proposed harvester is compared with the state-of-the-art energy harvesters as shown in Table I. The proposed switched capacitor based MISO energy harvester achieves competitive and even higher efficiency to that of prior SISO switched capacitor energy harvesters [13], [21], and it achieves comparable efficiency to that of inductor based MISO harvesters [1], [3]. While the output power range of the prototype chip is from 35 μW to 70 μW, through design choices and architectural improvements, the power range of the proposed harvester can be extended to match the output power range of inductor based harvesters.

VI. Conclusion

This work presents a new switched capacitor based energy harvester, which can simultaneously harvest from multiple energy sources. An MPPT algorithm, which can achieve maximum output power at the desired output voltage is proposed. The proposed harvester delivers 35 μW to 70 μW of output power while maintaining a constant output voltage from 1.8 V to 2.5 V at a peak power conversion efficiency of 74.6%. Future modifications to this design can be extending it to support different types of loads, introducing an energy storage feature and implement a cold-start circuit.

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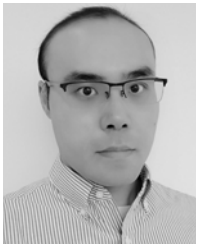

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