10.7 A 6.75-to-8.25GHz 2.25mW 190fs$_{rms}$ Integrated-Jitter PVT-Insensitive Injection-Locked Clock Multiplier Using All-Digital Continuous Frequency-Tracking Loop in 65nm CMOS

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Sub-harmonically injection locked oscillators provide a simple means for generating very-low-noise high-frequency clocks in a power, and area efficient manner [1-5]. Ideally, a free-running oscillator can be locked to the Nth harmonic of a reference clock simply by injecting narrow pulses at reference frequency (F_{REF}) into the oscillator, such that F_{OUT}=NF_{REF}. In the locked state, the oscillator tracks the reference clock and its close-in phase noise is greatly suppressed. As such, the phase noise of an injection-locked clock multiplier (ILCM) is limited only by the noise of reference clock. However, in practice, there are several design challenges that limit usage of ILCMs. First, lock-in range (ΔF_L) of the injection-locked oscillator is limited. Therefore, separate frequency tuning, typically performed using a phase-locked loop (PLL) is needed to bring the oscillator free-running frequency (F_{FR}) to be within the lock-in range, i.e., F_{ERR}= F_{FR}-NF_{REF}<ΔF_L [5]. If F_{ERR}≠ 0 (but <ΔF_L), injection ensures phase locking but causes a reference spur whose magnitude is proportional to F_{ERR} [1]. The second major challenge is the voltage and temperature (VT) sensitivity of ILCM. F_{ERR} increases as F_{FR} drifts due to VT variations, which degrades phase noise and spurious performance and may even lead to loss of lock once F_{ERR} exceeds ΔF_L [4]. This is especially problematic in the case of high-Q LC oscillators because of their relatively small ΔF_L. Techniques to extend ΔF_L by reducing N or lowering Q are undesirable as smaller N mandates higher F_{REF} and lower Q incurs a large power penalty.

Unlike in PLLs, extracting frequency-error information in ILCM is difficult. This issue is elucidated using the timing diagrams shown in Fig. 10.7.1, for the case of N=4. Jitter accumulates for the first 3 cycles, because F_{ERR}≠0 and its magnitude is proportional to both N and F_{ERR}. Reference injection in the 4th cycle resets the accumulated jitter resulting in very small phase error, $\Delta\Phi$, between the reference clock and oscillator output [1]. In [2] and [3] analog phase detector (PD) based PLLs are utilized to correct F_{ERR} by sensing this small phase difference. Due to their analog implementation, these approaches are susceptible to mismatch between injection path and PD path as well as charge-pump-current mismatch. These mismatches may cause a race condition between PLL and injection locking mechanism in addition to increasing the jitter and reference spur in the presence of VT variations [5]. Dedicated frequency-tracking loops (FTLs) reported in [1] and [4] can overcome the issue of detecting small $\Delta\Phi$. However, [4] requires two matched oscillators, which doubles both power and area. It is also not particularly suited for high-Q LC-based ILCMs because of potential pulling issues. The TDC-based approach in [1] requires a high-resolution TDC, which also incurs a large power and area penalty.

In this paper, we present a digital frequency-tracking loop (FTL) to continuously tune the oscillator free running frequency F_{FR} to be NF_{REF}. This ensures robust operation of the ILCM across PVT variations even with a very narrow lock-in range (ΔF_L<500ppm) and enables its implementation using large N and high-Q LC DCO. The prototype ILCM generates an output clock in the range of 6.75 to 8.25GHz by multiplying F_{REF} by 64 and achieves 190fs$_{rms}$ integrated jitter while consuming 2.25mW power. The timing diagram shown at the bottom of Fig. 10.7.1 illustrates the basic principle behind the proposed FTL. Because reference injection leads to a diminished phase error, $\Delta\Phi$, even in the presence of F_{ERR}, we measure $\Delta\Phi$ by disabling injection periodically. In the example shown in Fig. 10.7.1, every 4th reference edge is not injected, which results in a larger $\Delta\Phi$ that can be easily measured and used to correct F_{ERR} using a simple digital feedback loop as described next.

The block diagram of the ILCM with FTL is shown in Fig. 10.7.2. It is composed of a sub-harmonically injection-locked digitally-controlled oscillator (DCO) and an FTL implemented using a sub-sampling delay/phase-locked loop (D/PLL) in which the proportional control is implemented in phase domain using the DLL and integral control by the accumulator (ACC_I) [6]. The operation of the ILCM proceeds in the following steps. First, at start-up, F_{FR} of the DCO is coarsely tuned to be within the lock-in range of the injection-locked DCO. In the second step, the injection path is enabled, which rapidly locks DCO phase to the injected pulse (INJ). At this point, because of delay in the injection path, there is no pre-defined phase relationship between the DCO output and REF. Consequently, the resulting phase error, $\Delta\Phi$, cannot be directly attributed to the frequency error, F_{ERR}. To mitigate this, in the third step, the DLL consisting of a sub-sampling bang-bang phase detector (BBPD) and accumulator ACC_P tunes the delay of a digitally controlled delay line (DCDL) such that $\Delta\Phi$ = 0. In the final step, the integral path is enabled, which accumulates only those BBPD outputs that are generated when the injection path is gated (disabled) and drives the DCO frequency to NF_{REF}. The gating rate is made programmable and can take three values (1/2, 1/4, 1/8). At 1/8 gating rate, the tracking bandwidth reduces to 7/8th of its value when every reference edge is injected.

Figure 10.7.3 shows the schematic of the pulse generator and injection-locked DCO. The pulse generator generates a narrow pulse with programmable width using the positive edge of reference clock and injects it into the DCO using a PMOS switch. The pulse width is controlled from 20 to 35ps using a 4b pulse control word (PW). A NOR gate implements injection gating. The 16b DCO is implemented using NMOS cross-coupled pair and single-turn center-tapped inductor with a high Q (>27). This helps to reduce DCO power consumption and temperature sensitivity at the expense of smaller lock-in range. Thanks to the FTL, this can be tolerated as the DCO frequency is continuously tuned to be in the center of lock-in range. Frequency tuning is realized using two capacitor banks (8b coarse and 8b fine). The coarse capacitor bank is implemented using binary-weighted MOS capacitors to tune the frequency from 6.75 to 8.25GHz with about 6MHz step. The fine capacitor bank is implemented using minimum size devices to achieve fine resolution of 17ppm/LSB at 6.8GHz. A two-dimensional binary-to-thermometer decoder is adopted to achieve good linearity [7].

A prototype ILCM is implemented in a 65nm CMOS technology and occupies an active area of 0.25mm^2. At 6.8GHz, it consumes 2.25mW from a 0.9V supply, of which the DCO and its buffer consume less than 1.8mW. Figure 10.7.4 shows the measured phase noise for conventional ILCM and our ILCM with an initial F_{ERR} of 360ppm. Integrated jitter (10kHz to 100MHz) of conventional ILCM is 314fs$_{rms}$, which reduces to 177fs$_{rms}$ when F_{ERR} = 0. The integrated jitter of our ILCM is around 184fs$_{rms}$, independent of F_{ERR}. This indicates that FTL adds about 50fs$_{rms}$ of noise to the ILCM. The effectiveness of FTL to desensitize ILCM to voltage variations is demonstrated by measuring reference spur and integrated jitter when the supply voltage is varied from 0.88V to 1.08V. The measured F_{FR} varied by about 20MHz (~8ΔF_L) in that range. The conventional ILCM loses lock beyond 25mV supply variations, while our ILCM remains locked with the integrated jitter ranging from 180fs$_{rms}$ to 215fs$_{rms}$. The measured reference spur is around -40dBc. Figure 10.7.6 compares the measured performance of our ILCM with state-of-the-art low-jitter integer-N clock multipliers. The developed ILCM achieves excellent FoM of -251dB and the highest power efficiency of 0.33mW/GHz. The die micrograph is shown in Fig. 10.7.7.

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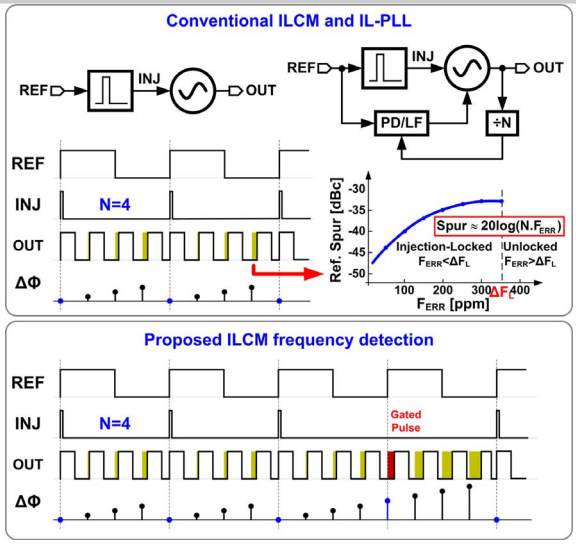

Figure 10.7.1: Illustration of the drawbacks of conventional ILCM and the concept of proposed frequency detection.

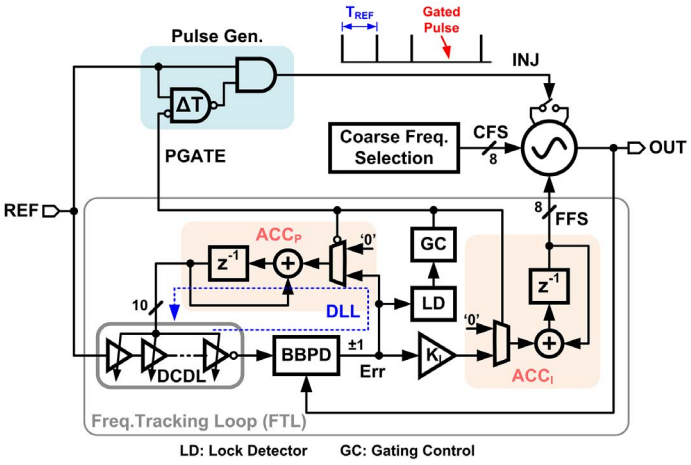

Figure 10.7.2: Block diagram of the ILCM with digital frequency tracking loop.

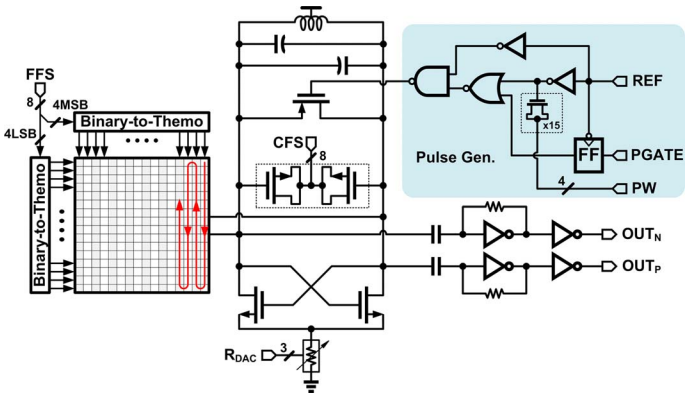

Figure 10.7.3: Schematic of pulse generator and injection-locked DCO.

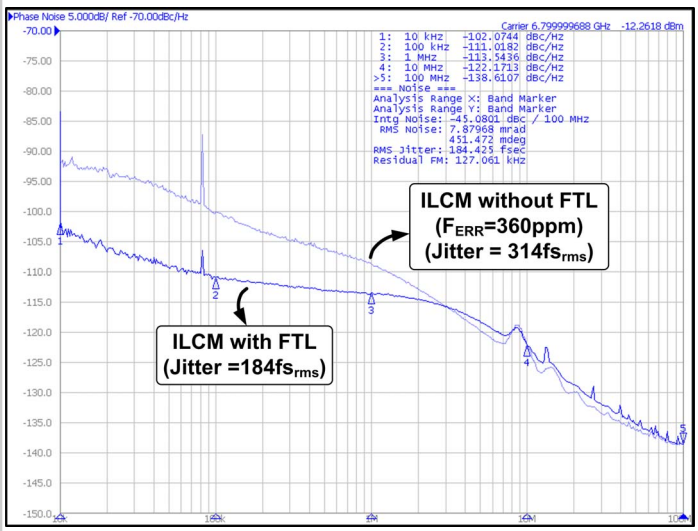

Figure 10.7.4: Measured phase noise of the ILCM with and without frequency-tracking loop (FTL) for F_{ERR} = 360ppm.

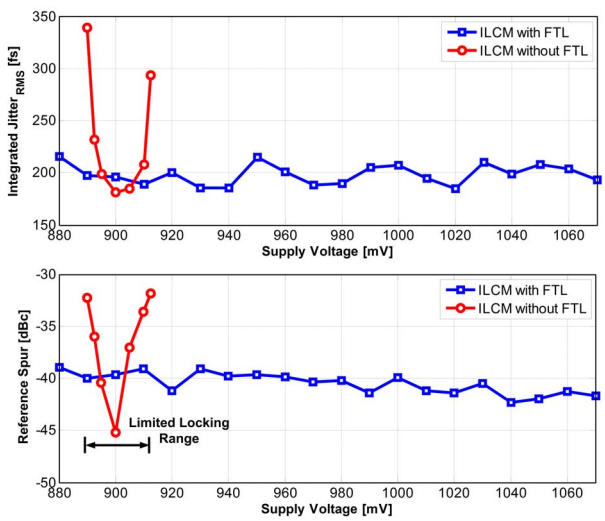

Figure 10.7.5: Measured integrated jitter (top) and reference spur (bottom) versus supply voltage.

	Helal JSSC'09 [1]	Huang ISSCC'12 [2]	Lee ISSCC'13 [3]	Musa JSSC'14 [4]	Chien ISSCC'14	This Work
Architecture	LC-ILCM	LC-ILPLL	LC-ILPLL	Ring-ILCM	PPM Ring-ILCM	LC-ILCM
Technology [nm]	130	180	65	65	20	65
Supply [V]	1.2	1.8	1.2	1.0	1.25/1.0	0.9
Output Freq. [GHz]	3.2	2.4	2.4	0.5-1.6	15	6.75-8.25
Ref.Freq. [MHz]	50	150	150	125-400	1875	105-129
Mult. Factor (N)	64	16	16	4	8	64
Ref. Spur [dBc]	-63.9	-40	-48.8	-57	-48	-40
Ref. RMS Jitter [fs]	80 [1k-20MHz]	75 [1k-40MHz]	75 [1k-40MHz]	NA	366 [100k-1GHz]	365 [10k-40MHz]
Output RMS Jitter [fs]	130 [100-40MHz]	145 [1k-40MHz]	188 [1k-40MHz]	700 [10k-40MHz]	268 [100k-1GHz]	190 [10k-100MHz]
Power [mW]	28.6	12.6	5.2	0.97	46.2	2.25
Power Eff. [mW/GHz]	**8.94**	**5.25**	**2.17**	**0.8**	**3.08**	**0.33**
FoM$_J$ [dB]	**-243**	**-246**	**-247**	**-243**	**-235**	**-251**
Freq. Tracking	**Digital (GRO-TDC)**	**Analog PLL**	**Analog SSPLL**	**Digital (VCO Replica)**	**No**	**Digital (Pulse Gating)**
Area [mm^2]	0.4*	0.64	0.25	0.022	0.044	0.25

* Use external loop filter

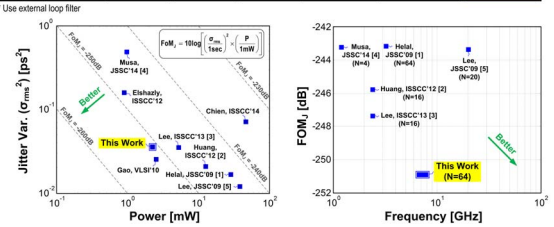

Figure 10.7.6: Performance summary and comparison with state-of-the-art designs.

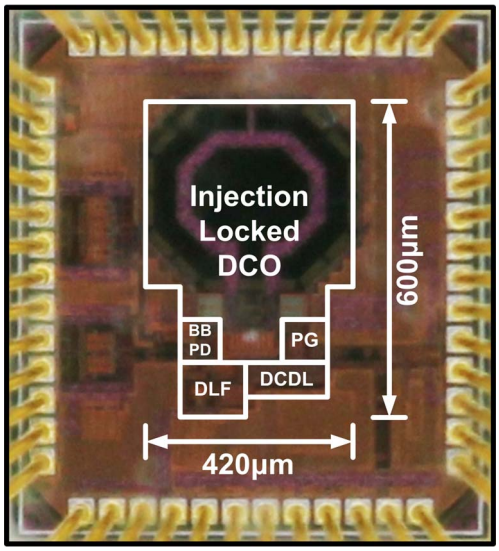

Figure 10.7.7: Die micrograph of the injection-locked clock multiplier.

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