A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC

Ahmed Elkholy, *Student Member, IEEE*, Tejasvi Anand, *Student Member, IEEE*, Woo-Seok Choi, *Student Member, IEEE*, Amr Elshazly, *Member, IEEE*, and Pavan Kumar Hanumolu, *Member, IEEE*

***Abstract*—A digital fractional-N PLL that employs a high resolution TDC and a truly $\Delta\Sigma$ fractional divider to achieve low in-band noise with a wide bandwidth is presented. The fractional divider employs a digital-to-time converter (DTC) to cancel out $\Delta\Sigma$ quantization noise in time domain, thus alleviating TDC dynamic range requirements. The proposed digital architecture adopts a narrow range low-power time-amplifier based TDC (TA-TDC) to achieve sub 1 ps resolution. By using TA-TDC in place of a BBPD, the limit cycle behavior that plagues BB-PLLs is greatly suppressed by the TA-TDC, thus permitting wide PLL bandwidth. The proposed architecture is also less susceptible to DTC nonlinearity and has faster settling and tracking behavior compared to a BB-PLL. Fabricated in 65 nm CMOS process, the prototype PLL achieves better than -106 dBc/Hz in-band noise and 3 MHz PLL bandwidth at 4.5 GHz output frequency using 50 MHz reference. The PLL consumes 3.7 mW and achieves better than 490 $\mathrm{fs_{rms}}$ integrated jitter. This translates to a $\mathrm{FoM_J}$ of -240.5 dB, which is the best among the reported fractional-N PLLs.**

***Index Terms*—Phase-locked loops (PLLs), digital PLL, ADPLL, fractional-N, fractional divider, frequency synthesizer, wide bandwidth, BBPD, DTC, LMS, TDC, time amplifier, jitter, digitally controlled oscillator (DCO).**

I. Introduction

FRACTIONAL-N phase-locked loops (PLLs) are key building blocks in many System on Chips (SoCs) and wireless transceivers [1]–[11]. Fractional-N PLLs offer flexibility in frequency planning using only a single crystal reference clock and are therefore well-suited for realizing single chip multi-standard solution in wireline applications. In all these applications, a wide PLL bandwidth is desirable as it helps improve both system- and circuit-level performance in multiple ways. For instance, it helps to improve jitter tolerance of wireline receivers [12], [13] and increase data modulation bandwidth and settling time in wireless transmitters [9], [11]. At circuit level, wide bandwidth results in: (a) larger suppression of oscillator phase noise, which helps to reduce the power, (b) better immunity to pulling [14], and (c) faster settling time. However, achieving low jitter (<1 $\mathrm{ps_{rms}}$) and wide bandwidth (2 MHz–5 MHz) using less than 50 MHz reference frequency is challenging mainly because of the presence of quantization error from feedback fractional divider and time-to-digital converter (TDC). For example, [8] suffers from degraded jitter performance when bandwidth is increased to 5 MHz due to its bang-bang phase detector (BBPD) quantization noise, while [7] relies on a high performance TDC with extensive calibration to achieve 3 MHz bandwidth at the expense of large power and area.

Analog charge-pump PLL has been the most preferred architecture to implement fractional-N frequency generation. Using bandwidth extension techniques typically based on divider quantization noise cancellation (QNC), analog PLLs were shown to achieve wide bandwidth, excellent jitter and spurious performance as reported in [9]–[12]. However, analog PLL loop filter occupies large area and is difficult to reconfigure. To overcome these drawbacks, digital fractional-N PLLs that obviate the need for large capacitors have been proposed [1]. Due to their highly digital nature, loop dynamics are easier to reconfigure and they are also easier to port from one process generation to other.

A digital fractional-N PLL is most commonly implemented using one of the two architectures depicted in Fig. 1. The main difference between the two architectures is in the way the phase error is calculated. In the so called *phase domain* PLL, phase of the oscillator is determined by counting the number of zero-to-one output transitions while the reference phase is obtained by accumulating the frequency control word on every rising edge of the synchronized reference clock [1]. A simple arithmetic logic determines the phase error by subtracting the oscillator phase from the reference phase. Because counter-based phase detection provides an estimate of the phase only with an accuracy of one oscillator period, a high resolution TDC is used to measure the residual phase error. In the architecture shown in Fig. 1(b), the feedback divider implicitly accumulates the oscillator phase and the phase error between the reference clock and the divider output is determined by using a TDC [2]. In both the architectures, a high performance TDC with sub-ps resolution

Manuscript received August 27, 2014; revised November 17, 2014; accepted December 08, 2014. Date of publication January 29, 2015; date of current version March 24, 2015. This paper was approved by Guest Editor Jeffrey Gealow. This work was supported in part by the Intel Labs University Research Office, and the National Science Foundation under CAREER EECS-0954969.

A. Elkholy, T. Anand, W.-S. Choi, and P. K. Hanumolu are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA (e-mail: elkholy2@illinois.edu).

A. Elshazly is with Intel Corporation, Hillsboro, OR 97124 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2014.2385753

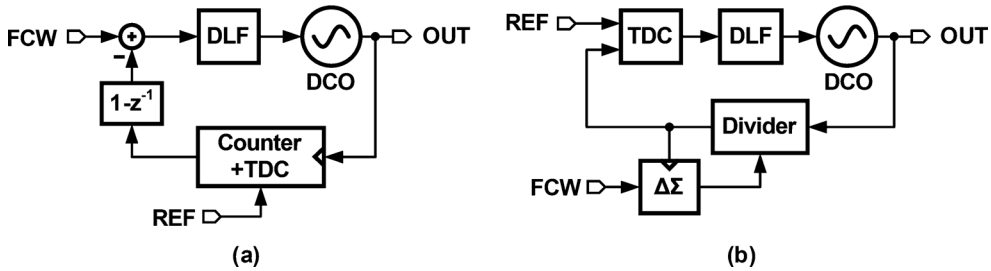

Fig. 1. Block diagram of conventional fractional-N digital PLL implementation using (a) counter-based divider-less architecture, and (b) $\Delta\Sigma$ fractional divider.

and at least one oscillator period measurement range is needed. Hence, we refer to both of them as TDC-DPLLs.

Recently, digital-to-time converter (DTC)-based DPLLs were proposed to ease the resolution requirements of the TDC [6], [15]. Based on the assumption that a high resolution DTC can be designed more power efficiently and with less hardware complexity compared to a TDC, a high resolution DTC is cascaded with a bang-bang phase detector (BBPD) to implement a fractional-N DPLL that behaves more over like an integer-N PLL [6]. However, BBPD, digitally controlled oscillator (DCO), and fractional divider introduce quantization error at different points in the loop and their contribution to output phase noise increases as with the loop bandwidth. Hence, a wide bandwidth PLL requires higher resolution TDC along with quantization noise cancellation techniques to mitigate fractional divider quantization noise, as described in Section II. In other words, digital PLLs suffer from conflicting bandwidth requirements imposed by oscillator phase noise and the quantization error introduced by the TDC and fractional divider.

In this paper, we present digital enhancement techniques to increase the bandwidth of DTC-PLLs [16]. Using a high resolution low-power time-amplifier (TA) based TDC (TA-TDC) in combination with a DTC, the DPLL achieves an in-band noise of -106 dBc/Hz and integrated jitter of 490 $\mathrm{fs_{rms}}$ at 4.5 GHz output frequency and has a bandwidth higher than 3 MHz $(\mathrm{F_{REF}}/16)$. The entire PLL consumes 3.7 mW from 1 V supply and achieves an FoM of -240.5 dB.

The rest of the paper is organized as follows. After a brief overview of state-of-the-art digital fractional-N PLLs in Section II, the proposed architecture is presented in Section III. The circuit implementation of critical building blocks is illustrated next in Section IV. The measured results from the test chip are shown in Section V. Finally, the key contributions of this work are summarized in Section VI.

II. TDC- and DTC-Based Fractional-N Digital PLLs

A TDC-based fractional-N DPLL is obtained from a conventional charge-pump fractional-N PLL by replacing the phase detector/charge-pump, analog loop filter, and VCO by TDC, digital loop filter, and DCO, respectively (see Fig. 1(b)). The TDC acts as a digital phase detector and its output is filtered by a digital loop filter and then used to control the DCO. Fractional-N operation is achieved by dithering the multi-modulus divider using a delta-sigma $(\Delta\Sigma)$ modulator. The most challenging aspect of designing a low noise, wide bandwidth, low power digital fractional-N PLL is the design of a wide dynamic range high resolution TDC. The dynamic range of the TDC must be large enough to measure the time difference between the reference clock and the dithered feedback clock. Consequently, the TDC range must at least be as large as one DCO period when the fractional divider is dithered by a first order $\Delta\Sigma$ modulator and several DCO periods for higher order modulators.

Because TDC quantization noise is low-pass filtered by the PLL's feedback loop, it limits in-band phase noise of the PLL. For instance, achieving -110 dBc/Hz in-band phase noise of a 4 GHz PLL operating with 40 MHz reference requires the TDC resolution to be less than 3 ps. Assuming second order $\Delta\Sigma$ modulator in the fractional divider, the TDC has to cover at least 2 DCO periods ($\sim$500 ps), which is very difficult to achieve in practice. Additionally, non-linearity of the TDC further exacerbates in-band noise by folding the shaped quantization noise of the $\Delta\Sigma$ divider [4]. It is also shown to introduce in-band fractional spurs that are difficult to predict and hence are difficult to suppress. The detrimental impact of TDC quantization error on in-band noise and fractional spurs increases at wider PLL bandwidth, which puts even more stringent requirements on the TDC.

The $\Delta\Sigma$ fractional divider quantization noise, $\mathrm{E_Q}$, impacts both analog and digital PLLs alike. Because $\mathrm{E_Q}$ is low-pass filtered by the PLL feedback loop, it can only be suppressed by lowering the PLL bandwidth, which is undesirable in many applications. As a result, several bandwidth extension techniques based on quantization noise cancellation (QNC) were proposed for both analog [9], [10], [17] and digital PLLs [2]. A digital QNC scheme, shown in Fig. 2, seeks to cancel $\mathrm{E_Q}$ by extracting the $\Delta\Sigma$ quantization error, scaling it with a calibrated gain and subtracting it from the TDC output [2]. The digital implementation makes this technique insensitive to analog inaccuracies and PVT variations present in analog charge-pump PLLs. However, canceling divider quantization noise after the TDC requires a high-performance wide-range TDC. Hence, high performance TDC is critical to the implementation of low noise wide bandwidth fractional-N digital PLLs. Consequently, over the past decade, significant research efforts were focused on the design of wide dynamic range, high resolution, and highly linear TDCs. Several architectures have been proposed that mimic the operation of ADCs: flash (delay line [1], vernier lines [5], parallel

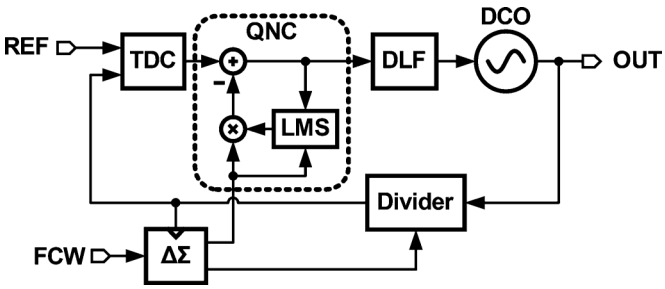

Fig. 2. Digital fractional-N PLL architecture with $\Delta\Sigma$ quantization noise cancellation (QNC).

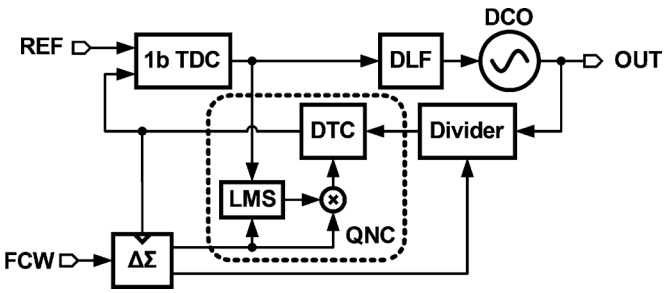

Fig. 3. A DTC-based bang-bang phase detector (BBPD) digital fractional-N PLL implementation.

delay lines [4]), two-step [18], pipelined [19], and noise shaped [2], [20]. Most of these techniques adopt analog-intensive design approaches with complex calibration schemes to achieve sub-gate delay resolution. As a result, they occupy large area and consume high power.

A DTC-based digital fractional-N PLL shown in Fig. 3 was proposed as a power efficient alternative to TDC-based PLLs [4], [6], [21]. The DTC in the feedback path is used to cancel the $\Delta\Sigma$ quantization noise at the output of the fractional divider. As a result, the TDC dynamic range requirement is relaxed. For instance, in [4], 4 bit DTC is implemented using 16-stage delay locked loop and a phase selection multiplexor to reduce E_Q by $1/16$ and consequently relax the TDC requirements to 4 bit. However, the non-linearity of the DTC caused by mismatch between delay cells and routing paths severely degrades the spurious and in-band noise performance of the PLL. To mitigate these non-linear errors, complex background non-linearity calibration technique such as those reported in [4] was employed at the expense of large area, high power, and long settling time. To overcome these drawbacks, a 10 bit DTC implemented using a digitally controlled delay line (DCDL) whose gain is accurately calibrated using a least-mean square (LMS) technique to implement a truly fractional divider was proposed in [6]. The high resolution DTC limits the input range of TDC to within the random noise range, as the reference and feedback clocks are now aligned as in the case of an integer-N PLL. Consequently, wide range requirement of the TDC is alleviated and a simple 1 bit TDC or bang bang phase detector (BBPD) was adequate [6].

A BBPD can be implemented power efficiently using a single flip-flop (FF). However, its large quantization error and grossly non-linear behavior limits its use in wide bandwidth PLLs. In [22], the non-linear dynamics of second-order BB-PLL are analyzed to find the condition for loop stability. The behavior of BB-PLLs is a strong function of loop gain and delay. If the loop gain is made large to achieve wide bandwidth, the steady-state of the BB-PLL becomes a bounded limit cycle, which manifests as undesirable fractional spurs and large peaking in the phase noise [23]. If the loop gain is reduced, BBPD operates in a random-noise limited regime and the PLL exhibits linear response. In [23], it was illustrated that there is optimal loop gain and consequently loop bandwidth that minimizes the PLL's overall noise. This optimum noise performance is usually achieved at relatively low PLL bandwidth (312 kHz in [6]). Furthermore, the gain of BBPD operating in noise-limited regime depends on the noise at its input, which not only makes the loop dynamics difficult to control but also makes the PLL bandwidth sensitive to reference clock jitter [22].

In addition to the BBPD-related issues, the non-idealities of the DTC also have significant impact on the performance of the fractional-N PLL. The integral non-linearity (INL) of the DTC causes imperfect QNC and appears as a periodic error at the BBPD input. If the magnitude of DTC INL is larger than random noise, it reduces BBPD gain and leads to an increase in the in-band phase noise and generation of spurious tones [21]. Finally, the architecture in [6] also suffers from long settling time for DTC gain calibration, as 1 bit is used only in LMS correlation. In view of these drawbacks, we propose a digital fractional-N PLL architecture that employs a narrow range high resolution TDC in addition to a truly fractional divider to achieve low jitter, wide bandwidth, and low power consumption.

III. Proposed Wide-Bandwidth Fractional-N DPLL Architecture

The block diagram of the proposed fractional-N PLL is shown in Fig. 4. It employs the proposed narrow range high resolution TA-TDC along with a DTC-based fractional divider, a programmable digital loop filter, and LC-based DCO. The TDC detects the phase difference between the reference and feedback clocks with a resolution of 1 ps and drives 4 bit digital output into a programmable digital loop filter. The filtered TDC output controls the DCO and drives it toward frequency/phase lock. The true fractional divider, implemented using a multi-modulus divider (MMD) and a DTC, generates the feedback clock input to the TDC. Because DTC alleviates the dynamic range requirement of TDC, it is designed only to have sufficiently large enough range (± 8 ps) to cover jitter in the reference and feedback clocks and the non-zero DTC INL. Leveraging time amplification techniques, sub 1 ps resolution is achieved at low power consumption [16]. The circuit implementation details of the proposed TA-TDC are provided in Section IV.A.

By using a TA-TDC in place of a BBPD, the proposed fractional-N DPLL overcomes the drawbacks of [6] discussed earlier. First, the limit cycle behavior that usually plagues BB-PLLs is greatly suppressed by the TA-TDC. Because instantaneous time difference between the reference clock and DCO output

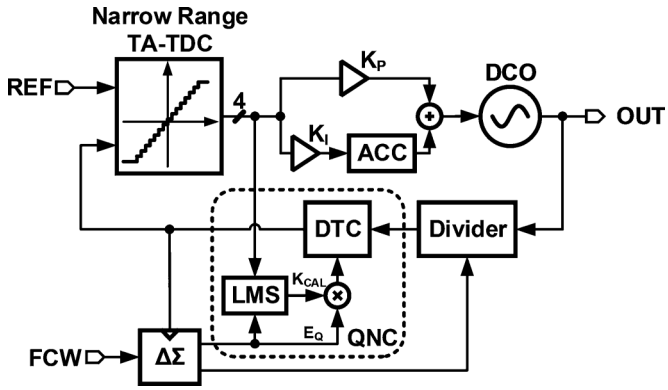

Fig. 4. Block diagram of the proposed digital fractional-N PLL.

caused by random noise is larger than TA-TDC step size, the TA-TDC's transfer characteristic is linearized and the DCO control is also scrambled. As the TA-TDC range is designed to be larger than noise induced input time difference at any moment, even a large loop gain does not saturate the TA-TDC. As a result of its linear behavior, the TA-TDC eliminates the limit cycle behavior across a wide range of loop gain (and bandwidth) settings. In other words, TA-TDC extends the random-noise limited regime of BB-PLLs by nearly the time-amplifier gain $(\mathrm{K_{TA}})$. Second, low quantization error of the TA-TDC leads to lower in-band phase noise compared to a BB-PLL. Alternatively, for the same in-band phase noise, PLL bandwidth can be extended, which relaxes DCO phase noise requirements. Third, the proposed architecture is less susceptible to DTC INL as long as it doesn't saturate the TA-TDC. Transistor-level simulations of the DTC show that its INL ($<$3 ps) can be managed to be less than TA-TDC range of $\pm$8 ps relatively easily. Fourth, because gain of the TA-TDC is independent of reference clock jitter, the proposed architecture exhibits well-controlled loop dynamics. Finally, TA-TDC improves settling and tracking behavior of the PLL by preventing slewing across a larger input time difference compared to a BBPD.

A. DTC-Based Fractional Divider

A fractional divider is realized by dithering the frequency divider between integer values using a $\Delta\Sigma$ modulator. The truncation error of the $\Delta\Sigma$ modulator appears as phase quantization error, $\Phi_{\mathrm{E_q}}$, at the output of the divider, which can be computed by subtracting the output of the $\Delta\Sigma$ from its input and accumulating it to account for the phase integration in the divider. The magnitude of $\Phi_{\mathrm{E_q}}$ depends on the order of $\Delta\Sigma$ modulator. It can be as large as one DCO period $(\mathrm{T_{DCO}})$ in case of first order $\Delta\Sigma$ modulator and several DCO periods for higher order modulators.

Phase quantization error can be cancelled at the output of MMD in time domain, which obviates the need for a high resolution TDC [6]. This can be implemented by feeding properly scaled $\mathrm{E_Q}$ into a DTC, as shown in Fig. 4. The DTC performs digital-to-time conversion and subtracts quantization error from the MMD output. As a result, this approach does not suffer from path mismatches present in analog PLLs QNC techniques [9], and is hence employed in our implementation. A key consideration in the design of DTC-based cancellation approach is the gain accuracy and non-linearity of the DTC, both of which cause quantization error leakage and degrade the spurious and noise performance of the PLL.

A DTC can be implemented using either a phase interpolator (PI) or digitally controlled delay line (DCDL). A PI-based implementation has the advantage of well defined gain but suffers from poor linearity [4], [21]. Complex digital calibration techniques are needed to correct for PI non-linearity, which often incur large power and area penalties [4]. On the other hand, DCDL-based DTC can achieve very fine resolution ($<$0.5 ps) but its gain is not well defined and sensitive to process, voltage, and temperature (PVT) variations [6], [24]. Because of its scaling friendly properties, a DCDL-based DTC is employed in our implementation. Digital background calibration is used to accurately set the DTC gain independent of PVT variations and DCO output frequency.

The DTC gain scaling factor $\mathrm{K_{CAL}}$ is computed in a background manner using a least mean square (LMS) algorithm [6]. Based on the observation that any residual phase quantization error due to imperfect cancellation appears at the TDC output, DTC gain error can be estimated digitally by correlating $\mathrm{E_q[k]}$ with TDC output as shown in Fig. 4. The accumulated digital correlator output after scaling by LMS algorithm step-size μ_{LMS}, provides $\mathrm{K_{CAL}}$. By scaling $\mathrm{E_q[k]}$ by $\mathrm{K_{CAL}}$ prior to controlling the DTC, its input range is scaled such that its output range is equal to $\mathrm{T_{DCO}}$ [6]. Once the quantization error is completely cancelled, the correlation becomes zero and the accumulator output equals the optimal $\mathrm{K_{CAL}}$ value. The LMS step-size μ_{LMS} must be carefully chosen considering the tradeoff between convergence time and $\mathrm{K_{CAL}}$ accuracy [25]. A large μ_{LMS} leads to faster convergence at the expense of larger noise in the steady-state value of $\mathrm{K_{CAL}}$. The convergence time is improved by more than an order of magnitude because of the extra error information provided by the TA-TDC.

B. DPLL System Analysis

Fig. 5 shows the discrete-time phase-domain linear model of the DPLL. The DCO is modeled as an integrator in z-domain with gain $2\pi\mathrm{K_F T_R}$, where $\mathrm{K_F}$ [Hz/LSB] is the DCO gain and $\mathrm{T_R} = 1/\mathrm{F_{REF}}$ is the reference period [26]. The fractional divider effectively divides the DCO phase Φ_{OUT} by its nominal division factor $\mathrm{N} = \mathrm{N_{int}} + \alpha$, where N_{int} and α are the integer and fractional division parts, respectively as modeled in [27]. The output of the $\Delta\Sigma$ modulator has two more components: zero-mean signal $(\mathrm{s_{DS}[k]})$, and zero-mean quantization noise $(\mathrm{q_{DS}[k]})$. The divider control is modeled as an accumulator with 2π gain factor to account for the frequency-to-phase conversion. The divider output phase Φ_{DIV} is equal to the DCO phase divided by the nominal division factor (N) after subtracting the phase due to modulus control.

The DTC delays the feedback clock by $\mathrm{DCW[k]} \times \mathrm{K_{DTC}}$, where $\mathrm{K_{DTC}}$ [s/LSB] is the DTC gain and $\mathrm{DCW[k]}$ is the DTC delay control word. So DTC can be modeled as a combination of summing block and a gain $2\pi\mathrm{K_{DTC}}/\mathrm{T_R}$. The function of

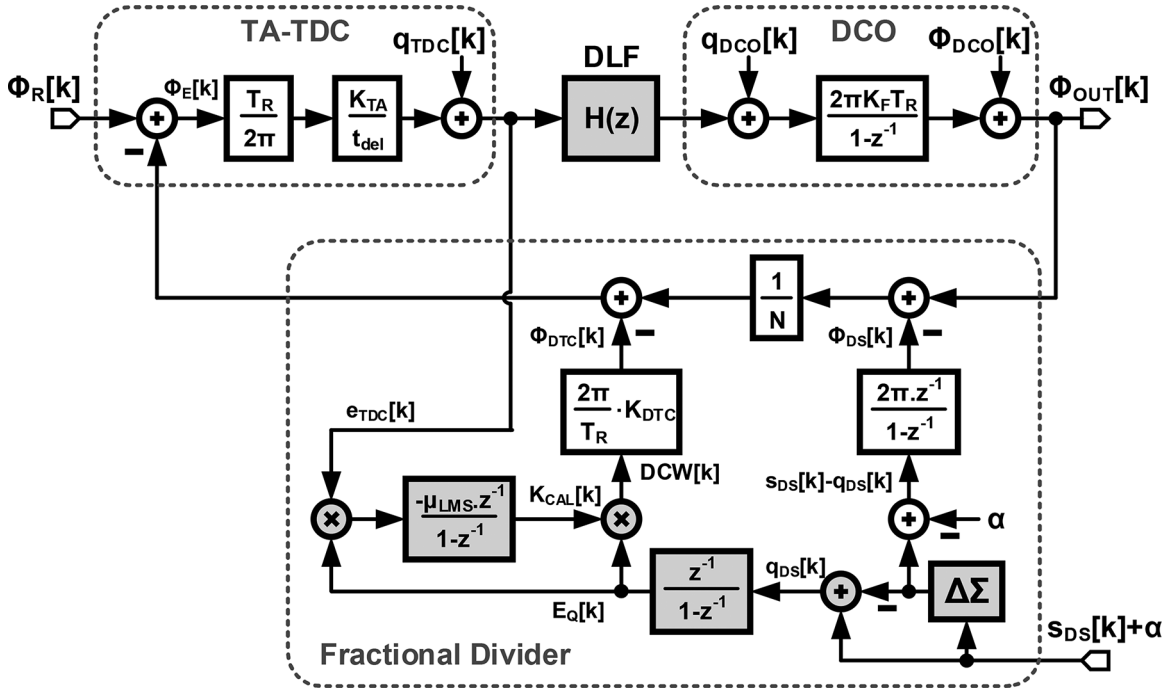

Fig. 5. Simplified discrete-time linear phase-domain model of the DPLL.

TA-TDC is modeled as a gain factor of $T_R/2\pi$ to account for phase-to-time conversion followed by a gain K_{TA}/t_{del}, where K_{TA} is the gain of the time-amplifier and t_{del} [s] is the resolution of the delay-line TDC. Finally, the loop filter is modeled by its discrete-time transfer function $H(z)$, and the loop gain transfer function can be defined as:

$$LG(z) = \frac{T_R^2\, K_{TA}\, K_F}{N\, t_{del}} \cdot \frac{H(z)}{1 - z^{-1}}. \tag{1}$$

This linear model is used for stability and noise analysis of the DPLL system. All of the noise sources in the DPLL, namely the reference phase noise, TDC quantization error, DCO frequency quantization error, and DCO phase noise are represented by their respective power spectral densities $S_{\Phi_{REF}}$, $S_{q_{TDC}}$, $S_{q_{DCO}}$, and $S_{\Phi_{DCO}}$. The total output phase noise $S_{\Phi_{OUT}}$ can be calculated using:

$$\begin{aligned} S_{\Phi_{OUT}} = &\left| \frac{2\pi\, t_{del}}{T_R\, K_{TA}} \cdot N \cdot G(z) \right|^2 S_{q_{TDC}} \\ &+ \left| \frac{2\pi\, K_F\, T_R (1 - G(z))}{1 - z^{-1}} \right|^2 S_{q_{DCO}} \\ &+ |N \cdot G(z)|^2\, S_{\Phi_{REF}} + |1 - G(z)|^2\, S_{\Phi_{DCO}} \end{aligned} \tag{2}$$

where $G(z) = LG(z)/(1 + LG(z))$. Assuming uniform distribution for the quantization error, it can be easily shown that $S_{q_{TDC}} = T_R/12$ [LSB^2/Hz]. Equation (2) shows that the in-band phase noise (IBPN) is dominated by reference and TDC noise. This emphasizes the benefit of adding the time-amplifier in order to suppress the TDC quantization noise by its gain factor K_{TA}.

Fractional divider quantization error $q_{DS}[k]$ is cancelled using DTC in the feedback path. The LMS algorithm is used to determine the optimal K_{CAL} that minimizes the mean square value of $\Phi_E[k]$ (or equivalently $e_{TDC}[k]$). When the PLL is locked, $\Phi_{OUT} = (N_{int} + \alpha) \cdot \Phi_R = N \cdot \Phi_R$, then we can write $\Phi_E[k] = \Phi_{DS}[k]/N + \Phi_{DTC}[k]$ as a function of $E_Q[k]$ and $S[k]$, where $E_Q[k]$ is the integration of $\Delta\Sigma$ quantization error $q_{DS}[k]$ and $S[k]$ is the integration of the $\Delta\Sigma$ modulator input signal $s_{DS}[k]$. Therefore $\Phi_E[k]$ is given by:

$$\Phi_E[k] = \frac{2\pi}{N}\,(S[k] - E_Q[k]) + \frac{2\pi\, K_{DTC}}{T_R} \cdot K_{CAL}[k]\, E_Q[k] \tag{3}$$

Since output period $T_{DCO} = T_R/N$ and $e_{TDC}[k] = \Phi_E[k] \cdot K_{TDC}\, T_R/(2\pi)$, where $K_{TDC} = K_{TA}/t_{del}$ is the effective TDC gain, then the TDC output is equal to:

$$\begin{aligned} e_{TDC}[k] = &\; T_{DCO}\, K_{TDC}\, S[k] \\ &- (T_{DCO} - K_{DTC}\, K_{CAL}[k]) \cdot K_{TDC}\, E_Q[k] \end{aligned} \tag{4}$$

This means the optimum K_{CAL} is equal to T_{DCO}/K_{DTC}. Based on the analysis in [25], the recursive equation of LMS algorithm is used for convergence analysis as follows:

$$K_{CAL}[k+1] = K_{CAL}[k] - \mu_{LMS}\, E_Q[k]\, e_{TDC}[k] \tag{5}$$

By substituting (4) into (5), we get:

$$\begin{aligned} K_{CAL}[k+1] = &\; K_{CAL}[k]\left(1 - \mu_{LMS} K_{TDC} K_{DTC} E_Q^2[k]\right) \\ &+ \mu_{LMS} K_{TDC} T_{DCO}\left(E_Q^2[k] - E_Q[k] S[k]\right) \end{aligned} \tag{6}$$

Assuming $K_{CAL}[k]$ and $E_Q[k]$ are independent, then the expectation $E\{K_{CAL}[k]\, E_Q^2[k]\} = E\{K_{CAL}[k]\} \cdot E\{E_Q^2[k]\}$, where $E\{E_Q^2[k]\}$ is the variance σ_{EQ}^2 of $E_Q[k]$. Since $E_Q[k]$

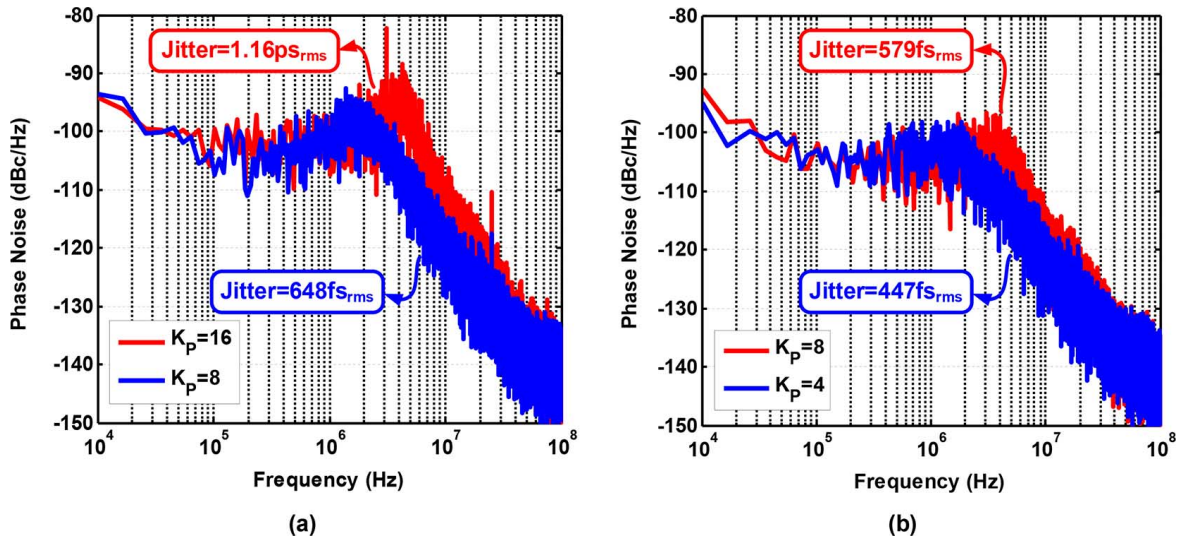

Fig. 6. Simulated output phase-noise spectrum, 5.003 GHz output using 50 MHz reference, with different proportional gain settings for (a) conventional BBPD, and (b) proposed narrow range TA-TDC.

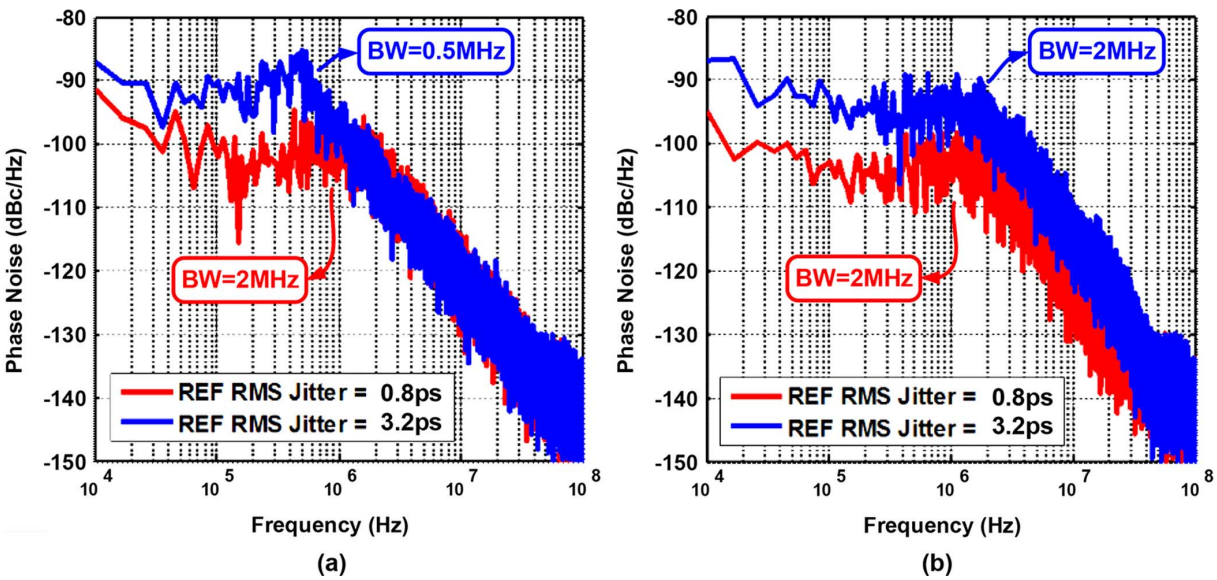

Fig. 7. Simulated output phase-noise spectrum, 5.003 GHz output using 50 MHz reference, with different reference noise jitter for (a) conventional BBPD, and (b) proposed narrow range TA-TDC.

and $\mathrm{S[k]}$ are uncorrelated, then $\mathrm{E\{E_Q[k]\,S[k]\}} = 0$ and the expectation $\mathrm{E\{K_{CAL}[k+1]\}}$ is given by:

$$\mathrm{E\{K_{CAL}[k+1]\}} = \mathrm{E\{K_{CAL}[k]\}} \times \left(1 - \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma^2_{\mathrm{EQ}}\right) + \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{T_{DCO}}\,\sigma^2_{\mathrm{EQ}} \tag{7}$$

So the solution will be in the form of $\mathrm{K_{CAL}[k+1]} = \mathrm{K_{CAL}[0]} \cdot (1 - \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma^2_{\mathrm{EQ}})^{\mathrm{k}}$, which means to guarantee loop stability μ_{LMS} has to satisfy $0 < \mu_{\mathrm{LMS}}\,\mathrm{K_{TDC}}\,\mathrm{K_{DTC}}\,\sigma^2_{\mathrm{EQ}} < 2$.

C. Performance Comparison

Time domain mixed-signal simulations were performed to compare the performance between the proposed TA-TDC- and BBPD-based PLLs. In all the simulations reference clock frequency is equal to 50 MHz and output frequency is 5.01 GHz. The phase noise of the reference clock and the DCO at 1 MHz offset are -150 dBc/Hz and -107 dBc/Hz, respectively. The simulated output phase noise plots of the BB-PLL with a bandwidth of 2 MHz and 4 MHz are shown in Fig. 6(a). Peaking in the phase noise plot caused by limit cycle behavior is clearly visible and as expected is more pronounced in the wider bandwidth case. The simulated output phase noise plots of the proposed PLL for two different bandwidth conditions are shown in Fig. 6(b). Because of its linear loop dynamics, no peaking was observed and the integrated jitter is about 0.45 $\mathrm{ps_{rms}}$ and 0.58 $\mathrm{ps_{rms}}$ for a bandwidth of 2 MHz and 4 MHz, respectively. At 4 MHz bandwidth condition, this represents an improvement of more than $2\times$ compared to the BB-PLL.

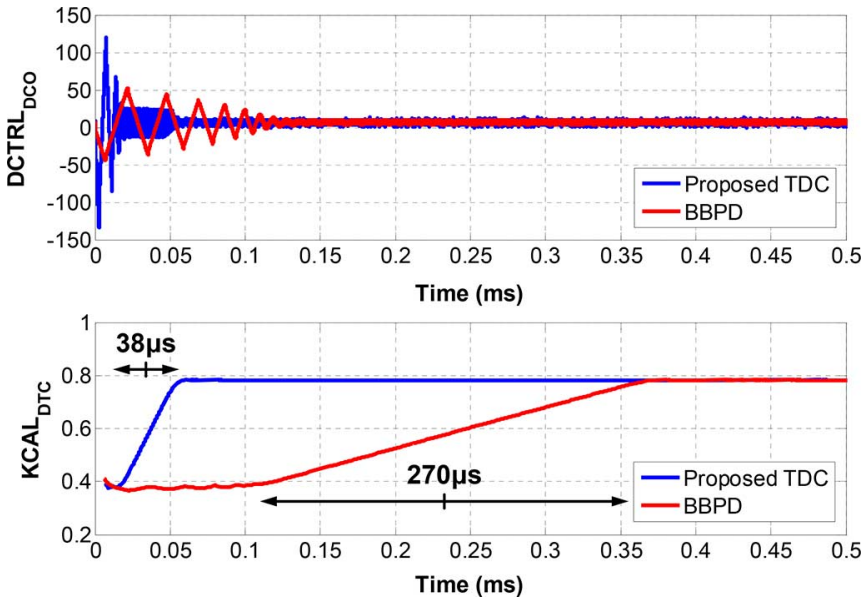

Fig. 8. Simulated settling behavior of (a) DCO control word and, (b) DTC calibration factor.

Sensitivity of loop bandwidth to reference clock jitter is quantified by plotting the output phase noise for two different clock jitter conditions (see Fig. 7). Because BBPD gain is inversely proportional to input jitter, loop gain and hence the loop bandwidth reduces from 2 MHz to about 0.5 MHz when the input jitter is increased from 0.8 $\mathrm{ps_{rms}}$ to 3.2 $\mathrm{ps_{rms}}$. On the other hand, the gain of the TA-TDC is independent of input jitter and as a result the bandwidth remains almost constant even when the reference clock jitter is varied.

The settling behavior of the proposed PLL is compared to the BB-PLL in Fig. 8. Shown on the top is the settling of DCO control word when the PLLs are started with an initial phase offset of 750 ps. As the phase error accumulates beyond the random noise limited regime, the BBPD slews, which greatly increases the settling time. On the other hand, the proposed PLL achieves lock in shorter time due to the higher gain and wider range of the TA-TDC. Using the output of the TA-TDC in LMS DTC gain calibration loop improves the convergence time, compared to BBPD. As shown in Fig. 8, $\mathrm{K_{CAL}}$ settles in about 270 μs in case of BBPD which reduces to about 38 μs when the TA-TDC is employed. In both cases, the LMS step-size parameter μ_{LMS} is set to achieve the same mean squared error in $\mathrm{K_{CAL}}$. This speed improvement is attributed to the improved LMS correlation process using multi-bit error signal.

IV. Building Blocks

A. TA-TDC

Time amplification provides an attractive alternative to implement high resolution TDCs [18], [28]. Similar to a voltage amplifier in pipelined ADCs, time-amplifier (TA) amplifies the time residue to enhance the resolution of pipelined TDCs. For instance, TA is employed in a two-step TDC in [18] and a sub-exponent TDC in [28]. However, the requirement for accurate amplification gain ($\mathrm{K_{TA}}$) in these architectures limits their practical usage in a high performance fractional-N PLL. In view of this, we propose a one-step TA-based TDC whose performance does not directly depend on $\mathrm{K_{TA}}$.

The block diagram of the proposed narrow range high resolution TDC is shown in Fig. 9. It consists of a time-amplifier (TA) that amplifies the input time difference by a gain of $\mathrm{K_{TA}}$ and a conventional flash TDC that digitizes the TA output into 4 bits. The flash TDC is implemented using a 3-state phase frequency detector (PFD) followed by a 4 bit delay line based TDC that quantizes the phase difference between the UP and DN outputs of the PFD with a resolution of one inverter delay $\mathrm{t_{del}}$. Because minimum inverter delay is about 12 to 15 ps in 65 nm CMOS technology, $\mathrm{K_{TA}}$ must be equal to 16 to achieve 1 ps resolution for the entire TA-TDC. With 4 bit output the linear range of the TA-TDC is equal to ± 8 ps.

The TA shown in Fig. 10 is similar to the $2\times$ gain stage reported in [28]. This fully-symmetric architecture consists of cross-coupled inverters wherein each inverter has two pull-down paths (main and dependent) to discharge the output node. Early input makes the late input of the cross-coupled inverters slower by reducing the strength of the dependent path, resulting in an amplified time difference. The strength of the dependent path is made programmable to achieve gain ranging from $1\times$ to $16\times$ using the 5 bit input control word, $\mathrm{D_{TA}}$. The linear input range of the TA is determined by the fall time of cross-coupled inverters and can be easily designed to achieve higher than ± 50 ps linear input range. However, increased linear range comes at the expense of more noise. Post-layout phase noise simulations of the TA indicate a noise floor better than -160 dBc/Hz at 50 MHz reference clock. Transient noise simulation shows less than 10 $\mathrm{fs_{rms}}$ input-referred jitter. Monte-Carlo post-layout simulation results show the standard deviation of the input referred time offset is around 0.75 ps. Beyond the linear range, the TA gain will drop gradually to

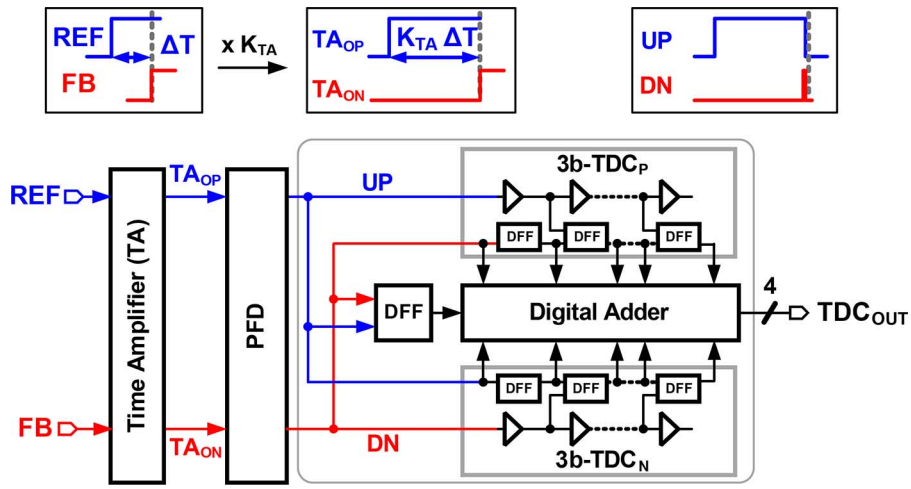

Fig. 9. Bock diagram of the proposed narrow range time-amplifier based TDC.

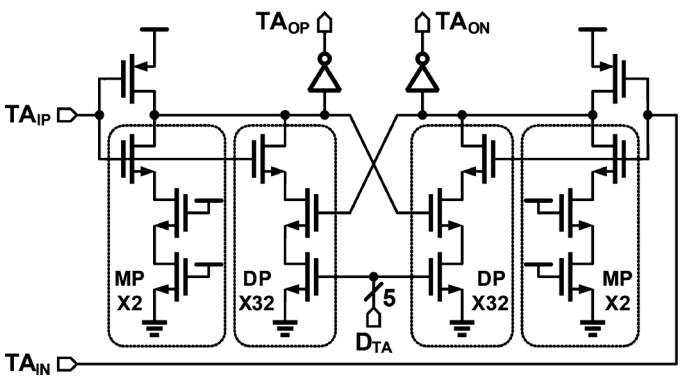

Fig. 10. Schematic of the proposed fully-symmetric time-amplifier (TA).

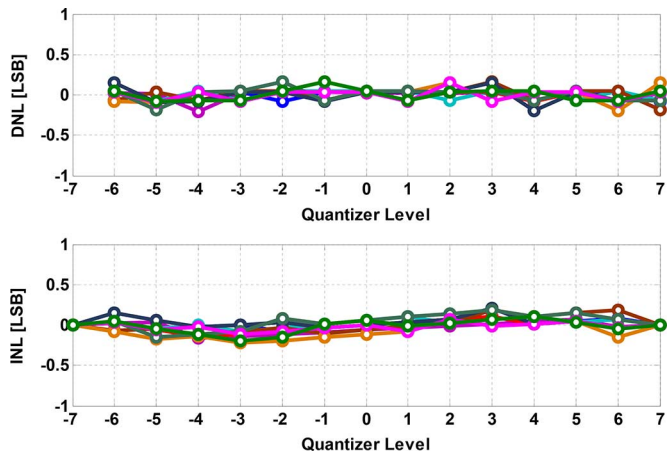

Fig. 11. Monte-Carlo post-layout simulated DNL and INL of TA-TDC: DNL [0.2 LSB] and INL [0.25 LSB].

reach unity, as the dependent path will be switched-on during transition. As a result, the TA will function as a buffer during the PLL settling process and will not impact the operation.

A 4 bit TDC is implemented using delay line TDC architecture [1]. The TDC is designed to have fully-symmetric characteristics with zero input referred time offset. Two identical 3 bit TDCs, $\mathrm{TDC_P}$ and $\mathrm{TDC_N}$, digitize $\mathrm{T_{UP}-T_{DN}}$ and $\mathrm{T_{DN}-T_{UP}}$, respectively. The difference between $\mathrm{TDC_P}$ and $\mathrm{TDC_N}$ outputs yields the magnitude of the input time difference, while a separate BBPD determines the sign. The final TA-TDC output ranges from -7.5 to $+7.5$ with a step size of 1, which allows the PLL to lock without phase offset. This will assure that TA operates in the center of its linear range in steady state. Each of the 3 bit TDCs is implemented using a conventional 7-stage inverter-based delay line in addition to 7 BBPDs as time quantizers. The TDC resolution is equal to one inverter delay, which is about 15 ps in 65 nm technology. TDC nonlinearity is reduced by making rise/fall times small and matching $\mathrm{t_{LH}}$ and $\mathrm{t_{HL}}$ propagation delays.

Non-linearity of the TA-TDC is a result of the non-linearity introduced either by the TA or TDC. Quantization noise cancellation in the DTC greatly reduces the input range of the TA-TDC. As a result, linearity requirements of the TA are greatly alleviated. The non-linearity of TDC resulting from systematic and random offsets of BBPDs in the TDC is minimized by using sense-amplifier based DFFs similar to [28]. High gain of the TA further suppresses non-linear errors of the TDC when referred to the TA input. Monte-Carlo post-layout simulation results show the standard deviation of BBPD input referred time offset is less than 0.35 ps. Fig. 11 shows Monte-Carlo simulation results of the linearity performance of the entire TA-TDC (post-layout). The DNL and INL are 0.2LSB and 0.25LSB, respectively. TA-TDC performance summary and comparison to state-of-the-art high resolution TDCs are shown in Table I. The proposed architecture leverages a high gain TA and simple TDC architecture, to achieve sub-1 ps resolution at low power consumption.

The simulated gain variation of the TA-TDC across PVT variations is $\pm 25\%$. This variation will impact the loop gain of PLL and DTC calibration loop. The LMS step size (μ_{LMS}) is chosen to guarantee loop convergence as explained in Section III.B. If the variation of PLL bandwidth resulting from TA-TDC gain variations is high, bandwidth calibration techniques reported in [29], [30] can be used to overcome the variations.

TABLE I
TDC PERFORMANCE SUMMARY

	This Work	Lee [33] JSSC'08	Vercesi [34] JSSC'10	Zanuso [4] JSSC'11	Kim [35] JSSC'13	Kim [19] JSSC'14
Architecture	TA+DL	Two-step	2D Vernier	Flash	Two-step	Pipelined
Technology [nm]	65	90	65	65	65	65
Supply [V]	1	1	1.2	1.2	1.2	1.2
F_s [MS/s]	50	10	50	40	200	250
N_{bits}	4	9	7	4	7	9
Resolution [ps]	0.9	1.25	4.8	3	3.7	1.1
DNL [LSB]	0.2	0.8	1	0.5	0.9	0.6
INL [LSB]	0.25	3	3.3	0.5	2.3	1.7
N_{linear} [bits]*	3.68	7	4.9	3.41	5.28	7.57
Power [mW]	0.2	3	1.7	8	3.6	15.4
FoM**	0.31	2.34	1.14	18.81	0.46	0.32
Area [mm^2]	0.045	0.6	0.02	0.04	0.02	0.14

*$N_{linear} = N_{bits} - \log_2(INL + 1)$, **$FoM = Power/(2^{N_{linear}} \times F_s)$ [pJ/conv.step]

B. Digitally Controlled Oscillator (DCO)

While the DTC-based fractional divider and TDC are the key elements in achieving wide PLL bandwidth, the DCO present its own design challenges to realize high performance fractional-N DPLL. In this work, we exploit a hybrid DCO approach which is realized as the combination of a DAC and a LC-VCO with a linear varactor. The schematic of the 14 bit LC DCO is shown in Fig. 12. A second order $\Delta\Sigma$ modulator truncates the 14 bit control word (D_{CTRL}) to control 5 bit thermometer-coded current DAC. A second order RC post filter suppresses the shaped quantization noise of the DAC and controls VCO varactors. The effective resolution of the DCO is around 5 kHz/LSB which is equivalent to less than 10 ppm. Unlike [6], which uses low VCO gain (K_{VCO}) of only 3 MHz/V, this design employs a K_{VCO} of 100 MHz/V to ensure that the PLL doesn't lose lock across wide range of voltage and temperature variations. However, larger K_{VCO} increases the contribution of $\Delta\Sigma$ DAC quantization noise to output phase noise. To mitigate this, the in-band quantization error of the $\Delta\Sigma$ modulator is reduced by: (a) increasing oversampling ratio of the $\Delta\Sigma$ modulator by clocking it at a frequency of $\sim$150 MHz, which is obtained by dividing the DCO output by 32, (b) using a 5 bit (as opposed to 1 bit) current-mode DAC. Unit cells in the DAC are sized to improve static linearity while dynamic non-linearity is reduced by using thermometer coding, adding a DFF in each cell, and matching clock routing. The poles of the RC filter are set to 16 MHz and 32 MHz to suppress the shaped noise with minimum impact on the PLL stability even at wide bandwidth setting of 3 MHz.

The VCO is implemented using CMOS cross coupled architecture and is optimized for low power as the phase noise requirement is relaxed by the wide loop bandwidth. The VCO core power consumption is less than 1 mA. The 1.4 nH inductor is implemented using 2 turns of top thick metal and has a simulated quality factor of 16. The output frequency is tuned from 4.4 to 5.2 GHz using two scaled banks of capacitors; 4 bit MIM capacitor bank provides the coarse control while 4 bit MOS capacitor bank provides the fine control, resulting in a nominal coarse and fine step of around 70 MHz and 10 MHz, respectively. This segmentation guarantees 50% overlap between the coarse and fine banks to cover process variations. The resolution of the fine capacitor bank is chosen to be much less than the frequency tuning by the $\Delta\Sigma$ DAC, so that the PLL locks near $\Delta\Sigma$ DAC mid range. This will allow more range for VCO temperature and supply variations after the PLL is locked.

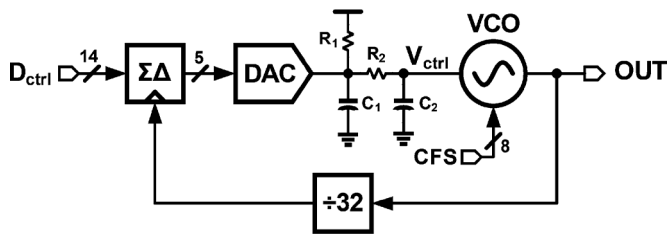

Fig. 12. LC-based DCO implementation.

C. Fractional Divider

The DCO output is divided using a 27 bit fractional divider, 7 bit integer FCW_I and 20 bit fractional FCW_F shown in Fig. 13. It is composed of a 6 stage multi-modulus divider (MMD) with extended division range from 32 to 127. The first divide-by-2/3 cell is implemented using TSPC DFFs to reduce the power consumption, while the other five cells are implemented using standard CMOS latches. The MMD is followed by a 9 bit DTC implemented using a 8 stages digitally

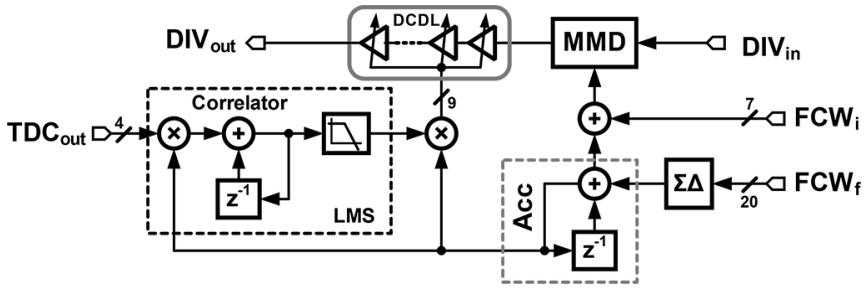

Fig. 13. Proposed truly fractional divider.

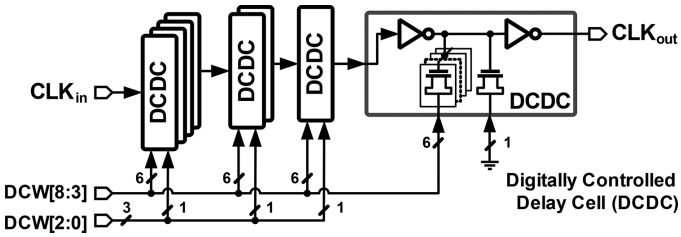

Fig. 14. The 9 bit digitally controlled delay line (DCDL) block diagram.

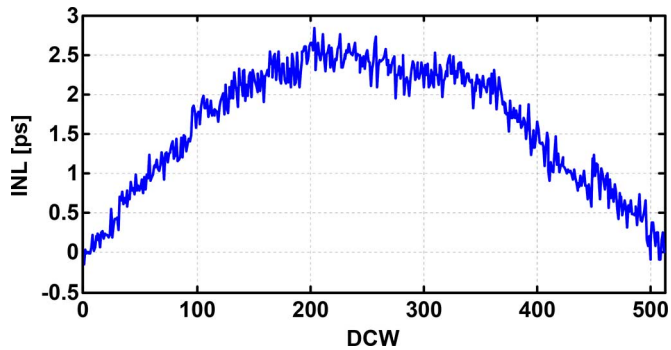

Fig. 15. Post-layout Monte-Carlo simulations for the DCDL integral nonlinearity (INL).

controlled delay line (DCDL). The 20 bit fractional word, $\mathrm{FCW_F}$, is truncated to 9 bit using second-order $\Delta\Sigma$ modulator cascaded by a 9 bit first-order $\Delta\Sigma$ modulator. First-order error feedback modulator is adopted, because it reduces the required DTC range to one $\mathrm{T_{DCO}}$ only without affecting fractional spur level [4]. Error feedback architecture simplifies the digital implementation as it provides divider control as the carry of accumulator output and accumulated quantization error $\mathrm{E_q[k]}$ as the sum output directly. The TDC output is correlated with $\mathrm{E_q[k]}$ then accumulated to find the optimum DTC scale factor. An IIR low-pass filter is used to further smooth the scale factor signal. Using a single range DTC instead of coarse-fine DTC architecture in [6] simplifies the implementation of QNC.

A 9 bit DCDL is implemented using a cascade of eight identical digitally controlled delay cells [24] shown in Fig. 14. It provides about 256 ps incremental delay, to cover the minimum operating frequency of 4.4 GHz across PVT variations. Eight delay stages are used instead of one large delay cell as in [6] to ensure fast rise and fall times and to reduce DCDL noise and sensitivity mismatches. Each delay cell consists of a CMOS inverter loaded with a tunable 64-unit capacitor bank followed by another inverter to restore fast rise and fall times. As shown in Fig. 14, the 6 MSBs of the delay control word drives 63 capacitors in all delay cells, while each of the 3 LSBs control one unit capacitor in different delay cells. Post-layout Monte-Carlo simulations shown in Fig. 15 indicate maximum INL of less than 3 ps of delay deviation, where the LSB resolution equals to about 0.5 ps.

V. Measurement Results

The proposed digital fractional-N digital PLL depicted in Fig. 16 was fabricated in 65 nm CMOS process and its die photograph is shown in Fig. 17. It occupies 0.22 $\mathrm{mm^2}$ active area, of which the proposed TA-TDC occupies only 0.045 $\mathrm{mm^2}$. The overall power consumption is less than 3.7 mW of which the TA-TDC consumes less than 0.2 mW while operating from a 1 V supply voltage. A 50 MHz external reference clock has been used in testing. It has an integrated jitter of 0.8 $\mathrm{ps_{rms}}$ and a noise floor of -147 dBc/Hz. The measured phase-noise of the digital fractional-N PLL at 4.5 GHz is shown in Fig. 18 for a conventional BBPD and the proposed TA-based TDC. Using the proposed TA-TDC, the PLL achieves an integrated jitter of 0.44 $\mathrm{ps_{rms}}$ which is $2\times$ lower than a conventional BBPD of 0.84 $\mathrm{ps_{rms}}$. This results also shows that about 9 dB in-band phase-noise improvement is achieved while using the TA-TDC.

Fig. 19 shows the measured phase-noise for different bandwidth settings, from 0.75 MHz to 3 MHz, at 4.5 GHz output. The bandwidth is controlled by changing the gain of the proportional path $\mathrm{K_p}$. Even for a wide bandwidth setting of 3 MHz ($\sim$Fref/16), no peaking or limit cycle behavior is observed in the output spectrum, and the proposed TA-TDC achieves an in-band noise of -106 dBc/Hz. At 1.5 MHz BW, an excellent integrated jitter of 0.4 $\mathrm{ps_{rms}}$ is achieved which slightly increases to 0.45 $\mathrm{ps_{rms}}$ and 0.53 $\mathrm{ps_{rms}}$ for bandwidth of 0.75 MHz and 3 MHz, respectively. For the low bandwidth setting ($\mathrm{K_p} = 2$), the DCO noise is not adequately filtered. As a result, it exceeds the in-band noise floor which should be limited by reference and TDC noise. The measured in-band noise floor is better than -106 dBc/Hz at 4.5 GHz output frequency. The measured integrated jitter is plotted as a function of output fractional frequency offset, shown in Fig. 20, indicates a worst-case jitter less than 0.49 $\mathrm{ps_{rms}}$. The slight increase in jitter at small fractional

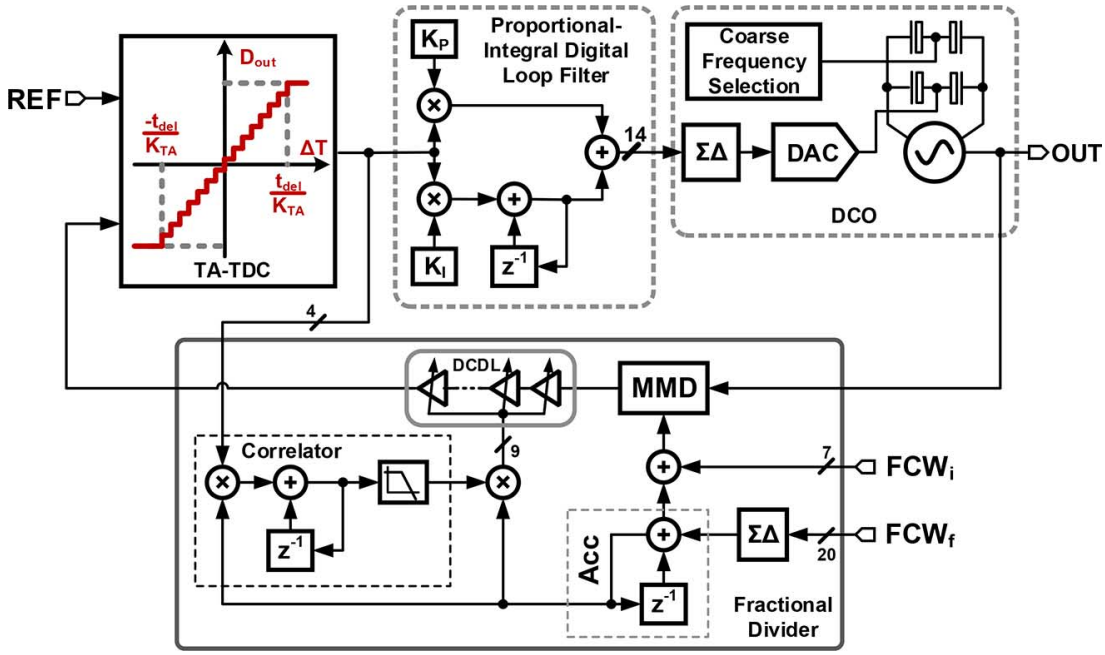

Fig. 16. Detailed block diagram of the proposed fractional-N PLL.

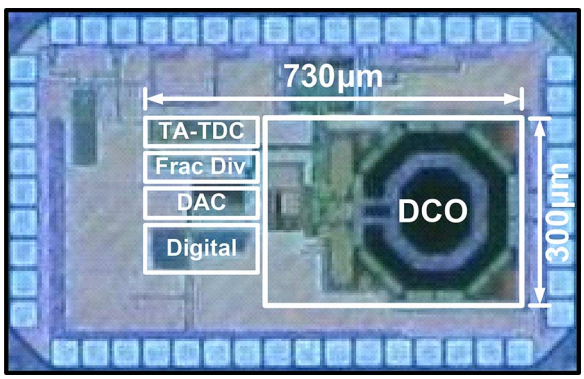

Fig. 17. Die photograph.

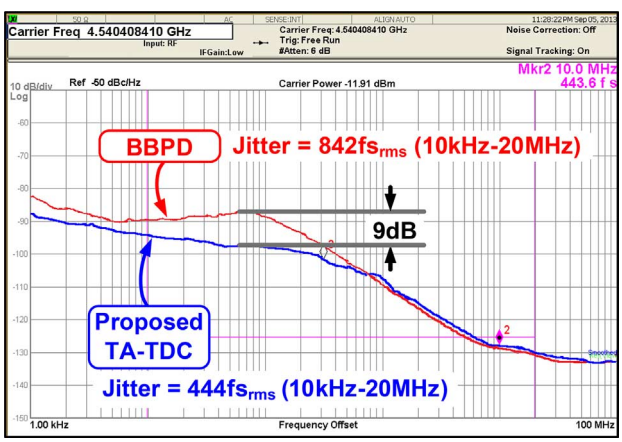

Fig. 18. Measured phase noise of the digital fractional-N PLL at 4.5 GHz for (a) conventional BBPD, and (b) proposed TA-TDC.

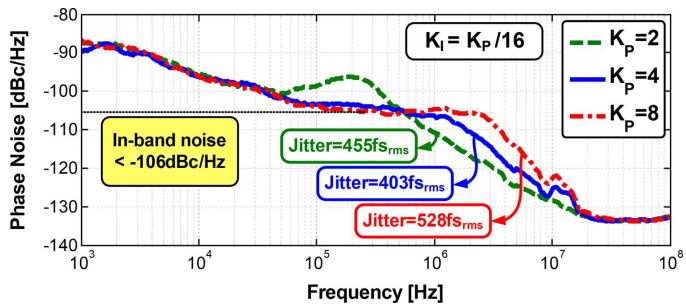

Fig. 19. Measured phase noise for different BW settings (0.75 MHz to 3 MHz) at 4.5 GHz output using 50 MHz reference, obtained by varying the proportional path (K_p) settings.

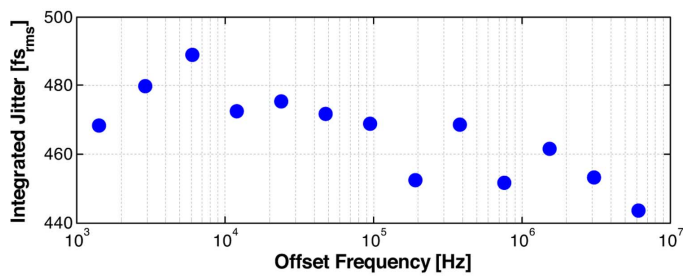

Fig. 20. Measured rms integrated jitter as a function of output fractional frequency offset.

frequency offsets is due to in-band fractional spurs generated due to DCDL integral non-linearity (INL).

The measured phase noise spectra for 0.75 MHz and 2.5 MHz bandwidths are shown in Fig. 21 for the in-band and out-of-band fractional spurs. For 0.75 MHz bandwidth, the proposed fractional-N DPLL achieves an integrated jitter of 423 fs_{rms} and 448 fs_{rms}, for out-of-band and in-band spurs, respectively. When the bandwidth is increased to 2.5 MHz, the integrated jitter increases only by about 85 fs, thanks to the fine resolution of the proposed TA-TDC. Fig. 22 shows the measured output spectrum of the proposed PLL with 392 kHz in-band fractional spurs. The

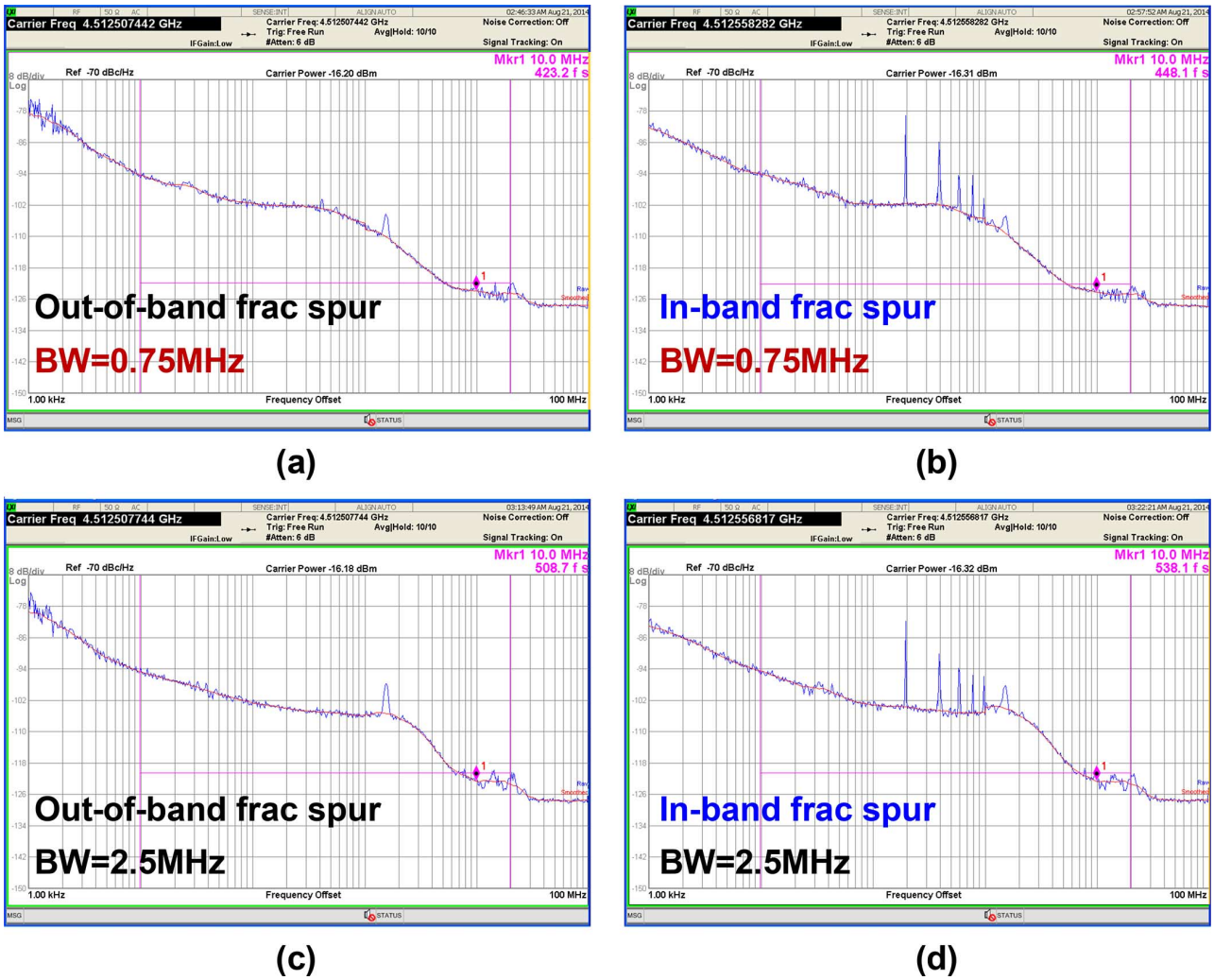

Fig. 21. Measured output spectra for (a) out-of-band fractional spurs and 0.75 MHz bandwidth, (b) in-band fractional spurs and 0.75 MHz bandwidth, (c) out-of-band fractional spurs and 2.5 MHz bandwidth, and (d) in-band fractional spurs and 2.5 MHz bandwidth.

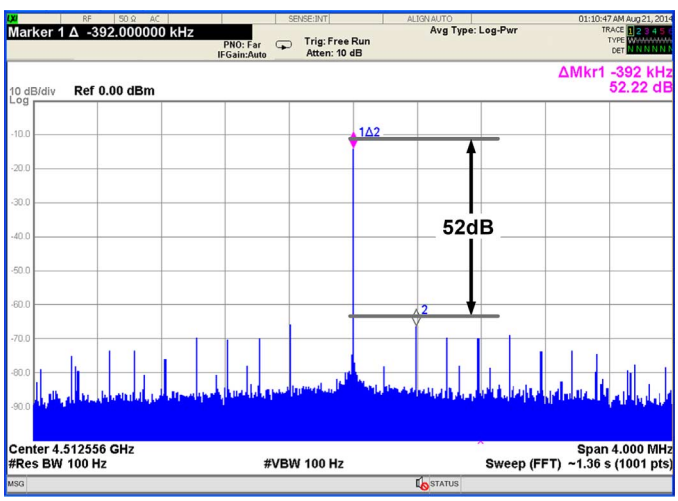

Fig. 22. Measured output spectrum at 4.5 GHz output frequency and 392 kHz fractional offset.

in-band fractional spur is -52.2 dBc. This excellent spurious performance, compared to [6], is achieved due to the better linearity of the proposed DTC architecture, without using complex non-linearity calibration [31]. The measured reference spur is less than -69 dBc. The integrated jitter was measured for different values of the output frequencies from 4.4 GHz to 5.2 GHz, and the results are shown in Fig. 23 for different bandwidth values. The integrated rms jitter varies by less than 100 fs over the output frequency range.

The performance summary and comparison with state-of-the-art low-jitter fractional-N PLLs are shown in Table II. The proposed architecture achieves the best reported jitter of 0.55 ps_{rms} at 3 MHz BW compared to [4], [7]. Plotted in Fig. 24 is the worst-case integrated jitter performance versus power consumption which is reflected in a figure of merit (FoM_J) [32]. The proposed digital fractional-N PLL, achieves the best FoM_J of -240.5 dB compared to state-of-the art digital and analog fractional-N PLLs. It achieves at least 8 dB better than other reported fractional-N DPLLs when the in-band phase noise is included in FoM_{IBPN}. The proposed architecture achieves excellent spurious performance along with the best power efficiency of 0.82 mW/GHz.

VI. Conclusion

A digital fractional-N PLL that achieves wide bandwidth and low jitter is presented. The proposed PLL employs a 9 bit DTC-

TABLE II
DPLL PERFORMANCE SUMMARY

	Hsu [2] JSSC'08	Temporiti [7] JSSC'10	Yao [36] VLSI'11	Zanuso [4] JSSC'11	Tasca [6] JSSC'11	Nonis [21] JSSC'13	This Work
Architecture	TDC	TDC	TDC	PI+TDC	DTC+BBPD	PI+BBPD	DTC+TDC
Technology [nm]	130	65	55	65	65	130	65
Supply [V]	1.5	1.2	1.2	1.2	1.2	1.5	1.0
Output Freq. [GHz]	3.67	2.8-3.8	5.9-8.0	3.6	2.9-4.0	0.84-1.032	4.4-5.2
Ref. Freq. [MHz]	50	35	2×40	40	40	25	50
Power [mW]	39	8.7	36	80	4.5	7.5	3.7
Ref. Spur [dBc]	-64	-61	-94	-61	-72	-70	-69
In-band Frac. Spur [dBc]	-53	-58	-70	-57	-42	N/A	-51.5
Bandwidth [MHz]	0.5	3.4	0.5	3.2	0.312	1	0.75 3
In-band PN [dBc/Hz]*	-108	-101	-107	-104	-101	-95	-102 -108
Integrated Jitter [ps_{rms}]	0.3 1k-40MHz	1.07 10k-10MHz	0.19 1k-10MHz	0.89 10k-30MHz	0.56 3k-30MHz	2.1 1k-10MHz	0.49 0.55 10k-20MHz
FoM_{IBPN} [dB]**	-283.2	-282.7	-282.8	-276.1	-285.1	-277.4	-287.4 -293.4
FoM_J [dB]* **	**-234.5**	**-230**	**-238.9**	**-222**	**-238.3**	**-224.8**	**-240.5 -239.5**
Power Eff. [mW/GHz]	10.82	2.29	6.1	22.22	1.13	7.5	0.82
Area [mm^2]	0.95	0.44	0.68	0.4	0.22	0.25	0.22

* *Normalized IBPN to 3.6GHz*, $^{**}\mathrm{FoM_{IBPN}} = \mathrm{IBPN} + 10\log\left[\left(\frac{1\mathrm{Hz}}{\mathrm{F_{out}}}\right)^2 \frac{\mathrm{P}}{1\mathrm{mW}}\right]$,

$^{***}\mathrm{FoM_J} = 10\log\left[\left(\frac{\sigma_{\mathrm{rms}}}{1\mathrm{sec}}\right)^2 \frac{\mathrm{P}}{1\mathrm{mW}}\right]$,

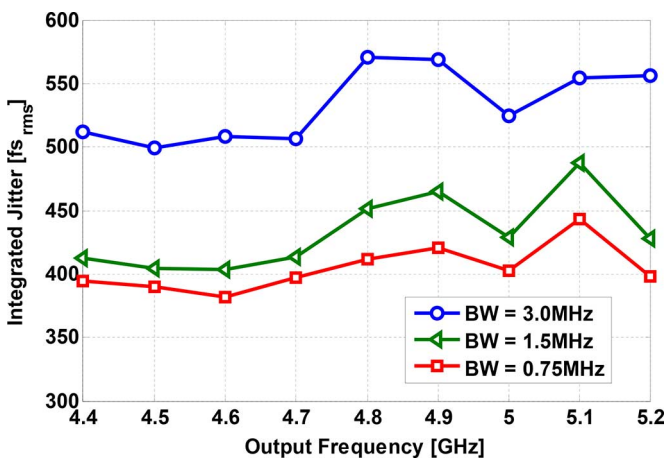

Fig. 23. Measured rms integrated jitter as a function of the output frequency for different bandwidth settings.

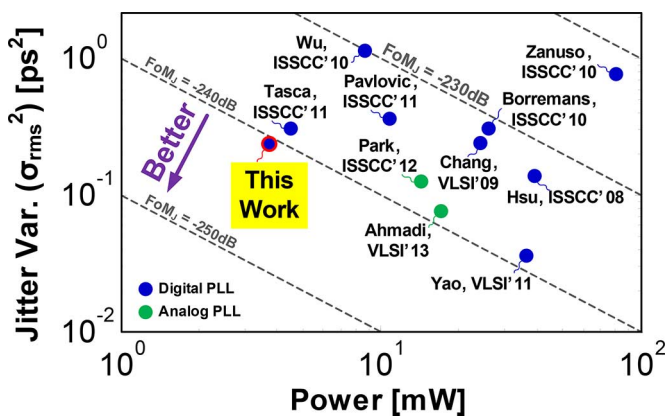

Fig. 24. FoM comparison.

based fractional divider that alleviates TDC dynamic range requirements. A high-resolution low-power time-amplifier based TDC (TA-TDC) is used to achieve low in-band noise and PLL wide bandwidth. The proposed TDC maintains linear loop dynamics with programmable PLL BW and faster DTC-gain calibration. The measured results indicate an excellent jitter performance at low power consumption, low in-band phase noise and wide PLL BW with no limit cycles.

ACKNOWLEDGMENT

The authors thank Berkeley Design Automation for providing the Analog Fast Spice (AFS) simulator. Thanks also to Seong-Joong Kim for his assistance in testing.

REFERENCES

[1] R. B. Staszewski *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2469–2482, Dec. 2005.

[2] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A low-noise wide-BW 3.6-GHz digital $\Delta\Sigma$ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008.
[3] E. Temporiti, C. Weltin-Wu, D. Baldi, R. Tonietto, and F. Svelto, "A 3 GHz fractional all-digital PLL with a 1.8 MHz bandwidth implementing spur reduction techniques," *IEEE J. Solid-State Circuits*, vol. 44, pp. 824–834, Mar. 2009.
[4] M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "A wideband 3.6 GHz digital $\Delta\Sigma$ fractional-N PLL with phase interpolation divider and digital spur cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, Mar. 2011.
[5] L. Vercesi, L. Fanori, F. De Bernardinis, A. Liscidini, and R. Castello, "A dither-less all digital PLL for cellular transmitters," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1908–1920, Aug. 2012.
[6] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9–4.0-GHz fractional-N digital PLL with bang-bang phase detector and 560-fs$_{\mathrm{rms}}$ integrated jitter at 4.5-mW power," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2745–2758, Dec. 2011.
[7] E. Temporiti, C. Weltin-Wu, D. Baldi, M. Cusmai, and F. Svelto, "A 3.5 GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2723–2736, Dec. 2010.
[8] S. Levantino, G. Marzin, C. Samori, and A. L. Lacaita, "A wideband fractional-N PLL with suppressed charge-pump noise and automatic loop filter calibration," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2419–2429, Oct. 2013.
[9] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1 Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.
[10] A. Swaminathan, K. J. Wang, and I. Galton, "A wide-bandwidth 2.4 GHz ISM band fractional-N PLL with adaptive phase noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, pp. 2639–2650, Dec. 2007.
[11] H. Hedayati, W. Khalil, and B. Bakkaloglu, "A 1 MHz bandwidth, 6 GHz 0.18 μm CMOS type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3244–3252, Dec. 2009.
[12] M. R. Ahmadi *et al.*, "A 288 fs RMS jitter versatile 8–12.4 GHz wideband fractional-N synthesizer for SONET and SerDes communication standards in 40 nm CMOS," in *IEEE VLSI Circuits Symp. Tech. Papers*, 2013, pp. C160–C161.
[13] G. Shu, W.-S. Choi, S. Saxena, T. Anand, A. Elshazly, and P. K. Hanumolu, "A 4-to-10.5 Gb/s 2.2 mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 150–151.
[14] C.-H. Hsiao, C.-J. Li, F.-K. Wang, T.-S. Horng, and K.-C. Peng, "Analysis and improvement of direct-conversion transmitter pulling effects in constant envelope modulation systems," *IEEE Trans. Microw.Theory Tech.*, vol. 58, no. 12, pp. 4137–4146, Dec. 2010.
[15] N. Pavlovic and J. Bergervoet, "A 5.3 GHz digital-to-time-converter-based fractional-N all-digital PLL," in *IEEE ISSCC Dig. Tech. Papers*, 2011, pp. 54–56.
[16] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW 3 MHz bandwidth 4.5 GHz digital fractional-N PLL with -106 dBc/Hz in-band noise using time amplifier based TDC," in *IEEE VLSI Circuits Symp. Tech. Papers*, 2014, pp. 1–2.
[17] M. Gupta and B.-S. Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2842–2851, Dec. 2006.
[18] M. Lee, M. E. Heidari, and A. A. Abidi, "A low-noise wideband digital phase-locked loop based on a coarse-fine time-to-digital converter with subpicosecond resolution," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2808–2816, Oct. 2009.
[19] K.-S. Kim, W.-S. Yu, and S.-H. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, Apr. 2014.
[20] A. Elshazly, S. Rao, B. Young, and P. K. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators: Analysis, design, and measurement techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1184–1197, May 2014.
[21] R. Nonis, W. Grollitsch, T. Santa, D. Cherniak, and N. Da Dalt, "digPLL-lite: A low-complexity, low-jitter fractional-N digital PLL architecture," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3134–3145, Dec. 2013.
[22] N. Da Dalt, "Linearized analysis of a digital bang-bang PLL and its validity limits applied to jitter transfer and jitter generation," *IEEE Trans. Circuits Syst. I*, vol. 55, pp. 3663–3675, Dec. 2008.
[23] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Exploiting stochastic resonance to enhance the performance of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 10, pp. 632–636, Oct. 2013.
[24] A. Elkholy, A. Elshazly, S. Saxena, G. Shu, and P. K. Hanumolu, "A 20-to-1000 MHz $\pm$14 ps peak-to-peak jitter reconfigurable multi-output all-digital clock generator using open-loop fractional dividers in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 272–273.
[25] S. S. Haykin, *Adaptive Filter Theory*, 5th ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2013.
[26] G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 20 Mb/s phase modulator based on a 3.6 GHz digital PLL with -36 dB EVM at 5 mW power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974–2988, Dec. 2012.
[27] M. H. Perrott, M. D. Trott, and C. G. Sodini, "A modeling approach for $\Sigma\Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.
[28] S.-K. Lee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 1 GHz ADPLL with a 1.25 ps minimum-resolution sub-exponent TDC in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2874–2881, Dec. 2010.
[29] N. Da Dalt, "Theory and implementation of digital bang-bang frequency synthesizers for high speed serial data communications," Ph.D. dissertation, RWTH Aachen University, Aachen, Germany, Feb. 2007.
[30] G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A background calibration technique to control bandwidth in digital PLLs," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 54–55.
[31] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1762–1772, Aug. 2014.
[32] X. Gao, E. A. Klumperink, P. F. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 2, pp. 117–121, Feb. 2009.
[33] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.
[34] L. Vercesi, A. Liscidini, and R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010.
[35] K.-S. Kim, Y.-H. Kim, W. Yu, and S.-H. Cho, "A 7 bit, 3.75 ps resolution two-step time-to-digital converter in 65 nm CMOS using pulse-train time amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, Apr. 2013.
[36] C.-W. Yao, L. Lin, B. Nissim, H. Arora, and T. Cho, "A low spur fractional-N digital PLL for 802.11a/b/g/n/ac with 0.19 ps$_{\mathrm{rms}}$ jitter," in *IEEE VLSI Circuits Symp. Tech. Papers*, 2011, pp. 110–111.

Ahmed Elkholy (S'08) received the B.Sc. degree with honors and the M.Sc. degree in electrical engineering from Ain Shams University, Cairo, Egypt, in 2008 and 2012, respectively. Currently, he is a research assistant at University of Illinois, Urbana-Champaign, IL, USA, where he is pursuing the Ph.D. degree.

He has been working on the design of energy-efficient high-speed serial links. From 2008 to 2012, he was an analog/mixed-signal design engineer at Si-Ware Systems, Cairo, Egypt, designing high-performance clocking circuits and LC-based reference oscillators. His research interests include frequency synthesizers, high-speed serial links, and low-power data converters.

Mr. Elkholy received Edward N. Rickert Engineering Fellowship from Oregon State University (2012–2013), and the Best M.Sc. Degree Award from Ain Shams University in 2012. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and IEEE International Symposium on Circuits and Systems (ISCAS).

Tejasvi Anand (S'12) is currently pursuing the Ph.D. degree at the University of Illinois at Urbana-Champaign, IL, USA. He received the M.Tech. degree (first class with distinction) in electronics design and technology from the Indian Institute of Science, Bangalore, India, in 2008.

From 2008 to 2010, he worked as an Analog Design Engineer at Cosmic Circuits (now a part of Cadence), Bangalore, on the design of analog-to-digital converters. From 2010 to 2011, he worked as a Project Associate at Indian Institute of Science, Bangalore, where he was involved in the design of neural recoding system and RF building blocks. His research interests are in energy-efficient high-speed wireline communication systems, frequency synthesizers, data converters and energy-efficient sensors.

Mr. Anand received the Analog Devices Outstanding Student Designer Award in 2013.

Woo-Seok Choi received the B.S. and M.S. degrees in electrical engineering and computer science from Seoul National University, Seoul, Korea, in 2008 and 2010, respectively. Currently, he is a Ph.D. candidate in electrical and computer engineering at the University of Illinois at Urbana-Champaign, IL, USA. His research interests include designing power-efficient high-speed serial links, low-power analog-to-digital converters and interface circuits for capacitive sensors.

Amr Elshazly (S'04–M'13) received the B.Sc. (Hons.) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2003 and 2007, respectively, and the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 2012, all in electrical engineering.

He is currently a Design Engineer at Intel Corporation, Hillsboro, OR, USA, developing high-performance high-speed I/O circuits and architectures for next generation process technologies. From 2004 to 2006, he was a VLSI Circuit Design Engineer at AIAT, Inc. working on the design of RF building blocks. From 2006 to 2007, he was with Mentor Graphics Inc., Cairo, designing multi-standard clock and data recovery circuits. His research interests include high-speed serial-links, frequency synthesizers, digital phase-locked loops, multiplying delay-locked loops, clock and data recovery circuits, data converter techniques, and low-power mixed-signal circuits.

Dr. Elshazly received the Analog Devices Outstanding Student Designer Award in 2011, the Center for Design of Analog-Digital Integrated Circuits (CDADIC) Best Poster Award in 2012, and the Graduate Research Assistant of the year Award in 2012 from the College of Engineering at the Oregon State University. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE International Symposium on Circuits and Systems, IEEE International Conference of Electronic Circuits Systems, and IEEE Asian Solid State Circuits Conference.

Pavan Kumar Hanumolu (S'99–M'07) is currently an Associate Professor in the Department of Electrical and Computer Engineering and a Research Associate Professor with the Coordinated Science Laboratory at the University of Illinois, Urbana-Champaign, IL, USA. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, Corvallis, OR, USA, in 2006, where he subsequently served as a faculty member until 2013. His research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.

Dr. Hanumolu received the National Science Foundation CAREER Award in 2010. He currently serves as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and is a technical program committee member of the VLSI Circuits Symposium and the IEEE International Solid-State Circuits Conference (ISSCC).