Design and Analysis of Low-Power High-Frequency Robust Sub-Harmonic Injection-Locked Clock Multipliers

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***Abstract*—A low-jitter, low-power LC-based injection-locked clock multiplier (ILCM) with a digital frequency-tracking loop (FTL) is presented. Based on a pulse gating technique, the proposed FTL continuously tunes the oscillator's free-running frequency to ensure robust operation across PVT variations. The FTL resolves the race condition existing in injection-locked PLLs by decoupling frequency tuning from the injection path, such that the phase-locking condition is only determined by the injection path. This paper also introduces an accurate theoretical large-signal analysis for phase domain response (PDR) of injection-locked oscillators (ILOs). The proposed PDR analysis captures the asymmetric nature of ILO's lock-in range, and the impact of frequency error on injection strength and phase noise performance. The proposed architecture and analysis are demonstrated by a prototype fabricated in 65 nm CMOS process with active area of 0.25 mm^2. The prototype ILCM generates output clock in the range of 6.75–8.25 GHz by multiplying the reference clock by 64. It achieves superior integrated jitter performance of 190 fs$_{\text{rms}}$, while consuming 2.25 mW power. This translates to an excellent figure-of-merit (FoM) of -251 dB, which is the best reported high-frequency clock multiplier.**

***Index Terms*—Clock multiplier, DCO, digital phase-locked loop (PLL), frequency multiplier, frequency tracking, impulse sensitivity function (ISF), injection locking, multiplying injection-locked oscillator (MILO), phase domain response (PDR), phase noise, PLLs, pulse, reference spur, rms jitter, sub-harmonic locking, sub-sampling (SS).**

I. Introduction

PHASE-LOCKED loops (PLLs) are most commonly used for high-frequency clock generation from a low-frequency clock provided by crystal oscillator. While they have been optimized for low power consumption and small area, their noise performance is fundamentally limited by the coupled noise bandwidth tradeoff. The oscillator noise is high-pass shaped, whereas noise of the other loop components such as the charge pump and divider is low-pass filtered by the PLL bandwidth. Assuming a clean reference clock, optimum jitter performance is achieved at a loop bandwidth where the oscillator and loop noise contribution to the output jitter are equal. Because of this tradeoff, achieving superior jitter performance ($<$200 fs$_{\text{rms}}$) with conventional PLLs mandates stringent noise performance of the oscillator and/or loop components, thus resulting in high power consumption (tens of mWs) [1]–[3]. A sub-sampling (SS)-PLL architecture alleviates these tradeoffs. The feedback divider is omitted and the charge pump noise is suppressed by a high gain sub-sampling phase detector (SSPD) [4]. Consequently, excellent in-band phase noise and figure-of-merit (FoM) were achieved [4], [5]. However, the SSPD has a limited capture range especially at low supply voltage and more importantly a large loop filter capacitor is needed because of high-phase detector gain.

Another commonly used approach for low-noise clock generation is based on directly resetting jitter accumulation in the oscillator. This is done by replacing the noisy oscillator edge with a clean reference clock edge and this architecture is referred to as a multiplying delay locked loop (MDLL) [6], [7]. This architecture also alleviates the conflicting noise filtering requirements of conventional PLLs and is shown to be capable of achieving low jitter and low power [8], [9]. However, MDLL by nature is suitable only for ring-based voltage-controlled oscillators (VCOs) and its frequency is usually limited to a few GHz because of the timing constraints in its selection logic. Sub-harmonic injection locking works, in principle, similar to an MDLL. A free-running oscillator can be *injection* locked to the Nth harmonic of the reference clock by injecting narrow pulses at the reference frequency into the oscillator ($F_{\text{OUT}} = NF_{\text{REF}}$) as depicted in Fig. 1(a). As a result, this technique provides a simple means for implementing very low-jitter integer-N clock multiplication using either ring [10]–[12] or LC VCOs [13]–[18]. When injection locked, the oscillator tracks the reference clock and its oscillator phase noise is greatly suppressed as illustrated in Fig. 1(b). Unlike MDLLs, injection-locked clock multipliers (ILCMs) have no selection logic, so they are suitable for very high-frequency clock generation using LC-VCOs [16]–[18].

However, in practice, any frequency error (F_{ERR}) between the oscillator free-running frequency (F_{o}) and the target frequency (NF_{REF}) will degrade the clock multiplier performance as shown in Fig. 1(c). F_{ERR} occurs due to drift in oscillator

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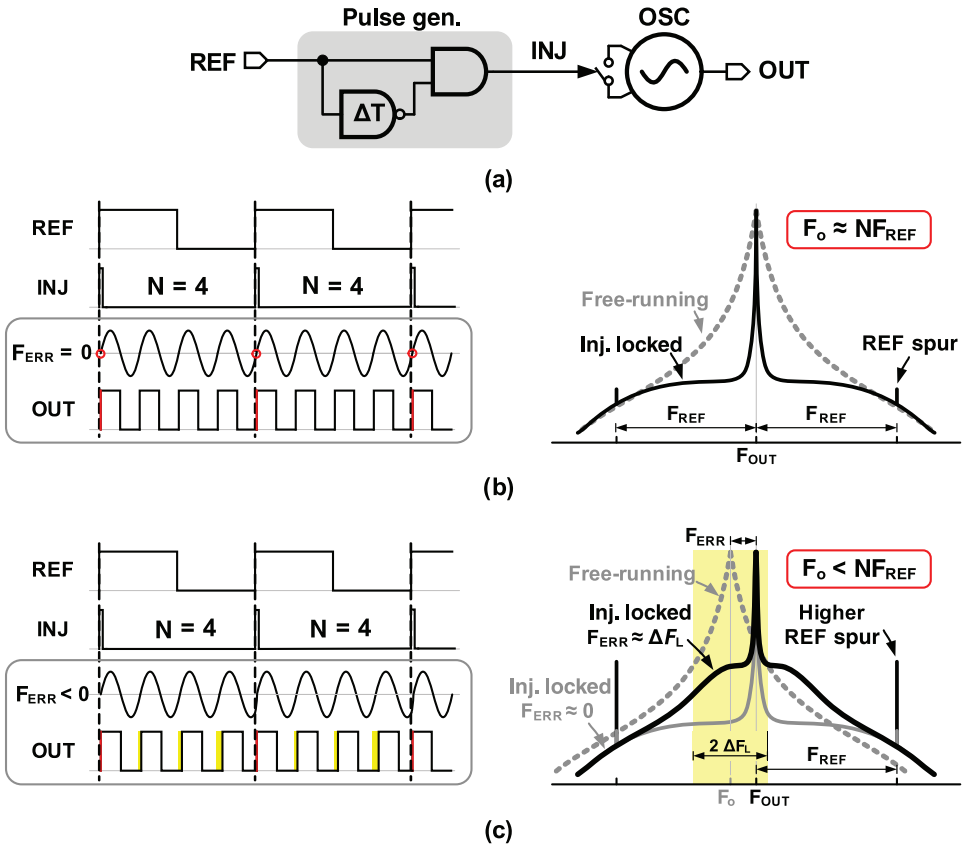

Fig. 1. (a) Sub-harmonic ILO. Timing diagram and output spectrum of ILCM when (b) $F_{\mathrm{ERR}} = 0$ and (c) $F_{\mathrm{ERR}} \approx \Delta F_L$.

free-running frequency across supply and temperature, and can easily exceed the lock-in range (ΔF_{L}) especially when ΔF_{L} is narrow (a few hundreds of ppms) as is the case when either a high-Q LC oscillator or large multiplication factor N is used. Dedicated frequency-tracking loop (FTL) is needed to correct F_{ERR} [11], [13].

In this paper, we present a digital FTL to continuously tune the oscillator's free-running frequency (F_{o}) to be NF_{REF} [19]. The proposed FTL, implemented using a low-power digital feedback loop, ensures robust operation of the ILCM across process, voltage, and temperature (PVT) variations even when the lock-in range ($\Delta F_{\mathrm{L}} < 500$ ppm) is narrow, multiplication factor N is large, and the oscillator Q is high. The prototype ILCM generates output clock in the range of 6.75–8.25 GHz by multiplying F_{REF} by 64 and achieves 190 $\mathrm{fs_{rms}}$ integrated jitter. The entire ILCM consumes 2.25 mW from 0.9 V supply and achieves an FoM of -251 dB.

This paper is organized as follows. Section II illustrates the basic concepts of injection locking highlighting frequency tracking challenges followed by a brief overview of state-of-the-art ILCMs. The proposed architecture is then presented in Section III, in addition to a detailed analysis of sub-harmonic injection-locking dynamics. The circuit implementation of critical building blocks is presented in Section IV. The measured results from the test chip are shown in Section V. Finally, the key contributions of this work are summarized in Section VI.

II. Injection-Locked Clock Multiplication

A. Basic Concept

Injection locking has many applications in frequency division [3], [20], phase de-skew [21], quadrature generation [22], and clock multiplication [10]–[19]. Our focus is on injection-locked clock multiplication, wherein a free-running oscillator is locked to the Nth harmonic of the injected signal. In this case of so-called sub-harmonic injection ($F_{\mathrm{REF}} = F_{\mathrm{INJ}}$), the injection signal is in the form of narrow pulses to increase the power of Nth harmonic [23]. These narrow periodic-injected pulses adjust the oscillator phase and if the oscillator free-running frequency F_o is within the lock-in range, the oscillator gets phase-locked to the injected signal. Under this condition, the oscillator runs at F_{o} for $(N-1)$ cycles, while the injection pulse changes the period of Nth cycle so that the average frequency equals NF_{REF} [see the timing diagram in Fig. 1(c)]. In other words, phase error accumulated in $(N-1)$ cycles is compensated by an excess phase equal to $2\pi\ NF_{\mathrm{ERR}}/F_{\mathrm{o}}$ due to pulse injection in the Nth cycle. This periodic correction appears as deterministic jitter (DJ $\approx (N-1)\ \alpha T_{\mathrm{OUT}} \approx \alpha T_{\mathrm{REF}}$) where $\alpha = F_{\mathrm{ERR}}/F_{\mathrm{OUT}}$ is the relative error. This translates to a reference spur ($\mathrm{Spur_{dBc}} \approx 20\ \log(\mathrm{DJ}/T_{\mathrm{OUT}}) \approx 20\ \log(\alpha\ N)$) [13]. Fig. 2 shows the impact of frequency error and the multiplication factor N on the deterministic jitter and reference spur performance. Phase noise performance is also degraded by NF_{ERR} because of the reduced filtering bandwidth as shown in

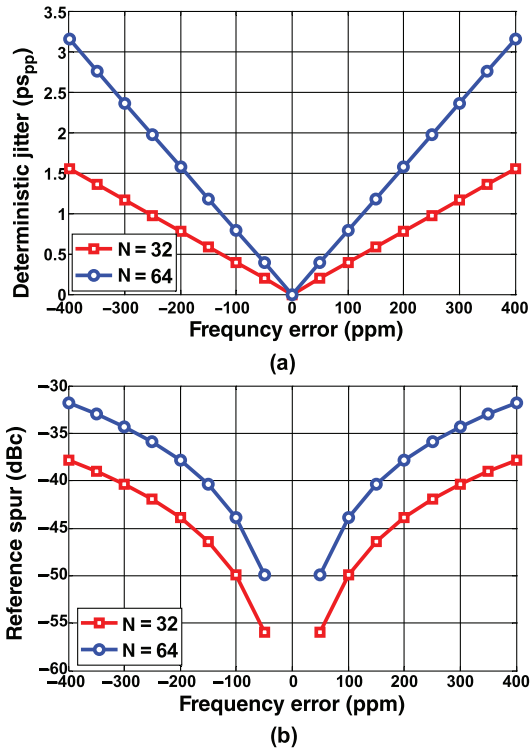

Fig. 2. (a) Deterministic jitter and (b) reference spur as a function of F_{ERR} for $N = 32$ and 64.

Fig. 1(c). Thus, the random and deterministic jitter performance of ILCMs greatly depends on NF_{ERR}, which mandates continuous tuning of the oscillator frequency to not only maintain phase lock but also to achieve excellent jitter/spur performance across voltage and temperature variations.

B. Conventional ILCM Architectures

A conventional injection-locked PLL is shown in Fig. 3. The PLL is introduced to tune the VCO free-running frequency F_{o} to be close to the center of the lock-in range. However, it is difficult to detect the drift in F_{o} at the phase detector input because the accumulated phase difference is almost reset at every reference cycle by the fast injection path as illustrated by the timing diagram in Fig. 3. Further, since the VCO phase is adjusted simultaneously by the injection and PLL paths, injection-locked PLL also has to contend with the resulting race condition. Calibration of the injection timing is needed to overcome such a race condition. In [14], calibration is done in a foreground manner, so it cannot track voltage and temperature variations, whereas in [18], calibration is done in background using an analog delay locked loop (DLL). In [10] and [15], the injection timing is matched relying on a time-adjusted SS phase detector with high gain. However, these techniques are susceptible to charge pump current mismatch, and vulnerable against voltage and temperature, which limit the multiplication factor (N) and may degrade jitter and spurious performance.

The drawbacks of injection-locked PLL can be alleviated by using a replica DCO locked in a digital FLL [18]. The main DCO placed outside the loop shares the same control word with the replica DCO to track any frequency drift to the extent the two oscillators are matched as shown in Fig. 4(a). However, this approach requires two matched oscillators, which doubles both power and area, and its effectiveness is limited by DCO gain (K_{DCO}) mismatch. Another approach proposed by Helal *et al.* [13] uses a high-resolution time-to-digital converter (TDC) as depicted in Fig. 4(b). The TDC measures the oscillator period when perturbed by the injection pulse and compares it to the measured free-running period. A correlator generates an error signal Δ as the difference between the two measurements as a direct representation of F_{ERR}. By accumulating Δ, the frequency error F_{ERR} can be corrected by continuously tuning the oscillator frequency to be in the middle of the lock-in range. However, the use of a high-resolution TDC incurs a large power and area penalty.

III. Proposed ILCM With Continuous FTL

A. Basic Concept of the Proposed FTL

The proposed continuous FTL is based on a pulse gating technique shown in Fig. 5(a). Because injection pulses reset oscillator phase and make it difficult to detect the phase error caused by frequency error F_{ERR}, we propose to disable or gate the injection pulse periodically, and measure the accumulated phase error Δ_{Gated}, as depicted in the timing diagram shown in Fig. 5(b). When a pulse is gated, the oscillator continues to run at its free-running frequency (F_{o}). Consequently, a phase detector can be used to detect the frequency error F_{ERR} without the need for a power-hungry high-resolution TDC. In this example, every fourth reference edge is not injected, which results in a large Δ_{Gated} that can be easily measured using a simple phase detector. We then use this error information to correct F_{ERR} using a simple digital feedback loop. Injection gating resolves the race condition present in IL-PLLs, as it decouples the FTL from the injection path. As a result, the phase-locking condition is now only determined by the injection path.

The sign of F_{ERR} is detected simply by detecting the sign of Δ_{Gated} using an SS bang-bang phase detector (BBPD). The measured error is integrated using a digital accumulator whose output updates the frequency of the injection-locked DCO incrementally at every pulse gating event as demonstrated in Fig. 6. This simple approach is similar to a bang-bang FLL and it corrects F_{ERR} accurately and continuously tunes the DCO frequency to the center of the lock-in range. The proposed FTL ensures robust operation across supply and temperature variations and helps achieve excellent jitter and spurious performance.

B. Complete Architecture

The complete block diagram of the proposed ILCM is shown Fig. 7. It consists of an injection-locked LC-DCO, a programmable pulse generator, and a digital FTL. The operation proceeds as follows. First, at startup, the DCO free-running frequency (F_{o}) is coarsely tuned to be within the lock-in range. Because of the sub-sampling nature of the architecture, coarse frequency selection is also used to set the target multiplication factor (N). The coarse frequency selection is done only during startup. Consequently, the power and noise associated with

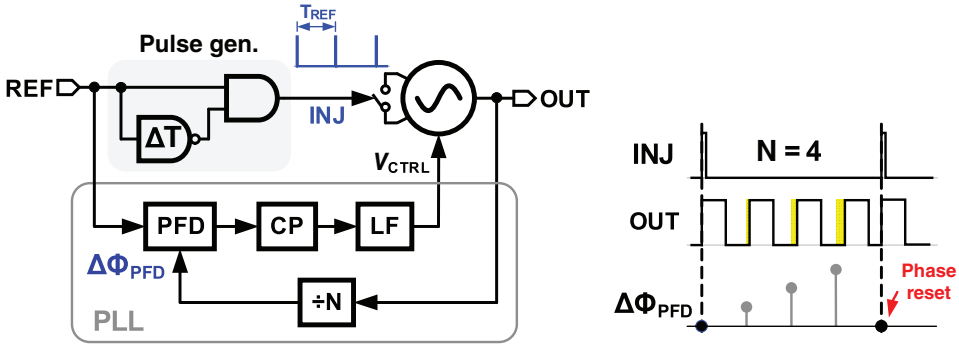

Fig. 3. Block diagram of conventional injection-locked PLL with an illustrating timing diagram.

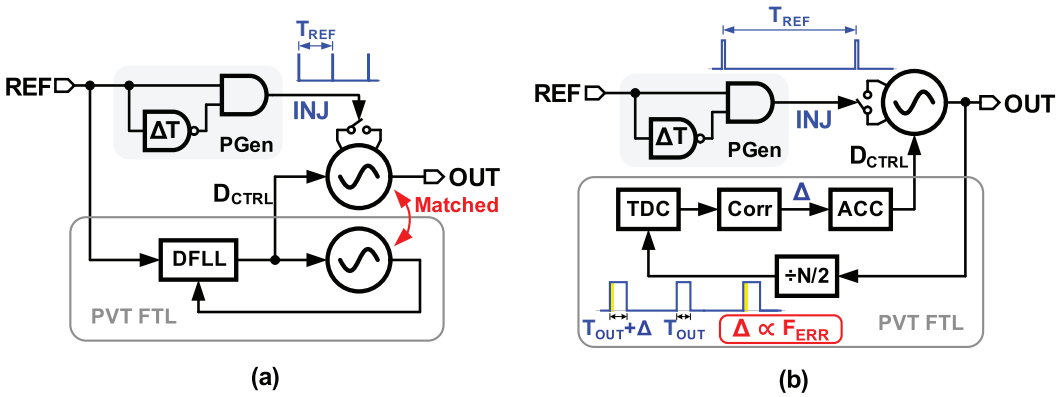

Fig. 4. Block diagram of ILCM with (a) replica-based FTL [11] and (b) TDC-based FTL [13].

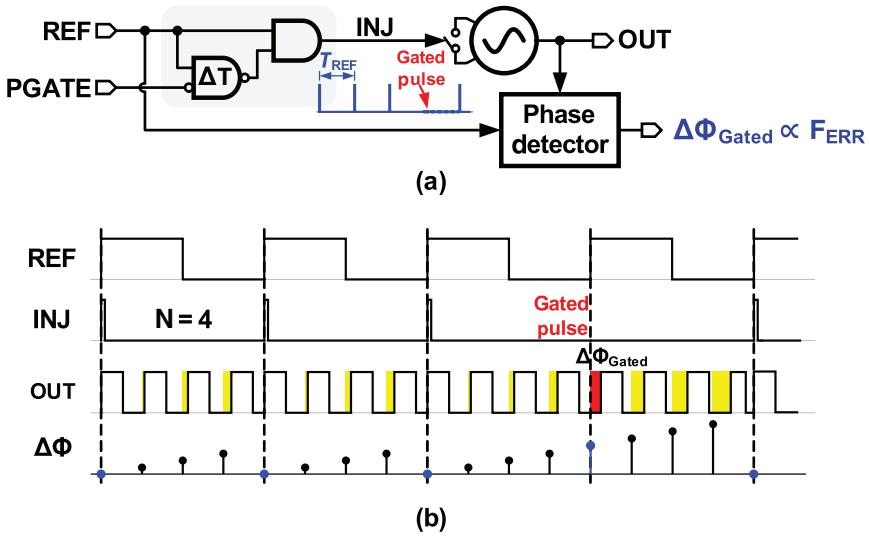

Fig. 5. (a) Conceptual diagram of the proposed pulse getting frequency error detection. (b) Timing diagram.

the divider is eliminated in normal operation. Injection path, enabled in the second step, locks DCO phase to the injected pulse (INJ) with a time constant proportional to the injection strength.

Once initial phase lock is achieved, FTL is used to maintain lock by correcting the frequency drift caused by voltage and temperature variations. To this end, the proposed FTL measures the accumulated phase error due to F_{ERR} when the injection pulse is gated. However, because of the unknown delay T_{D} in the pulse generator and DCO buffer, there is no predefined phase relationship between the DCO output and the reference (REF). Consequently, the resulting phase error Δ_{Gated} cannot be directly attributed to F_{ERR}. To mitigate this, a DLL consisting of the SS BBPD and accumulator ($\mathrm{ACC_P}$) tunes the delay of a digitally controlled delay line (DCDL) such that BBPD inputs are aligned. The frequency tracking path is enabled after the DLL is locked and the BBPD output is integrated only when the injection path is gated. Note that because the same BBPD is used in the DLL and FTL, its offset is not critical.

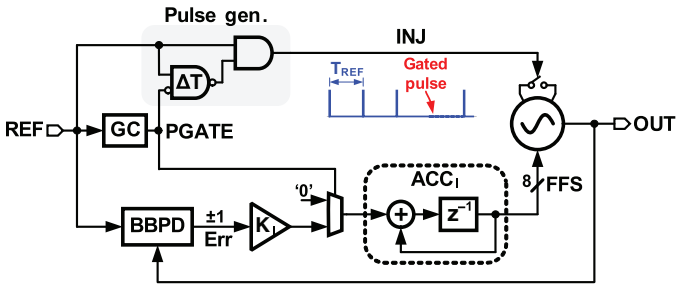

Fig. 6. Block diagram of the proposed FTL.

The proposed FTL architecture resembles a delay/phase-locked loop (D/PLL) architecture [24] in which the proportional control is implemented in phase domain using accumulator $\mathrm{ACC_P}$ and integral control using accumulator $\mathrm{ACC_I}$. Both control paths operate simultaneously but in an orthogonal manner, the integral control is updated only when injection is gated, while the DLL accumulator is updated when injection pulses are applied. The DLL has to be faster than the frequency-tracking path for accurate frequency error detection and to guarantee stable operation. The gating rate is made programmable and can take three values in the prototype (1/2, 1/4, 1/8). Lower gating rate is sufficient because FTL needs only to track slow variations caused by changes in voltage and temperature.

C. Phase Domain Response (PDR) Analysis

Pulse injection into an oscillator will perturb both amplitude and phase of the oscillator. Because of the amplitude-limiting dynamics of the oscillator, amplitude variations due to pulse injection will decay rapidly in a couple of oscillator cycles. On the other hand, phase fluctuations persist indefinitely as was shown in [25]. It can be shown that an injection pulse that is in the form of small current impulse will only change the voltage across the capacitor (V_c) and will not affect the current through the inductor [25]. The resultant oscillator phase change will depend on the position of the pulse with respect to the oscillator phase. For example, a pulse injected near the zero crossing of V_c will have a strong effect on phase and negligible effect on amplitude. Injection when V_c is near its peak will mainly cause amplitude change and minimal phase shift. This means pulse injection into oscillator is a time variant-process as described by the impulse sensitivity function (ISF) introduced by Hajimiri and Lee in [25] for phase noise analysis. In [26], a phase domain model for injection-locked oscillator (ILO) based on ISF is introduced. Dunwell and Carusone [27] shows that the ISF approach is limited to small-signal analysis and cannot model ILO under large-signal injection.

In [27] and [28], transient simulations were used to describe ILO's large-signal phase domain response under different injection conditions. A closed-form expression for PDR when the injection pulse is narrow was reported in [14]. These expressions: 1) become inaccurate under strong injection especially when the injection pulsewidth (D) is comparable to the oscillator period and 2) the asymmetric nature of ILO described in [27] is not captured. In view of these drawbacks, we seek to develop accurate analysis for large-signal PDR under different injection conditions.

The oscillator can be represented by the half circuit shown in Fig. 8(a) where the injection switch is modeled by its on resistance (R_{sw}). The tank losses are represented by parallel resistance (R_{p}) and the oscillator free-running frequency is equal to $\omega_o = 1/\sqrt{LC}$. The injection pulse whose width is D will cause the switch to turn on and change the voltage across the capacitor (V_c). Assuming $R_{\mathrm{sw}} \ll R_{\mathrm{p}}$, this circuit can be further simplified as a simple RC circuit because current through the inductor is not affected and R_{p} can be ignored [13], [25]. Input phase (Φ_i) is defined as the phase difference between the center of the injection pulse and the oscillator phase, and the output phase (Φ_o) represents the change in oscillator phase after it is pulled toward the injection pulse as illustrated in Fig. 8(a). The voltage change across the capacitor due to injection will depend on the time constant ($\tau = R_{\mathrm{sw}}C$), the capacitor voltage (V_c) during injection, and pulsewidth (D). Without injection, the capacitor voltage can be expressed as $V_c(t) = A\sin(\omega_o t + \Phi_i)$, where A is the oscillation amplitude. When the injection pulsewidth is much less than the oscillator period (i.e., $D\,\omega_o \ll 2\pi$), the capacitor voltage can be approximated by a constant during injection (i.e., from $-D/2$ to $D/2$) as $V_{c,\mathrm{inj}} = V_c(0) = A\sin(\Phi_i)$. Consequently, the voltage change due to injection can be approximated as $\Delta V = V_{c,\mathrm{inj}}\,(1 - e^{-D/\tau})$ as in [14].

However, this narrow pulse analysis is not accurate because it ignores the change of $V_c(t)$ during the duration of the injection pulse. In order to account for the effect of the pulsewidth correctly, we divide the injection pulse into M infinitesimally small pulses, each having a width of $d = D/M$ [see Fig. 8(a)]. Each of the kth pulse causes a change in V_c by δv_k. By summing the changes δv_k from each pulse, the total change in capacitor voltage can be calculated accurately. As $d\,\omega_o \ll 2\pi$, δv_k can be expressed as

$$\delta v_k = V_{c,k}\,(1 - e^{-d/\tau}) \approx V_{c,k}\,\frac{d}{\tau} \tag{1}$$

where $V_{c,k}$ is the capacitor voltage when pulse k is applied. The phase component of $V_{c,k}$ will depend on the position (x) of pulse k, and as x increases, the phase difference between thin pulse k and oscillator zero crossing decreases. So, when pulse position x changes from 0 to D, $V_{c,k}$ phase will change from $\Phi_i + 0.5\,\omega_o D$ to $\Phi_i - 0.5\,\omega_o D$ as illustrated in Fig. 8(a). $V_{c,k}$ can can expressed as follows:

$$x = 0 \Rightarrow \quad V_{c,0} = A\,\sin(\Phi_i + 0.5\,\omega_o D) \tag{2}$$

$$x = d \Rightarrow \quad V_{c,1} = A\,e^{-d/\tau}\,\sin(\Phi_i + 0.5\,\omega_o D - \omega_o d) \tag{3}$$

$$x = kd \Rightarrow \quad V_{c,k} = A\,e^{-kd/\tau}\,\sin(\Phi_i + 0.5\,\omega_o D - \omega_o kd). \tag{4}$$

Consequently, we can express the normalized total change in capacitor voltage due to injection as

$$\Delta_{\mathrm{INJ}} = \frac{1}{A}\sum_k \delta v_k\,\cos(\omega_o kd) = \frac{1}{A}\sum_k V_{c,k}\,\frac{d}{\tau}\,\cos(\omega_o kd)$$

$$= \sum_k e^{-kd/\tau}\,\sin(\Phi_i + 0.5\,\omega_o D - \omega_o kd)\,\cos(\omega_o kd)\,\frac{d}{\tau}. \tag{5}$$

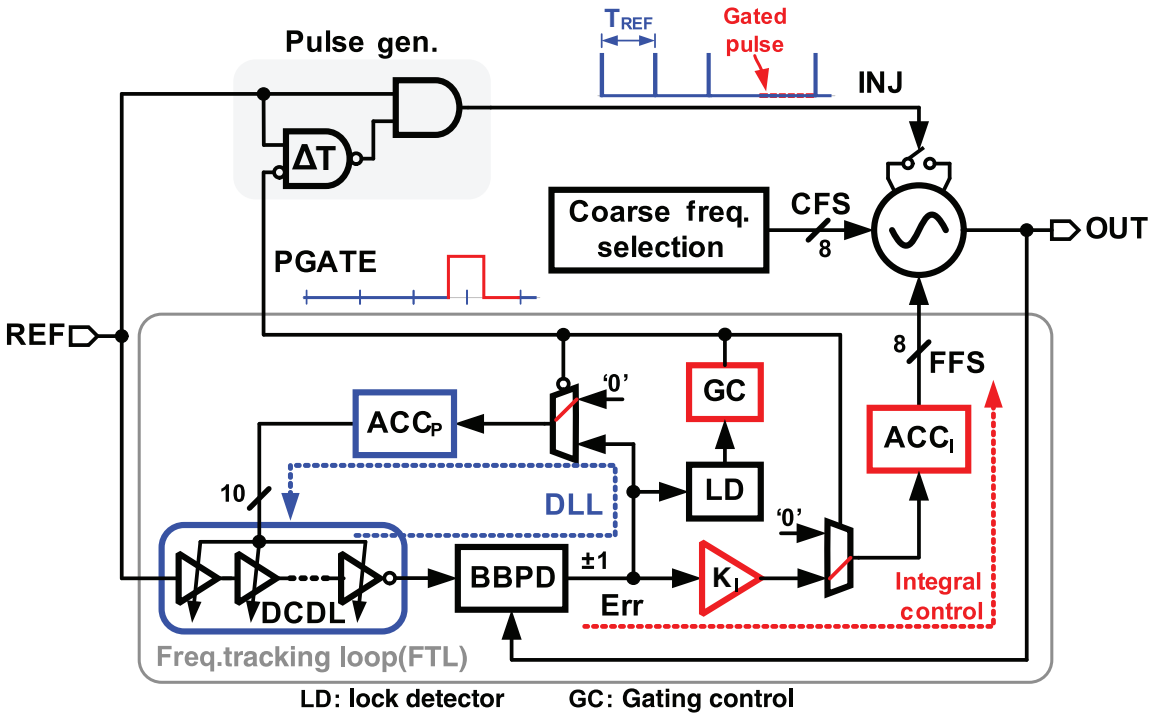

Fig. 7. Block diagram of the proposed ILCM.

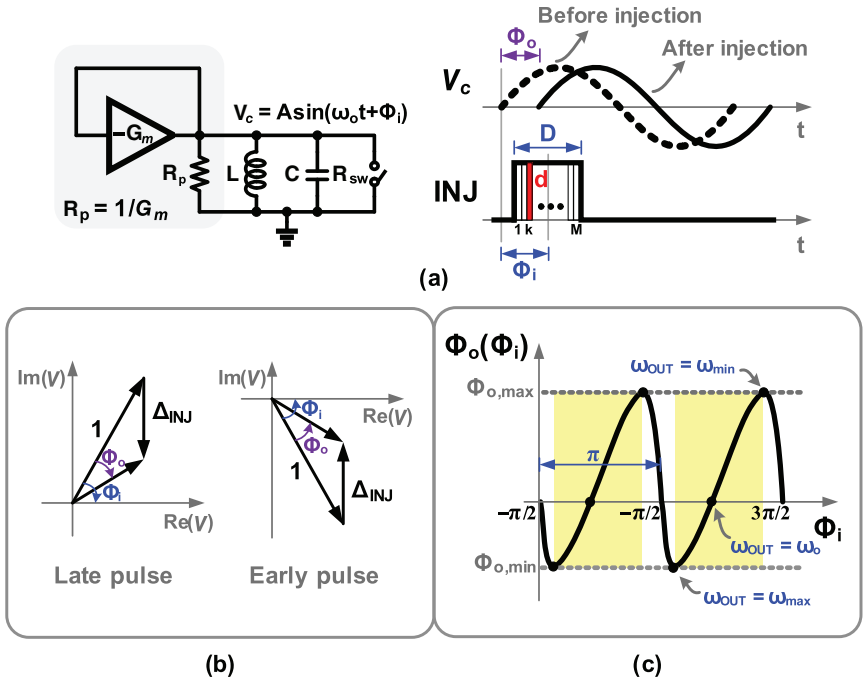

Fig. 8. PDR analysis. (a) LC oscillator simplified half circuit with an illustrating timing diagram. (b) Voltage phasor diagram. (c) PDR diagram.

The $\cos(\omega_o kd)$ term is added to account for the phase difference between pulses, as δv_k are summed as vectors. As $d \to 0$, the summation can be transformed into integration from $x = 0$ to $x = D$, where $x = kd$

$$\Delta_{\text{INJ}}(\Phi_i) = \frac{1}{\tau}\int_0^D e^{-x/\tau}\sin(\Phi_i + 0.5\,\omega_o D - \omega_o x) \times \cos(\omega_o x)\,dx \tag{6}$$

$$\Delta_{\text{INJ}}(\Phi_i) = \frac{1}{2}\sin\left(\Phi_i + \frac{\omega_o D}{2}\right)(1 - e^{-D/\tau}) - \frac{1}{2 + 8\omega_o^2\tau^2} \times \left[2\omega_o\tau\cos\left(\Phi_i + \frac{\omega_o D}{2}\right) - \sin\left(\Phi_i + \frac{\omega_o D}{2}\right) - e^{-D/\tau}\left(2\omega_o\tau\cos\left(\Phi_i - \frac{3\omega_o D}{2}\right) - \sin\left(\Phi_i - \frac{3\omega_o D}{2}\right)\right)\right]. \tag{7}$$

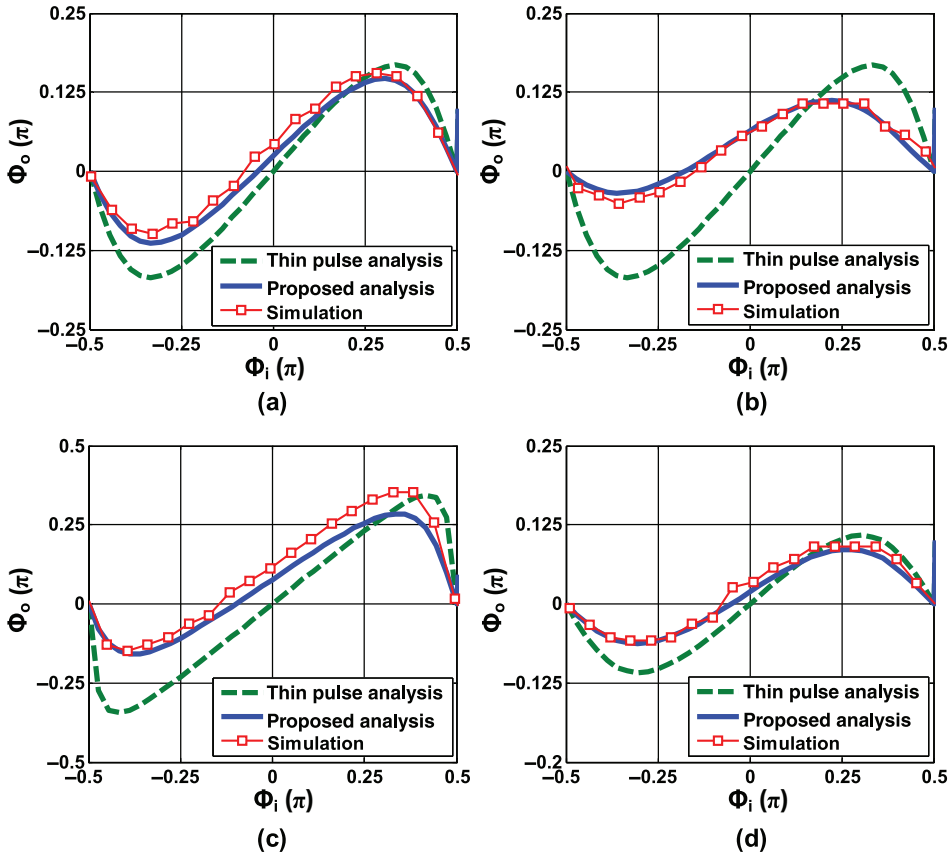

Fig. 9. PDR analysis and simulation results in case (a) $R_{sw} = 20\ \Omega$, $D = 20$ ps; (b) $R_{sw} = 40\ \Omega$, $D = 40$ ps; (c) $R_{sw} = 10\ \Omega$; $D = 25$ ps; and (d) $R_{sw} = 40\ \Omega$, $D = 25$ ps.

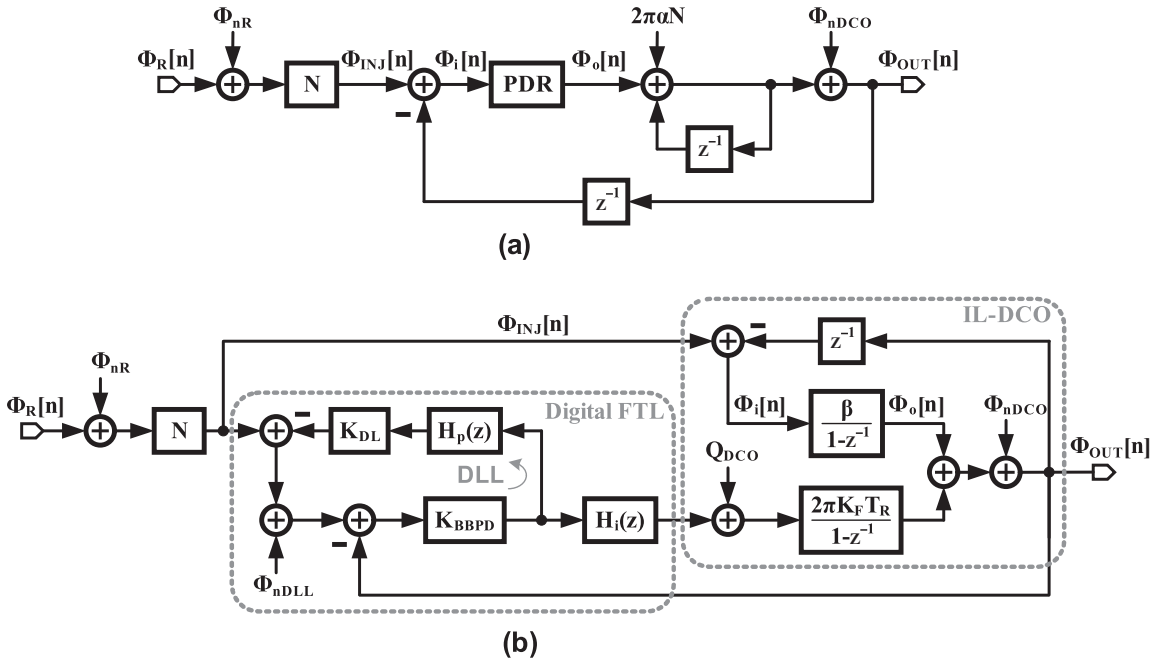

Fig. 10. (a) Phase-domain model of sub-harmonic ILO and (b) discrete-time phase-domain model of the proposed ILCM.

Once $\Delta_{\mathrm{INJ}}(\Phi_i)$ is obtained, a phasor diagram for the oscillator under injection can be drawn as shown in Fig. 8(b) as in [14] and [29]. The center of the pulse is assumed as the reference phase. Using simple trigonometry, the PDR that defines the relation between input phase (Φ_i) and output phase (Φ_o) can be deduced as follows:

$$\Phi_o = \Phi_i - \tan^{-1}(\tan(\Phi_i) - \Delta_{\mathrm{INJ}} \times \sec(\Phi_i)). \quad (8)$$

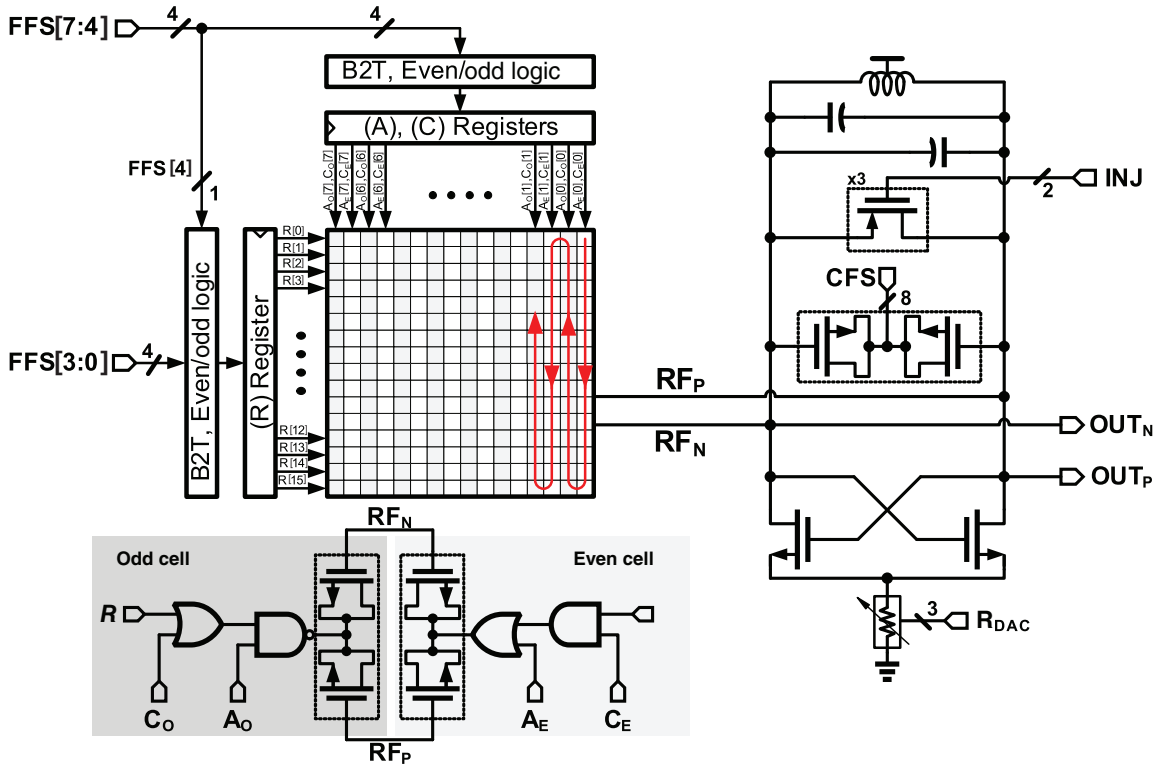

Fig. 11. LC-based DCO implementation.

Fig. 8(c) illustrates an example of a PDR diagram where Φ_o is drawn as a function of Φ_i. A few insightful observations can be deduced from this diagram. First, PDR is a periodic function with a period of π. This indicates that pulse injection stimulates positive and negative edges of the oscillator equally. Consequently, the pulse can be locked to either positive or negative edges depending on the initial input phase $\Phi_{i,\text{init}}$. This may create a $\pm\pi$ phase ambiguity in the output phase that has to be taken into consideration in applications that require output phase to be deterministic. Second, we can observe that Φ_o goes to zero when Φ_i gets close to $\pm\pi/2$. At these points, the oscillator output voltage will be at peaks or troughs where injection pulse will cause minimal phase change but can cause significant change in amplitude. The injection strength (β) is defined as the slope of the PDR and can be expressed as follows:

$$\beta(\Phi_i) = \frac{d\Phi_o}{d\Phi_i} = 1 - \frac{\sec(\Phi_i)^2 - \Delta'_{\text{INJ}}\sec(\Phi_i) - \Delta_{\text{INJ}} \times \sec(\Phi_i)\tan(\Phi_i)}{1 + (\tan(\Phi_i) - \Delta_{\text{INJ}}\sec(\Phi_i))^2} \tag{9}$$

where Δ'_{INJ} is the first derivative of (6). From the PDR, we can intuitively understand the dynamics of injection locking. When $F_{\text{ERR}} = 0$, pulses injected at reference rate with an initial phase of $\Phi_{i,\text{init}}$ will pull the oscillator phase by $\Phi_o(\Phi_{i,\text{init}})$, so that the next injection pulse will have a smaller Φ_i. In steady state, Φ_o reaches zero and the settling behavior depends on $\Phi_{i,\text{init}}$ and Δ_{INJ}. In case $F_{\text{ERR}} \neq 0$, the accumulated phase error ($2\pi\alpha N$), where $\alpha = F_{\text{ERR}}/F_{\text{OUT}}$, in each injection period has to be compensated to maintain the lock condition, in steady state. By

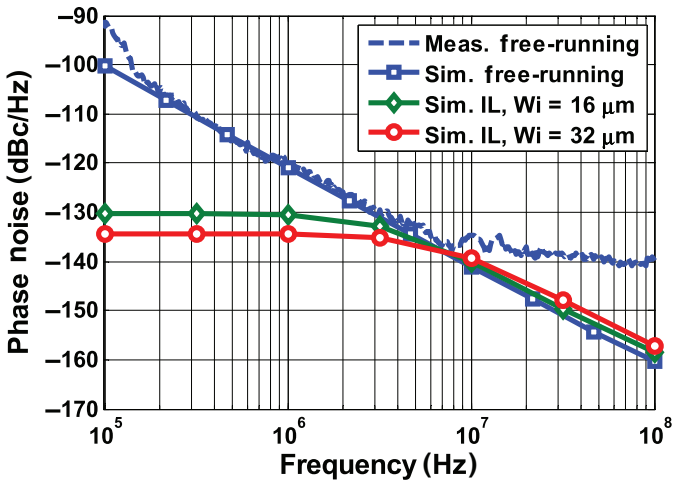

Fig. 12. Injection-locked DCO phase noise measurement and simulation results at 6.8 GHz.

treating each period of the injected signal as a discrete-time event [6], [27], sub-harmonic ILO behavior can be described using

$$\Phi_i[n+1] = \Phi_i[n] - \Phi_o[n] - 2\pi\alpha N \tag{10}$$

where in steady state, the injection pulse will be locked with the oscillator, and their phase difference will be fixed and reach a steady-state value (i.e., $\Phi_i[n+1] = \Phi_i[n] = \Phi_{i,\text{ss}}$). The steady-state condition $\Phi_{i,\text{ss}}$ depends on the amount of excess phase required to compensate for frequency error as $\Phi_o(\Phi_{i,\text{ss}}) = -2\pi\alpha N$. From the PDR, we can find $\Phi_{o,\max}$ and $\Phi_{o,\min}$ where there is no injection strength $\beta(\Phi_i) = 0$ [see

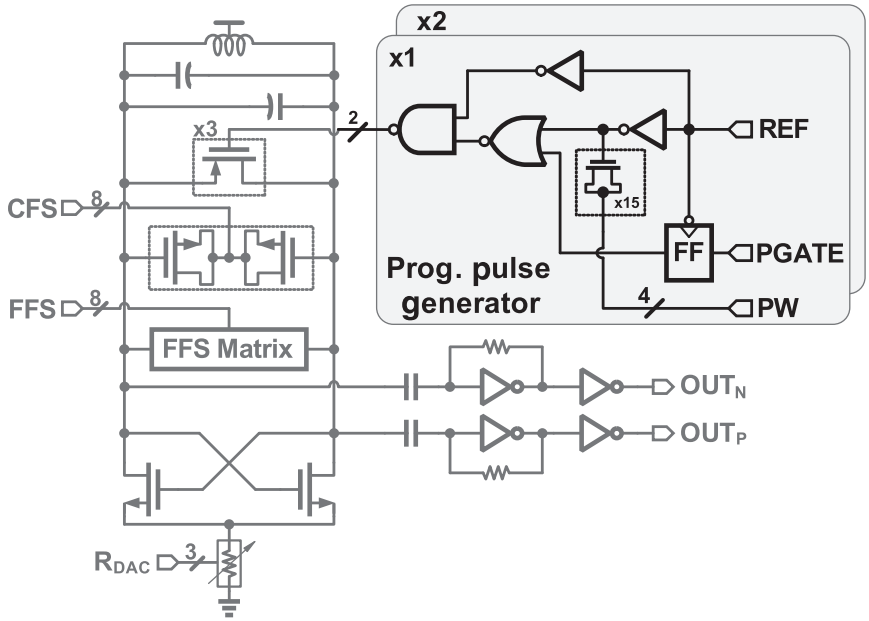

Fig. 13. Schematic of the programmable pulse generator.

Fig. 8(c)]. Then, the lock-in boundaries can be deduced from $\alpha_{\max} = -\Phi_{o,\min}/(2\pi N)$ and $\alpha_{\min} = -\Phi_{o,\max}/(2\pi N)$.

To validate the accuracy of the proposed analysis, PDR is extracted using transient simulations, similar to [27] and [28], for an 8 GHz LC oscillator under injection. As shown in Fig. 9, the PDR simulation results match theoretical analysis for various pulse widths (D) and switch resistances (R_{sw}). Even in case of a very strong injection (R_{sw} = 10 Ω and $\beta \to 1$) as shown in Fig. 9(c), the analysis captures ILO's nonlinear behavior accurately. The asymmetric nature of the PDR can be readily observed especially as D increases [see Fig. 9(b)]. Because of finite width of the pulse, pulse injection ability in delaying the oscillator phase is higher than advancing it. This asymmetry is captured accurately using the proposed analysis compared to the analysis with thin pulse assumption [14].

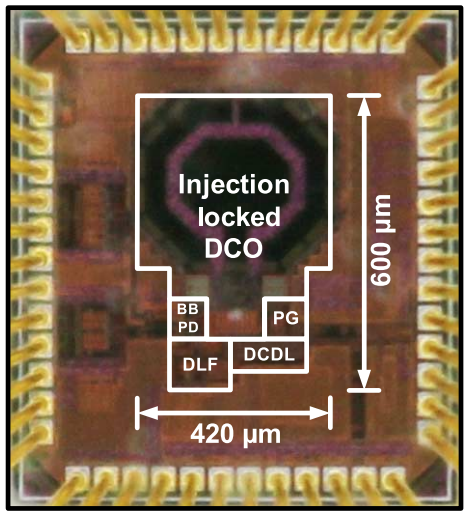

Fig. 14. Die photograph.

D. Phase Noise Analysis

In this section, we will analyze the phase noise behavior of sub-harmonic ILO, then employ it into a complete linear model for the whole ILCM architecture. Fig. 10(a) depicts a phase domain model of sub-harmonic ILO based on (10) [6], [27]. For purpose of noise analysis, the nonlinear PDR can be substituted by its slope $\beta(\Phi_{i,\text{ss}})$ where $\Phi_{i,\text{ss}}$ is a function of frequency error α. Reference clock and DCO phase noise are represented by their respective power spectral densities $S_{\Phi_{\text{nR}}}$ and $S_{\Phi_{\text{nDCO}}}$. The total output phase noise $S_{\Phi_{\text{OUT}}}$ can be calculated using

$$S_{\Phi_{\text{OUT}}} = \left|\frac{N\,\beta(\alpha)}{1-(1-\beta(\alpha))\,z^{-1}}\right|^2 S_{\Phi_{\text{nR}}} + \left|1-\frac{\beta(\alpha)\,z^{-1}}{1-(1-\beta(\alpha))\,z^{-1}}\right|^2 S_{\Phi_{\text{nDCO}}} \quad (11)$$

where reference phase noise is low-pass filtered and DCO phase noise is high-pass filtered before they appear at the output. The filter bandwidth depends on the injection strength $\beta(\alpha)$. From the PDR analysis, as frequency error deviates from zero, $\beta(\alpha)$ drops and accordingly the filtering bandwidth drops and the phase noise performance is degraded. Recently, rigorous phase noise analysis of ILO in [28] predicts the existence of the additional contribution due to power spectrum folding of oscillator phase noise. This arises from the sub-sampling of noise operated by pulse injection and it degrades the output phase noise over free-running phase noise at offset frequencies near F_{REF} by almost 3 dB [28].

Fig. 10(b) shows the discrete-time phase-domain linear model of the ILCM. This linear model is used for stability and noise analysis of the ILCM system. Unlike a PLL, the oscillator tracks the reference clock through two paths: injection path and tuning path. The sub-harmonic ILO model is simplified as a discrete-time integrator and a delay element. The FTL

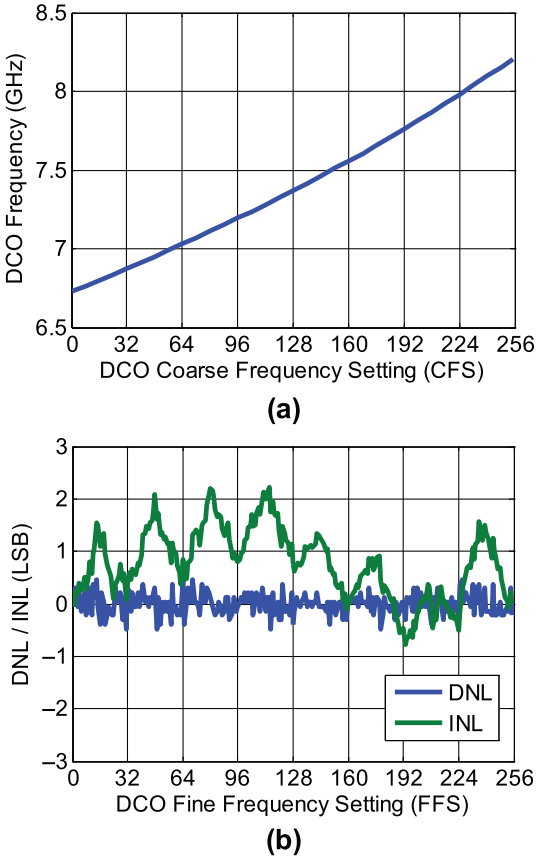

Fig. 15. Measured DCO tuning characteristics. (a) Coarse tuning. (b) Fine tuning DNL/INL.

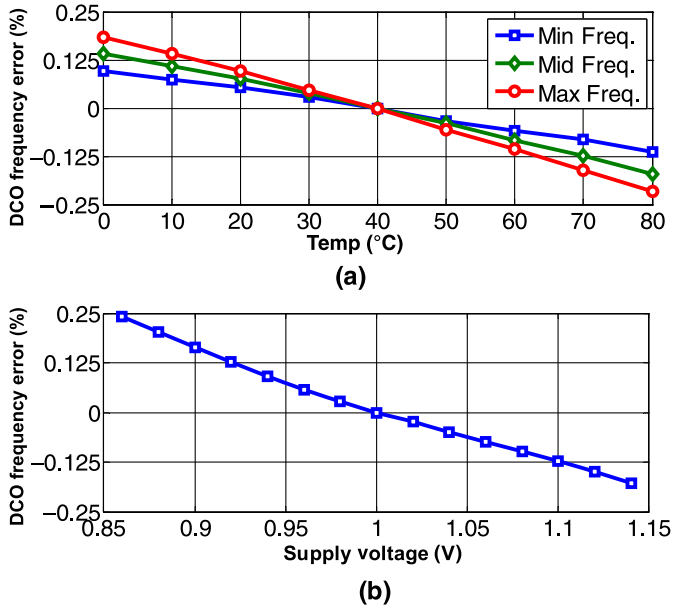

Fig. 16. Measured DCO free-running frequency across (a) temperature and (b) supply.

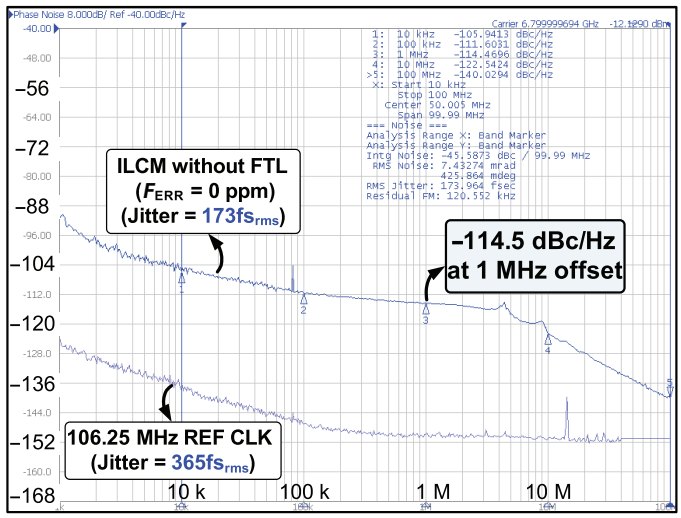

Fig. 17. Measured phase noise of the reference clock and ILCM output without FTL in case of $F_{\mathrm{ERR}} = 0$ at 6.8 GHz.

behaves as a bang-bang DFLL. The frequency tuning of DCO is modeled as an integrator in z-domain with gain $2\pi K_{\mathrm{F}} T_{\mathrm{R}}$, where K_{F} (Hz/LSB) is the DCO gain and $T_{\mathrm{R}} = 1/F_{\mathrm{REF}}$ is the reference period. The BBPD is represented by its linearized gain (K_{BBPD}). As the DCDL delays the reference clock before BBPD, it can be modeled as a combination of a summing block and a gain K_{DL} (rad/LSB). The DLL and frequency tuning accumulators have transfer functions of $H_{\mathrm{p}}(z)$ and $H_{\mathrm{i}}(z)$, respectively. The DLL random and quantization noise sources are modeled as input-referred phase noise whose power spectral density is $S_{\Phi_{\mathrm{nDLL}}}$, while DCO quantization noise has a power spectral density $S_{Q_{\mathrm{DCO}}}$. The total output phase noise $S_{\Phi_{\mathrm{OUT}}}$ can be calculated using

$$\begin{aligned} S_{\Phi_{\mathrm{OUT}}} = &\left|NTF_{\mathrm{R}}(z)\right|^2 S_{\Phi_{\mathrm{nR}}} + \left|NTF_{\mathrm{DCO}}(z)\right|^2 S_{\Phi_{\mathrm{nDCO}}} \\ &+ \left|NTF_{\mathrm{DCO}}(z) \times \left(\frac{2\pi K_{\mathrm{F}} T_{\mathrm{R}}}{1 - z^{-1}}\right)\right|^2 S_{Q_{\mathrm{DCO}}} \\ &+ \left|NTF_{\mathrm{DCO}}(z) H_{\mathrm{DLL}}(z) H_{\mathrm{i}}(z) \times \left(\frac{2\pi K_{\mathrm{F}} T_{\mathrm{R}}}{1 - z^{-1}}\right)\right|^2 S_{\Phi_{\mathrm{nDLL}}} \end{aligned} \tag{12}$$

where $NTF_{\mathrm{R}}(z)$ and $NTF_{\mathrm{DCO}}(z)$ are the noise transfer functions of reference and DCO phase noise, respectively. Because the injection path has a much higher bandwidth than the tuning path, $NTF_{\mathrm{R}}(z)$ and $NTF_{\mathrm{DCO}}(z)$ can be approximated as in (11). The $H_{\mathrm{DLL}}(z)$ represents a high-pass transfer function of the DLL

$$H_{\mathrm{DLL}}(z) = \frac{K_{\mathrm{BBPD}}}{1 + K_{\mathrm{BBPD}}\, K_{\mathrm{DL}}\, H_{\mathrm{p}}(z)}. \tag{13}$$

Because of the low bandwidth of the frequency tuning path, the FTL noise is filtered, such that the output phase noise is mainly determined by reference and oscillator phase noise. The analysis shows the great dependence of ILCM phase noise performance on the relative frequency error (α). As $NTF_{\mathrm{R}}(z)$ and $NTF_{\mathrm{DCO}}(z)$ depend on the injection strength ($\beta(\alpha)$), the phase noise performance is degraded considerably as α deviates from zero. This illustrates the importance of the proposed FTL to achieve robust operation and excellent performance across voltage and temperature variations.

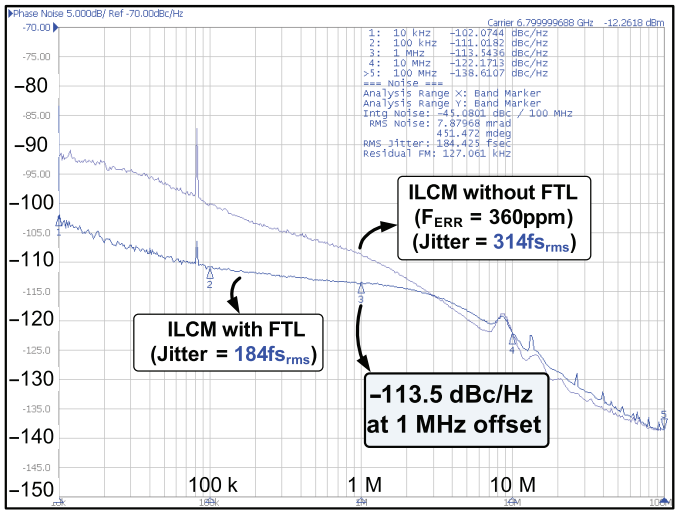

Fig. 18. Measured ILCM phase noise with FTL at (a) 6.8 GHz and (b) 8 GHz.

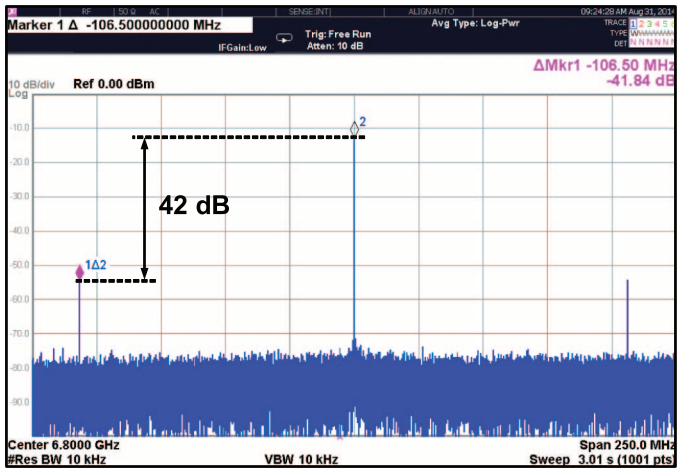

Fig. 19. Measured output spectrum of the proposed ILCM with FTL (at 6.8 GHz, $N = 64$).

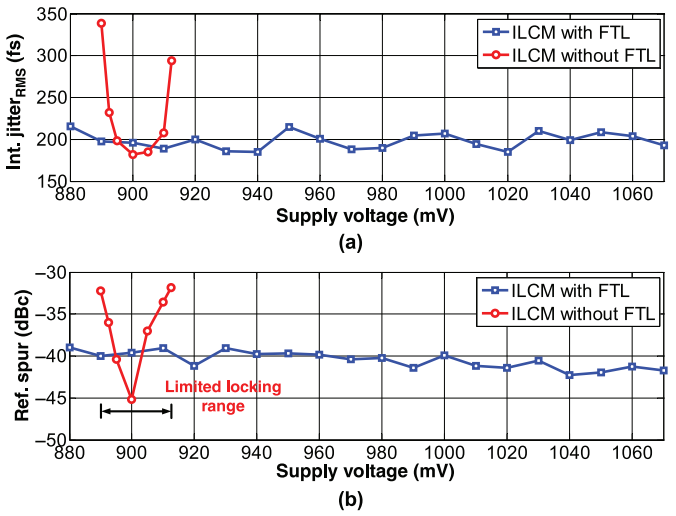

Fig. 20. (a) Measured integrated jitter and (b) measured reference spur versus supply voltage with and without FTL.

IV. Building Blocks

A. DCO

The schematic of the 16 bit LC DCO is shown in Fig. 11. It consists of an NMOS cross-coupled pair, a resistive bias network, a PMOS injection switch, and a high Q LC tank. A single-turn center-tapped 425 pH inductor is implemented using ultra-thick metal layer to maximize its quality factor. This helps to reduce DCO's power consumption and temperature sensitivity. The tail bias current is controlled digitally by $RDAC$[2:0]. Frequency tuning is realized using two MOS capacitor banks (8-bit coarse and 8-bit fine). The coarse capacitor bank is implemented using binary weighted MOS capacitors to tune the frequency from 6.75 to 8.25 GHz with a step size of about 6 MHz. The fine capacitor bank is implemented using minimum size devices to achieve fine resolution of 17 ppm/LSB at 6.8 GHz. Two-dimensional (2-D) (4×4) binary-to-thermometer decoder is used to achieve good tuning linearity with reasonable number of control lines [30]. The 4 LSBs (FFS[3:0]) are decoded to control 16 rows via R[15:0], while the 4 MSBs (FFS[7:4]) are decoded to control 16 columns via C[15:0] and A[15:0]]. R, C, and A controls are latched outside the varactor array, to avoid any coupling between RF lines and reference clock. Even and odd local decoders with matrix switching are used to realize zigzag switching order with only one (R, C, or A) control line changing at a time to eliminate any glitch. The proposed varactor control scheme guarantees monotonicity and helps to achieve excellent linearity.

The DCO core is optimized to minimize power consumption, as the required phase noise performance is relaxed by injection locking. The DCO core consumes about 2 mA from a 1 V supply at 6.8 GHz. Fig. 12 shows measured and simulation results of the DCO at 6.8 GHz when it is free-running and when it is injection locked ($N = 64$) using two different widths for injection transistor. The measured free-running DCO phase noise is around -120 dBc/Hz at 1 MHz offset, which translates to an FoM_{VCO} of -193.6 dB. We notice that injection

TABLE I
ILCM PERFORMANCE SUMMARY

	Helal [13] JSSC'09	Huang [14] JSSC'13	Lee [15] ISSCC'13	Musa [11] JSSC'14	Chien [12] ISSCC'14	This Work
Architecture	LC–ILCM	LC–ILPLL	LC–ILPLL	Ring–ILCM	Ring–ILCM	LC–ILCM
Technology (nm)	130	180	65	65	20	65
Supply (V)	1.2	1.8	1.2	1.0	1.25/1.0	0.9
Output Freq. (GHz)	3.2	2.4	2.4	0.5–1.6	15	6.75–8.25
Ref. Freq. (MHz)	50	150	150	125–400	1875	105–129
Mult. Factor (N)	64	16	16	4	8	64
Ref. Spur (dBc)	–63.9	–40	–48.8	–57	–48	–40
In–band PN (dBc/Hz)*	–127	–126.5	–123.5	NA	NA	–119.2
Ref. Integrated Jitter (fs_{rms})	80 1k–20MHz	75 1k–40MHz	75 1k–40MHz	NA	366 100k–1GHz	365 10k–40MHz
Output Integrated Jitter (fs_{rms})	130 100–40MHz	145 1k–40MHz	188 1k–40MHz	700 10k–40MHz	268 100k–1GHz	190 10k–100MHz
Power (mW)	28.6	12.6	5.2	0.97	46.2	2.25
Power Eff. (mW/GHz)	**8.94**	**5.25**	**2.17**	**0.8**	**3.08**	**0.33**
FoM_J (dB)**	**–243**	**–246**	**–247**	**–243**	**–235**	**–251**
Continuous Frequency Tracking	Digital (GRO–TDC)	Analog PLL	Analog SSPLL	Digital (VCO replica)	No	Digital (pulse gating)
Area (mm^2)	0.4†	0.64	0.25	0.022	0.044	0.25

*Normalized IBPN to 3.2 GHz.
†Use external loop filter.
**$\mathrm{FoM_J} = 10\log\left[\left(\frac{\sigma_{\mathrm{rms}}}{1\mathrm{sec}}\right)^2 \frac{\mathrm{P}}{1\ \mathrm{mW}}\right]$.

locking increases phase noise by almost 3 dB at higher offset frequencies as demonstrated by [28].

B. Pulse Generator and Other Blocks

The schematic of the pulse generator is shown in Fig. 13. It generates a narrow pulse using the positive edge of reference clock (REF) and injects it into the DCO using a 2 bit programmable PMOS switch. The pulsewidth can be varied from 20 ps to 35 ps using 4-bit digitally controlled delay cell to control injection strength and filtering bandwidth. A NOR gate implements the injection gating functionality after synchronization with REF negative edge.

The 10 bit digitally controlled delay line (DCDL) is implemented using a cascade of 16 identical delay cells similar to [31]. Each delay stage consists of an inverter loaded with a 6 bit MOS capacitor bank followed by another inverter to restore fast rise and fall times. The DCDL provides about 150 ps incremental delay to ensure DLL locking at lowest DCO frequency. The SS BBPD is implemented using a sense amplifier (SA)-based flip–flop followed by a symmetric latch to minimize the hysteresis [32].

V. MEASUREMENT RESULTS

The proposed ILCM depicted in Fig. 7 was fabricated in 65 nm CMOS process and its die photograph is shown in Fig. 14. It occupies 0.25 mm^2 active area. The total power consumption is less than 2.25 mW at a supply voltage of 0.9 V, of which the DCO and its buffer consume less than 1.8 mW. The chip is characterized using Agilent N9000A spectrum analyzer (SA) and Agilent E5052B signal source analyzer (SSA). The measured coarse tuning curve of the DCO is shown in Fig. 15(a). The output frequency is tuned from 6.75 to 8.25 GHz with about 6 MHz step by controlling the 8 bit coarse capacitor bank. A small coarse step is employed to guarantee at least 200% overlap between coarse and fine tuning curves. The fine tuning characteristics is measured at 6.8 GHz, where the approximate frequency resolution (1LSB) is 115 kHz (17 ppm). The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the fine tuning are shown in Fig. 15(b). The effectiveness of the proposed zigzag switching order is validated by the excellent DNL/INL performance. The DNL measurement also includes error due to the free-running DCO noise. The sensitivity of the DCO to voltage and temperature variations is measured and the results are shown in Fig. 16.

When the supply voltage is varied from 0.85 to 1.15 V, the frequency only changed by less than $\pm 0.25\%$ when the output frequency is 6.75 GHz. This variation is largely due to change in the DCO amplitude with the supply due to the resistive bias network. The variation across temperature is less than $\pm 0.20\%$ at 8.25 GHz and improved as the tank capacitance increases to less than $\pm 0.125\%$ at 6.75 GHz.

The performance of the ILCM is characterized using an external 106.25 MHz reference clock that has about 0.36 ps_{rms} measured integrated jitter from 10 kHz to 40 MHz and a noise floor of -150 dBc/Hz as shown in Fig. 17. The measured phase noise of the open loop ILCM without FTL at 6.8 GHz is depicted in Fig. 17. In case of a zero F_{ERR} and 64 multiplication factor, an excellent jitter of 173 fs_{rms}, integrated from 10 kHz to 100 MHz, is achieved, which is limited only by the reference clock noise. However, in the presence of a frequency error F_{ERR}, the performance of the open loop oscillator degrades considerably as depicted in Fig. 18(a). The integrated jitter increases from 173 fs_{rms} to about 314 fs_{rms} when $F_{ERR} = 360$ ppm. When the FTL is enabled using a pulse gating rate of 1/8, F_{ERR} is corrected and the excellent jitter performance is recovered. The integrated jitter is about 184 fs_{rms}, independent of F_{ERR}. This indicates that FTL adds less than 50 fs_{rms} of noise to the ILCM. Similar jitter performance is achieved across the entire frequency range. Fig. 18(b) shows the measured phase noise plots at 8 GHz with FTL and without FTL ($F_{ERR} = 0$). We also observe that pulse gating ($= 1/4$) causes slight reduction in the noise filtering bandwidth.

The measured output spectrum of ILCM with FTL at 6.8 GHz is shown in Fig. 19, where the measured reference spur is around -42 dBc. The effectiveness of the proposed FTL to desensitize the performance across voltage variations is demonstrated by measuring reference spur and integrated jitter across supply voltages ranging from 0.88 to 1.08 V (see Fig. 20). The measured DCO free-running frequency varied by 20 MHz in this range, which is about $8\times$ the lock-in range. The conventional ILCM loses lock beyond 25 mV supply variation, while the proposed FTL maintains lock with an integrated jitter ranging from 180 fs_{rms} to 215 fs_{rms}. The measured reference spur is around -40 dBc across the entire supply range.

The performance summary and comparison with state-of-the-art ILCMs are shown in Table I. The proposed architecture achieves excellent jitter and spurious performance even with a large multiplication factor of 64. Compared to prior arts, which either rely on a complex power hungry architecture [13] or sensitive analog approaches [14], [15], the proposed FTL is based on a simple and accurate digital pulse gating technique that ensures robust operation across PVT variations. The proposed architecture achieves the best power efficiency of 0.33 mW/GHz and the best-reported FoM of -251 dB. This FoM is defined by [33] to reflect the jitter power tradeoff in clock multipliers as plotted in Fig. 21(a) for state-of-the-art integer-N clock multipliers. However, in practice, achieving excellent FoM is more challenging at higher frequencies especially as the multiplication factor (N) increases. To clarify this, Fig. 21(b) plots the FoM and the output frequency of state-of-the-art integer-N clock multipliers. This work achieves

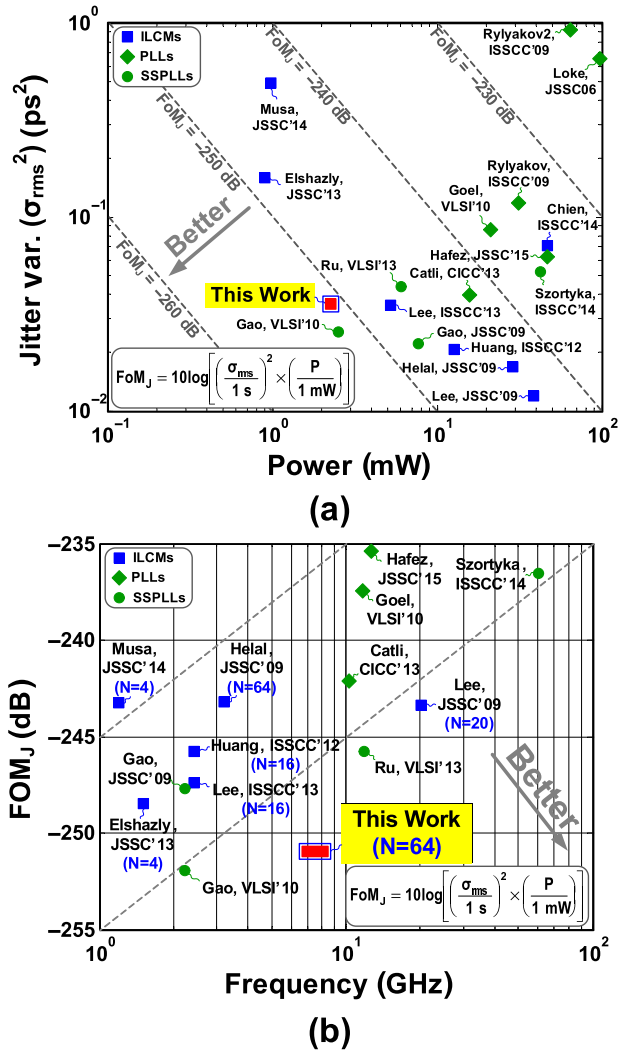

Fig. 21. FoM comparison. (a) Jitter and power comparison. (b) FoM as a function of output frequency.

at least 3 dB improvement in state-of-the-art FoM even while using a large multiplication factor of 64.

VI. Conclusion

Sub-harmonically, ILCMs provide a simple means to achieve superior jitter performance. While ILCMs offer many advantages in terms of phase noise, power, and area compared to classical PLLs, they suffer from a narrow lock-in range especially at a large multiplication factor (N). Because of the variations in the oscillator free-running frequency, in practice, the performance of ILCMs is vulnerable against process, voltage, and temperature (PVT). In this work, a low-phase noise 6.75–8.25 GHz ILCM is presented. It employs an all-digital continuous FTL to ensure robust operation across PVT variations even with a narrow lock-in range. This enables achieving low-power operation and large multiplication factor of 64. The measured jitter is only 190 fs_{rms} integrated from 10 kHz to 100 MHz. The power consumption is less than 2.25 mW from 0.9 V supply voltage for an output frequency range of 6.75–8.25 GHz. This translates to an excellent FoM of -251 dB. This

paper also introduced an accurate theoretical analysis for PDR of ILOs. Compared to ISF-based models, the proposed PDR analysis captures the large-signal behavior of pulse injection, provides accurate analytical prediction of asymmetric lock-in range, injection strength, tracking bandwidth, locking time, and phase noise performance of ILCMs.

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