A 3.7mW 3MHz Bandwidth 4.5GHz Digital Fractional-N PLL with -106dBc/Hz In-band Noise using Time Amplifier Based TDC

Ahmed Elkholy, Tejasvi Anand, Woo-Seok Choi, Amr Elshazly*, Pavan Kumar Hanumolu
University of Illinois, Urbana, IL, USA, *Oregon State University, Corvallis, OR, USA
E-mail: elkholy2@illinois.edu

Abstract

A digital fractional-N PLL that employs a time amplifier based TDC and a truly fractional divider to achieve low in-band noise with a wide bandwidth of 3MHz is presented. Fabricated in 65nm CMOS process, the prototype PLL consumes 3.7mW at 4.5GHz output frequency and achieves better than -106dBc/Hz in-band noise and 490fs$_{rms}$ integrated jitter. This translates to a FoM$_J$ of -240.5dB, which is the best among the reported fractional-N PLLs.

Introduction

The design of a low noise wide bandwidth (BW) digital fractional-N phase locked loop (PLL) is challenging due to conflicting BW requirements imposed by oscillator phase noise and the quantization error introduced by the time to digital converter (TDC) and fractional divider. A high resolution TDC is commonly used to achieve low phase noise at the expense of high power consumption [1]. Cancellation techniques are used to suppress divider quantization error but such schemes complicate the design and mandate a wide TDC range greater than one VCO period, which further degrades power efficiency [1]. Recently, digital-to-time converters (DTCs) were introduced to implement truly fractional dividers, thus alleviating the range requirements of the TDC [2]. Using only a bang-bang phase detector (BBPD), excellent phase noise performance was demonstrated [2]. However, [2] suffers from two main drawbacks. First, large BBPD quantization error limits the BW (300kHz) and sets the in-band phase noise level (-101dBc/Hz for 3.6GHz output). Second, BBPD gain depends on input jitter, which makes the loop dynamics difficult to control [3]. In this paper, we present a DTC-based digital fractional-N PLL with a high-resolution low power time amplifier (TA) based TDC (TA-TDC). The proposed TA improves the resolution of a conventional TDC by 16X, which helps to extend the PLL BW to higher than 3MHz (F_{REF}/16), and reduce in-band noise to less than -106dBc/Hz at 4.5GHz output frequency.

Proposed Architecture

Figure 1 shows the block diagram of the proposed fractional-N PLL. It consists of a TA-TDC, digital loop filter, LC-based digitally controlled oscillator (DCO) and fractional divider. The 4-bit TA-TDC digitizes the phase error between reference and feedback clocks and feeds it to a proportional-integral digital loop filter that drives the 14-bit DCO. The filter coefficients, K_P and K_I, are digitally programmable to control BW. A ΔΣ DAC truncates the 14-bit control word (D_{CTRL}) to control 5-bit thermometer-coded current DAC. A second order RC post filter suppresses the shaped quantization noise of the DAC and controls VCO varactors. The output frequency is tuned using two scaled banks of capacitors; a MIM capacitor bank provides coarse control while a MOS capacitor bank provides fine control. The DCO output is divided using a fractional divider composed of

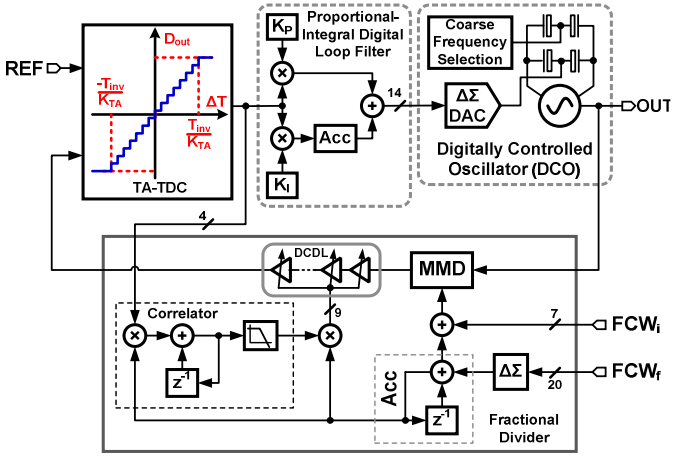

Fig. 1: Block diagram of the proposed digital fractional-N PLL.

a 6 stage multi-modulus divider (MMD) followed by a 9-bit digitally controlled delay line (DCDL) used to cancel ΔΣ quantization error. The DCDL consists of 8 identical cascaded inverter-based delay cells with a digitally controlled output capacitance. To accurately cancel ΔΣ quantization error under different PVT conditions, the DCDL range is calibrated, to be equal to one oscillator period, by scaling the DCDL control word with a gain factor K_{DCDL}. An LMS algorithm determines K_{DCDL} in a background manner by correlating the ΔΣ quantization error with the TDC output [2]. By using the proposed TA-TDC, the convergence time of the LMS background loop is improved by 10X, as 4-bits are used for correlation instead of only 1-bit in [2].

The TA-TDC implementation is shown in Fig. 2. It consists of a time amplifier, phase-frequency detector (PFD), and 4-bit TDC. The TA amplifies the input time difference and drives a 3-state PFD whose outputs are denoted as UP and DN. The TDC digitize the difference between the UP and DN pulses into 4-bits. The final TA-TDC output ranges from -7.5 to +7.5 with a step size of 1, which allows the PLL to lock without static phase offset. The TA is implemented using cross-coupled inverters consisting of two pull-down paths, namely the main and dependent paths to discharge the output. Early input makes the late input slower by reducing the strength of the dependent path, resulting in an amplified time difference (see Fig. 2) [4]. The TA gain depends on the ratio between the main and dependent paths (1-16X), which is controlled using a 5-bit word (KTA). The TDC is composed of two separate 3-bit TDCs, TDC_P and TDC_N, that digitize the magnitude of time difference T_{UP}-T_{DN} and T_{DN}-T_{UP}, respectively, while a separate BBPD determines the sign. Each of the 3-bit TDCs is implemented using a conventional 7-stage inverter-based delay line. The TDC resolution is equal to one inverter delay, which is about 15ps in 65nm technology. TDC nonlinearity is reduced by making rise/fall times small and matching t_{LH} and t_{HL} propagation delays. Leveraging a high

gain TA and simple TDC architecture, the proposed TA-TDC achieves sub-1ps resolution at low power consumption.

Measurement Results

The fractional-N PLL is implemented in a 65nm CMOS technology and occupies an active area of 0.22mm^2. At 4.5GHz, it consumes 3.7mW of which the TA-TDC consumes less than 200µW from a 1V supply. The measured phase noise plots using the proposed TA-TDC and conventional BBPD are shown in Fig. 3. The integrated jitter (10kHz to 20MHz) is 444fs$_{rms}$ and 842fs$_{rms}$ for the proposed TA-TDC and BBPD, respectively. This improvement is attributed to the reduced TDC quantization error. Fig. 4 illustrates output phase noise for different BW settings (0.75 to 3MHz). An excellent jitter of 403fs$_{rms}$ is achieved at 1.5MHz BW, which slightly increases to 455fs$_{rms}$and 528fs$_{rms}$ for 0.75MHz and 3MHz BW respectively. The measured in-band noise floor is better than -106dBc at 4.5GHz output frequency. Integrated jitter plotted as a function of output fractional frequency offset, shown in Fig. 5, indicates a worst-case jitter of 490fs$_{rms}$ with 750kHz PLL BW and it increases to 550fs$_{rms}$ at 3MHz PLL BW. The jitter increase at smaller frequency offsets is due to in-band fractional spurs. Reference spur is less than -69dBc. Fig. 6 compares the proposed fractional-N DPLL with state of the art low-jitter digital and analog fractional-N PLLs. The proposed architecture achieves lowest in-band noise along with the best power efficiency of 0.82mW/GHz. It achieves the best-reported FoM$_J$ of -240.5dB that reflects jitter and power trade-off, and at least 8dB better than other reported fractional-N PLLs when the in-band phase noise is included in FoM$_{IBPN}$.

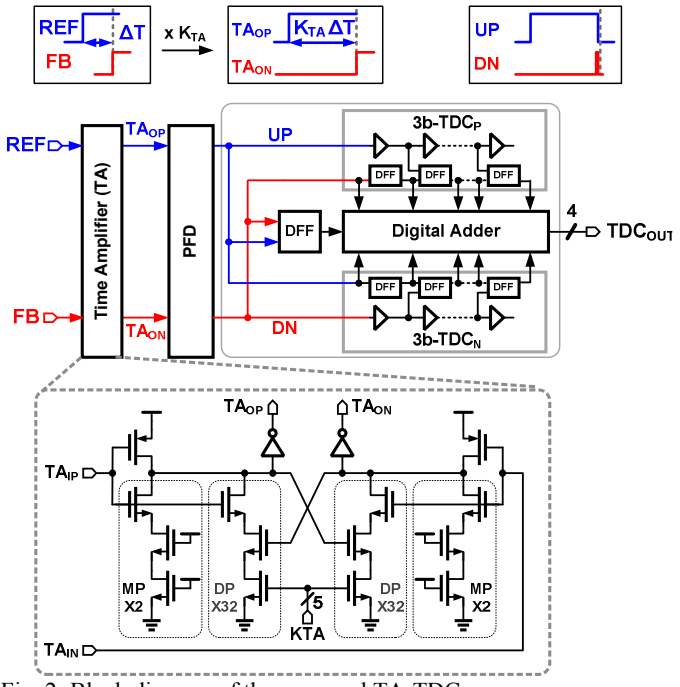

Fig. 2: Block diagram of the proposed TA-TDC.

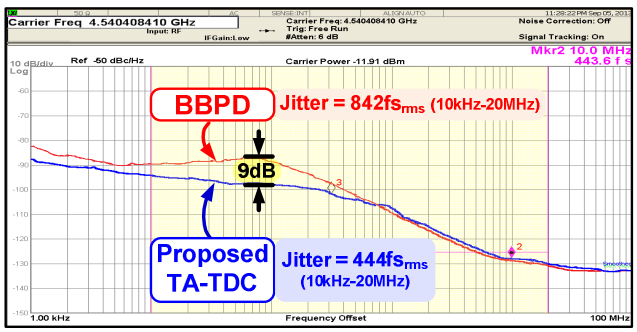

Fig. 3: Measured output phase noise at 4.5GHz output.

Acknowledgements

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References

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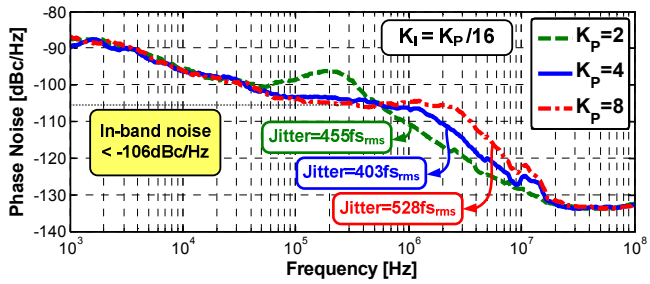


Fig. 4: Measured phase noise plots at 4.5GHz output for different BW settings: 0.75MHz, 1.5MHz, and 3MHz.

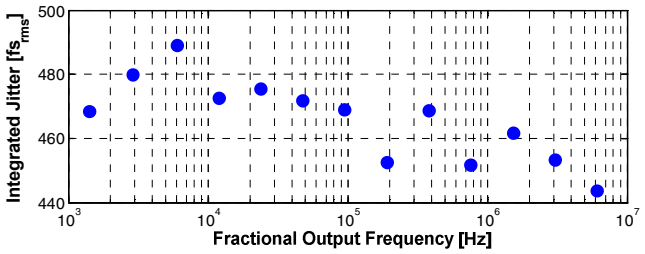
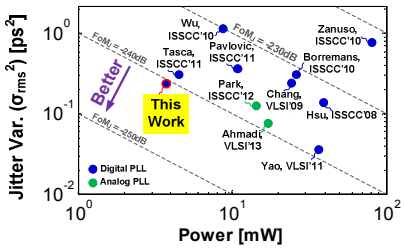


Fig. 5: Measured integrated jitter (10kHz-20MHz) at different fractional output frequencies offset from 4.5GHz.

	This Work		Hsu ISSCC'08	Tasca ISSCC'11	Yao VLSI'11	Nonis ISSCC'13
Technology [nm]	65		130	65	55	130
Supply [V]	1		1.5	1.2	1.2	1.5
Output Freq. [GHz]	4.4-5.2		3.67	2.9-4	5.9-8	0.84-1.032
Ref. Freq. [MHz]	49.1		50	40	40**	25
BW [MHz]	0.75	3	0.5	0.312	0.5	1
In-band PN [dBc/Hz]*	-102	-108	-108	-101	-107	-95
RMS Jitter [ps]	0.49	0.55	0.3	0.56	0.19	2.1
FoM$_{IBPN}$ [dB]	**-287.4**	**-293.4**	**-283.2**	**-285.1**	**-282.8**	**-277.4**
FoM$_J$ [dB]	**-240.5**	**-239.5**	**-234.5**	**-238.3**	**-238.9**	**-224.8**
Power Eff. [mW/GHz]	**0.82**		**10.82**	**1.13**	**6.1**	**7.5**
Area [mm^2]	0.22		0.95	0.22	0.68	0.25

* Normalized to 3.6GHz ** Use Reference doubler

$$FoM_J = 10\log\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \times \left(\frac{P}{1mW}\right)\right] \qquad FoM_{IBPN} = IBPN + 10\log\left[\left(\frac{1Hz}{F_{out}}\right)^2 \times \left(\frac{P}{1mW}\right)\right]$$



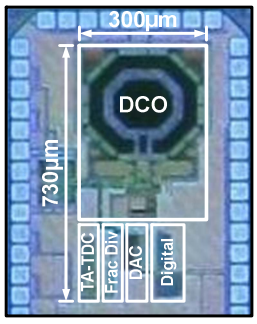


Fig. 6: Performance comparison and die micrograph.