A Sub 1µW Switched Source + Capacitor Architecture Free of Top/Bottom Plate Parasitic Switching Loss Achieving Peak Efficiency of 80.66% at a Regulated 1.8V Output in 180nm

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***Abstract*— This paper presents a 25nW-2.4µW switched-capacitor based energy harvester. The proposed harvester avoids charging and discharging of top and bottom plate parasitic capacitors by switching both the terminals of energy source as opposed to switching just one terminal. As a result, the energy lost in switching the top and bottom plate parasitic capacitors is zero joules, which helps to achieve highly efficient switched capacitor architecture for harvesting sub 1µW energy. The proposed harvester achieves an efficiency of 80% while delivering 1µW output and achieves a peak efficiency of 80.66% at 2.4µW output. It occupies an area of 1.95mm^2 in 180nm CMOS.**

***Keywords*— Harvester, switched capacitor, solar, integrated**

I. Introduction

Smart cities will need several mm size wireless sensor nodes powered by energy harvesters with the aim of deploying in an unobtrusive and concealed manner. Size limited sensor nodes limit photovoltaic cell to few millimeters in dimension, which limits the power that can be harvested. Since, several of these sensor nodes will be deployed in houses, offices, or subways, this restricts the photovoltaic (PV) cell usage to ambient light conditions (less than 200 lux). As a result, only 10s of nano-watts to a couple of microwatts power is available from the PV cell. Switched capacitor based harvester architecture is an attractive alternative to inductor-based harvester due to the absence of a large external inductor. However, conventional switched capacitor-based harvesters suffer from low energy efficiency when the harvested power is at sub-microwatt level [1-2].

Inefficiency in switched capacitors is primarily due to (a) charge redistribution loss and (b) parasitic switching loss of the charge pump. Both these losses must be reduced to achieve high efficiency. Charge redistribution loss can be reduced by (a) increasing the switching frequency or (b) increasing the capacitor size. Increasing the switching frequency increases the switching losses. On the other hand, increasing the size of the switched capacitor increases both top and bottom plate parasitic capacitors proportionally, which further increases the parasitic switching loss. This fundamental trade-off prevents the conventional switched capacitor architectures from achieving high energy-efficiency. For example, the energy efficiency for harvesting power levels of less than 1µW is approximately 50% [1-2].

The proposed switched source + capacitor architecture breaks this trade-off by eliminating the losses due to top and bottom plate parasitic capacitor switching. This allows to increase the capacitor size to reduce the charge redistribution loss without increasing losses in top and bottom plate parasitic.

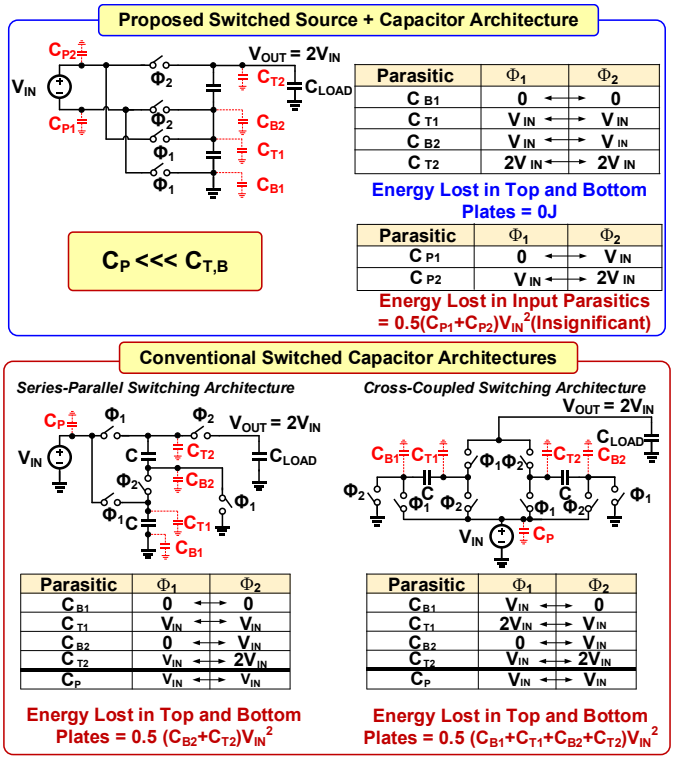


Fig. 1. Proposed parasitic insensitive switched source + capacitor concept and comparison with conventional switched capacitor architectures.

As a result, the proposed harvester can achieve ~30% higher efficiency than prior sub-microwatt switched capacitor architectures [1-2] and 3-13% higher efficiency than inductor-based harvesters [3-4] while harvesting 1µW output power.

The paper is organized as follows: Section II presents the concept of the switched source. Section III presents the system architecture, details of the MPPT and voltage regulation. Section IV presents the measured results followed by conclusion.

II. Proposed Switching Concept

Figure 1 shows the proposed parasitic insensitive switched source + capacitor converter concept and comparison with the two conventional switched capacitor architectures. In a 1:2 conventional series-parallel and cross-coupled switched capacitor architectures, the capacitors are switched to different voltages in the two phases (Φ_1 and Φ_2). This causes the top and bottom plate parasitic capacitors (C_{T1}, C_{T2}, C_{B1}, C_{B2}) to charge and discharge with a voltage difference of V_{IN} (source voltage). As a result, the energy lost in every clock cycle in a series-parallel architecture is defined as:

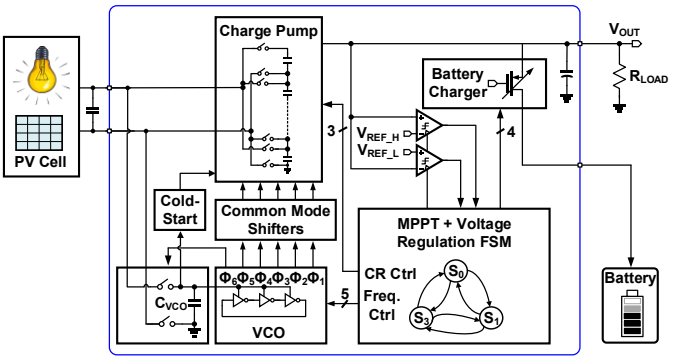


Fig. 2. Block diagram of the proposed energy harvesting system.

$$E_{Loss-SP} = \frac{1}{2}(C_{B2} + C_{T2})V_{IN}^2 \quad (1)$$

While a cross-coupled architecture the loss is defined as:

$$E_{Loss-CC} = \frac{1}{2}(C_{B1} + C_{T1} + C_{B2} + C_{T2})V_{IN}^2 \quad (2)$$

In a conventional switched capacitor architecture, this loss limits the size of the charge pump capacitance. For instance, using a hybrid MIM + fringe capacitance of 400pF would result in a combined top and bottom plate capacitance of 15.2pF capacitors. Switching this parasitic capacitor at 1V would result in energy loss of 7.6pJ and 15.2pJ per cycle for series-parallel and cross-coupled architectures, respectively.

In the proposed switched source + capacitor architecture, instead of switching the capacitors alone, the voltage source is also switched to different terminals of the capacitors, as shown in Fig. 1. Consequently, the voltage at the capacitor terminals remains constant in both phases. As a result, the top and bottom plate parasitic capacitors are neither charged nor discharged, and the energy lost in parasitic switching is 0 joules.

Despite removing the parasitic switching losses in top and bottom plate parasitic capacitors, the parasitic switching loss exist in the source terminals. This is because the source terminals are floating, and the terminal voltage changes by V_{IN} step at each clock phase. This results in losses in the parasitic capacitor from source terminal to ground. Fortunately, this parasitic capacitance is approximately 200x smaller than top and bottom plate capacitance and it depends on the switch sizes and pad capacitance, which can be minimized with careful design.

The proposed switched source + capacitor scheme differentiates itself from prior switched PV cell [5] on the fact that [5] uses multiple energy sources in series to get the desired boosted output voltage, whereas the proposed approach uses only one energy source. While this work harvests solar energy, the proposed switched source + capacitors can be leveraged to harvest from other ambient sources as well.

III. Proposed Harvester Architecture

The block diagram of the harvester is shown in Fig. 2. It consists of a programmable switched capacitor boost converter which can boost the input from 1x to 5x, a 7-stage VCO based clock generator generating 6 output phases, common mode level shifters for clock phases, battery charger with digitally programmable current sources, and an MPPT + voltage regulation FSM. An on-chip storage capacitor (C_{VCO}) is charged to the input voltage during one of the six phases and this capacitor acts as a supply to the oscillator. The proposed harvester has 3 degrees of freedom (1) conversion ratio (CR), (2) switching frequency and (3) current to charge the external battery. MPPT is achieved by controlling the conversion ratio and switching frequency, the output voltage regulation is achieved by controlling the amount of charge provided to the external battery.

On-chip comparators are used to verify that the output voltage is within the specified window of regulation. A Dickson based cold-start circuit is used to provide the supply voltage for these comparators and static level shifters that are used to program static switches.

A. Reconfigurable Charge Pump

Detailed schematic of x1-to-x5 switched source + capacitor converter is shown in Fig. 3(a). It consists of 5 x 400pF capacitors to reduce the charge redistribution loss and it requires 5 non-overlapping clock phases. Since the peak voltage of the harvester output is 1.8V, in a conventional scenario, the non-overlapping clock phases, required to turn on/off harvester switches, must have a 1.8V swing. However, rail-to-rail level shifters consume a significant amount of power. Moreover, parasitic losses in a clock distribution network for 1.8V clock signal swing are significant. Therefore, in the proposed harvester, switches are designed in such a way that only DC-shifted clock phases with a maximum voltage swing of V_{IN} is required. Fortunately, V_{IN} could be 5x smaller than 1.8V. This helps to exponentially reduce the losses in clock distribution.

The proposed switch consist of series NMOS and PMOS transistors. Turning off the switch requires turning off only one of the two transistors (either NMOS or PMOS). An example of source +ve terminal (V_{IN}+) connection to C_3 top plate and disconnection from C_2 top plate (C_3 bottom plate) is shown in Fig. 3(b). During Φ_3, V_{IN}- = $2V_{IN}$ because it is connected to top plate of C_2 resulting in $V_{IN}^+ = 3V_{IN}$. PMOS (P1) gets $2V_{IN}$ at its gate while NMOS (N1) gets $4V_{IN}$ at its gate. This turns both N1 and P1 on and connects V_{IN}^+ to C_3 top plate. Simultaneously, PMOS (P2) gets $2V_{IN}$ at its gate while NMOS (N2) gets $2V_{IN}$ at its gate. This turns off N2 and disconnects V_{IN}^+ from C_2 top plate. Fig. 3 (c) shows the detailed waveforms of all the switches with regards to time and voltage levels. An ultra-low power (1nW) common mode shifter is designed to provide the DC shifted clocks. For higher DC shift, cascading stages are used to provide higher DC shift with $1V_{IN}$ swing. The values of the common mode values are taken from the top plates of the charge pump capacitors which are V_{IN}, $2V_{IN}$, $3V_{IN}$, $4V_{IN}$ and $5V_{IN}$.

There are two types of parasitic capacitances associated with the energy source (a) coupling capacitance between the two inputs of the ambient source (C_C), and (b) parasitic capacitance to ground from the terminals of the input source (C_{P1} and C_{P2}), as shown in Fig 3(a). Coupling capacitance between the two inputs does not contribute to switching losses because both terminal voltages change with the exact same amount. The on chip parasitic capacitance from source terminals to ground is very small (37fF in this chip), which results in insignificant switching loss. Parasitic capacitance on the PCB is minimized by careful PCB design.

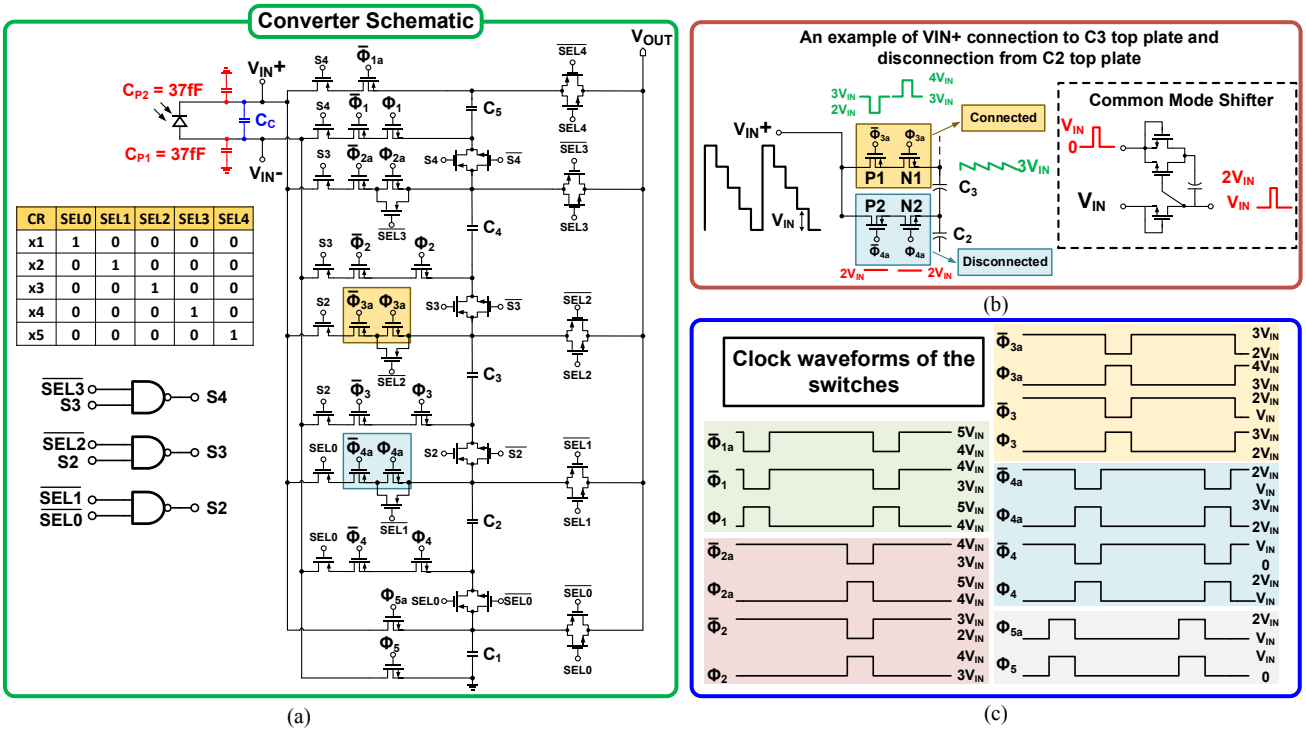


Fig. 3. (a) Schematic of the proposed programmable charge pump. (b) Switching example and common mode voltage shifter. (c) Associated clock waveforms.

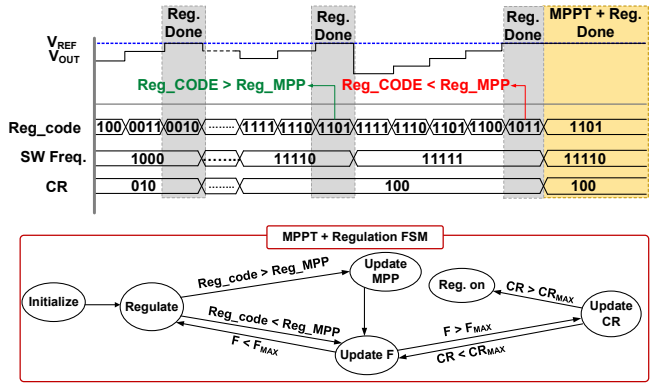


Fig. 4. Proposed MPPT and voltage regulation state machine and timing diagram

B. *MPPT and Voltage Regulation*

The proposed MPPT + voltage regulation FSM, algorithm and timing diagram is shown in Fig. 4. With a fixed output load resistance, the power harvested is maximized by maximizing the power going to charge the battery. Therefore, the aim of the proposed MPPT is to charge the battery with maximum current. The MPPT is initialized with values for the frequency code and CR code, which are set to their minimum values. Regulation starts with changing the regulation code (i.e charger current) till the output voltage is within two reference voltage levels ($V_{REF-H} > V_{OUT} > V_{REF-L}$). If the regulation fails, the switching frequency is incremented. Upon success of voltage regulation, the value of the regulation code (charger current) is checked and compared to the maximum value of regulation code from previous regulation attempts. The maximum value is saved in a register based on the result of this comparison. After all CR and frequency combinations are tested, the algorithm loads CR, frequency and regulation code configuration which corresponds to the maximum charger current (maximum output power). By using digital battery charger as a means to monitor the harvester power, power hungry current sensing circuits are avoided, which helps to further improve the harvester efficiency.

IV. Measurement Results

The proposed harvester is implemented on a 180nm CMOS technology and occupies an area of 1.95mm^2. Figure 5 shows die micro-graph. Most of the area is occupied by the charge pump capacitors to achieve the maximum possible efficiency by reducing the charge redistribution loss. A hybrid of MIM + fringe capacitor structure (MIM on top of metal cap) is used to achieve the maximum capacitance density.

Figure 6 shows the transient MPPT + voltage regulation FSM settling behavior with an input light source of 144 lux using 2 solar cells of combined area of 38.7mm^2. After the V_{OUT} is settled to 1.8V at 1.52µW output power, the harvester has a peak-to-peak ripple of 90mVp-p with an output capacitance of 510pF (external). After MPPT settling, voltage regulation ability is measured by applying the current step. For a current step of 30nA, the proposed harvester recovers to 1.8V with a voltage droop of 250mV, as shown in Fig. 6 (b).

Figure 7(a) shows the measured end-to-end energy efficiency of the harvester. The efficiency is measured as output power/ (maximum possible harvestable input power + harvester losses). The proposed harvester achieves peak end-to-end efficiency of 80.66% while delivering 2.4µW at 1.8V with the input voltage of 0.67 V. The harvester achieves efficiency >70% while harvesting >200nW and achieves ≥80% efficiency while harvesting ≥1 µW. At V_{IN} of 0.45V, resistance of the switches increases, which limits the power efficiency at high power levels as higher frequencies are needed. This leads to reaching the fast

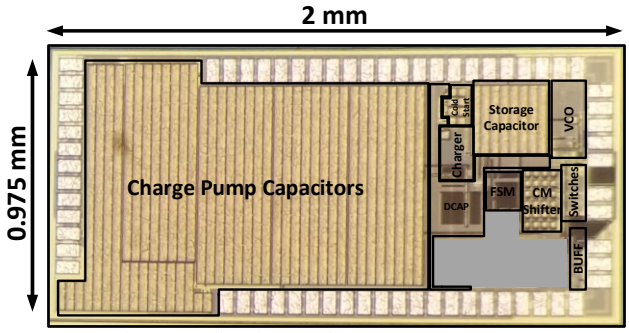


Fig. 5. Energy harvester die micrograph

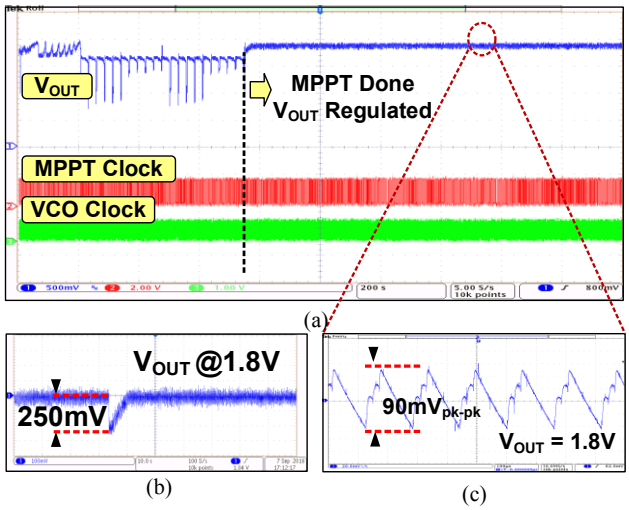
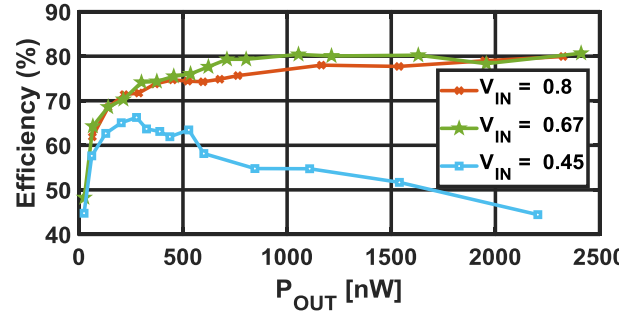


Fig. 6 Measured transient results for (a) MPPT and voltage regulation, (b) load regulation with the current step of 30n A and (c) output voltage ripple in steady state with the output power of 1.52µW and 144 lux input light



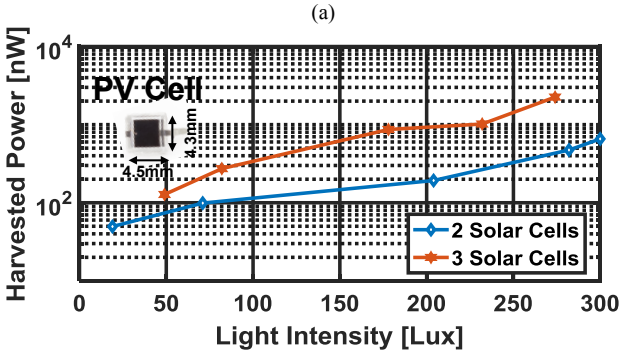


Fig. 7. (a) Measured energy efficiency versus harvester output power and (b) measured harvester output power versus light intensity.

switching limit of the converter. Figure 7(b) shows the harvester power vs. input lux using two and three 4.3mm x 4.5mm solar cells as a source. A comparison is made with prior state-of-the-art and shown in Table I. The proposed harvester achieves ~30% higher efficiency while harvesting 1µW in comparison with the prior switched capacitor harvester architectures[1][2].

V. Conclusion

This paper presents a switching approach that helps to break the trade-off between the charge redistribution loss and top/bottom plate switching loss in a switched capacitor harvester. With the proposed approach, the top/bottom plate switching loss is eliminated and charge redistribution loss is reduced to achieve an efficiency of 80% while harvesting 1µW power.

VI. Acknowledgment

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TABLE I. Comparison with State-of-the-Art Harvesters

	This work	[1]	[2]	[6]	[3]	[4]
Process	180 nm	180 nm	180 nm	180 nm	180nm	180 nm
Type	Switched Source + Capacitor	Switched Capacitor	Switched Capacitor	Inductor based	Inductor based	Inductor based
Fully Integrated	Yes	Yes	Yes	No	No	No
Output Power (W)	25n- 2.41µ	5n - 5µ	113 p - 1.5 µ	544p - 4 n	1µ-10mW	50n - 10 m
Output Voltage(V)	1.8	2.2 - 5.2	3.8 - 4	1.1 - 1.9	1 - 1.8	0.35 - 0.5
Input Voltage (V)	0.45 –0.8	0.14 - 0.5	0.25 - 0.65	20m - 70 m	NA	0.55 - 1
Harvesting Efficiency	80% (1µW)	50% (1µW)	52 %(1µW)	53% (1.2nW)	67%(1µW)	77% (1µW)
MPPT	Yes	No	Yes	No	Yes	Yes
MPPT Power	1.2nW	N/A	15pW	0.554nW	400nW	N/A
Regulation	Yes	No	No	No	Yes	Yes
Area	1.95 mm^2	0.86mm^2	2.72 mm^2	1.5275 mm^2	4.6225 mm^2	1.44 mm^2
Switching Frequency	0.3KHz – 41KHz	20KHz - 100KHz	N/A	12Hz	10 - 20 KHz	N/A

References

[1] W. Jung, et al., “An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler” IEEE J. Solid-State Circuits, pp. 2800-2811, Dec 2014

[2] X. Wu ,et al., "A 20-pW discontinuous switched-capacitor energy harvester for smart sensor applications," IEEE J. Solid-State Circuits, pp. 972-984, April 2017.

[3] K. W. R. Chew, et al. "A 400nW single-inductor dual-input-tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting," ISSCC Dig. Tech. Papers, Feb 2013, pp.68-69.

[4] P. Chen, et al., “A 50nW-to-10mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting,” ISSCC Dig. Tech. Papers, Feb 2015, pp. 1-3.

[5] I. Lee, et al., “A >78%-efficient light harvester over 100-to-100klux with reconfigurable PV-cell network and MPPT circuit” ISSCC Dig. Tech. Papers, Feb 2014, pp. 370-371.

[6] S. Bandyopadhyay et al., "A 1.1 nW energy harvesting system with 544pW quiescent power for next-generation implants", ISSCC Dig. Tech. Papers, Feb. 2014, pp. 396-397