A Calibration-Free Fractional-N Ring PLL Using Hybrid Phase/Current-Mode Phase Interpolation Method

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***Abstract*—A hybrid phase/current-mode phase interpolator (HPC-PI) is presented to improve phase noise performance of ring oscillator based fractional-N PLLs. The proposed HPC-PI alleviates the bandwidth trade-off between VCO phase noise suppression and $\Delta\Sigma$ quantization noise suppression. By combining the phase detection and interpolation functions into XOR phase detector/interpolator (XOR PD-PI) block, accurate quantization error cancellation is achieved without using calibration. Use of a digital MDLL in front of the fractional-N PLL helps in alleviating the bandwidth limitation due to reference frequency and enables bandwidth extension even further. The extended bandwidth helps in suppressing the ring-VCO phase noise and lowering the in-band noise floor. Fabricated in 65 nm CMOS process, the prototype generates fractional frequencies from 4.25 to 4.75 GHz, with in-band phase noise floor of -104 dBc/Hz and 1.5 $\mathrm{ps_{rms}}$ integrated jitter. The clock multiplier achieves power efficiency of 2.4 mW/GHz and FoM of -225.8 dB.**

***Index Terms*—Calibration-free, delta-sigma modulator, fractional-N PLL, frequency synthesizer, multiplying delay-locked loop (MDLL), phase interpolator (PI), phase noise, phase-locked loop (PLL), quantization error cancellation, ring-VCO.**

I. Introduction

FRACTIONAL-N phase-locked loops (PLLs) provide a convenient means to generate high-frequency clocks whose frequency can be controlled accurately. Conventional fractional-N PLLs are typically implemented using the charge-pump based architecture shown in Fig. 1 [1]. In addition to a phase frequency detector (PFD), loop filter, charge-pump, and a voltage-controlled oscillator (VCO), it consists of a dual modulus divider that is dithered by a delta-sigma ($\Delta\Sigma$) modulator. Because frequency division ratio of the feedback divider is restricted to only integer values (N), fractional division ratio ($\mathrm{N}+\alpha$) is obtained by switching the divide ratio between integer values using the $\Delta\Sigma$ output, $\mathrm{y[k]}$, i.e., instantaneous division ratio is equal to $\mathrm{N}+\mathrm{y[k]}$. The $\Delta\Sigma$ modulator truncates the input frequency control word and generates a sequence of integers, $\mathrm{y[k]}$, with a running average equal to the fractional division ratio, α. The quantization error introduced by the $\Delta\Sigma$ modulator is filtered by the low pass action of PLL feedback loop. The impact of quantization error on output phase noise can be reduced to negligible levels by reducing the PLL bandwidth.

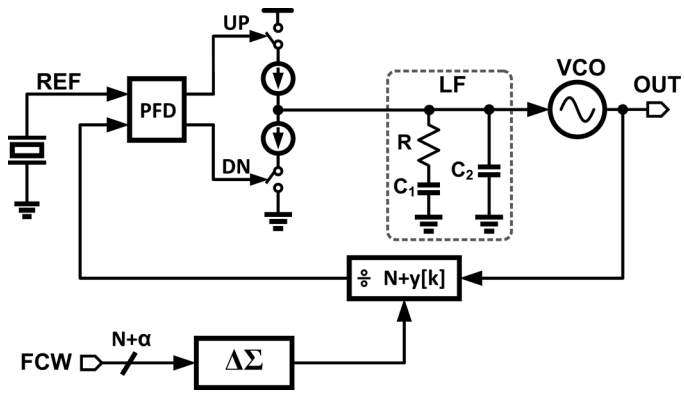

Fig. 1. Block diagram of a conventional charge-pump based fractional-N PLL.

Besides the $\Delta\Sigma$ modulator, VCO is a major source of phase noise in a fractional-N PLL. Owing to its high-pass noise transfer function, VCO phase noise can be suppressed by increasing the PLL bandwidth. Therefore, choosing the PLL bandwidth that suppresses both the $\Delta\Sigma$ quantization error and VCO phase noise adequately becomes very challenging. It is this conflicting bandwidth requirement that complicates the design of low-noise fractional-N PLLs with low power.

The noise bandwidth trade-off is quantified by using the simulated phase noise plots shown in Fig. 2. In the first case, PLL bandwidth is chosen low enough to make the contribution of quantization to the output phase noise negligible (see Fig. 2(a)). In this particular example, the bandwidth is only 250 kHz, the reference frequency is 50 MHz and the spot phase noise of the free running VCO running at 4.75 GHz is -87 dBc/Hz at

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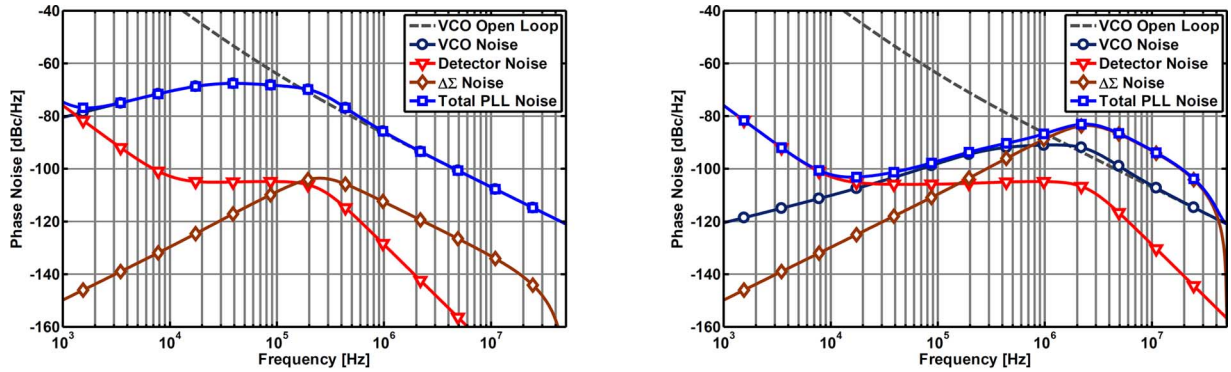

Fig. 2. Simulated phase noise plot for a charge pump based fractional-N PLL (a) using low bandwidth for $\Delta\Sigma$ quantization noise cancellation, and (b) using high bandwidth for VCO phase noise suppression.

1 MHz offset. Due to the low bandwidth, the total output phase noise is dominated by the VCO phase noise resulting in an integrated jitter of about 10 ps_{rms}, which is unacceptably large for most applications. On the other hand, when the PLL bandwidth is increased to 2.5 MHz ($\text{F}_{\text{REF}}/20$), VCO phase noise is greatly suppressed (see Fig. 2(b)). But output phase noise is dominated by $\Delta\Sigma$ quantization error resulting in an integrated jitter of more than 7 ps_{rms}, which is also large and unacceptable. This noise bandwidth trade-off makes the conventional architecture not well suited particularly for ring-VCO based PLLs because ring-VCO phase noise is significantly higher than that of LC-VCOs.

Several techniques that seek to mitigate the phase noise and bandwidth trade-off using quantization error cancellation have been proposed [2]–[5]. As described next in Section II, the effectiveness of these techniques is limited by gain mismatch between the quantization error and the cancellation paths as well as nonlinearity caused by analog circuit imperfections. As a result, complex calibration is often required to achieve high performance. In this paper, we demonstrate a ring-VCO based fractional-N PLL that employs a hybrid phase/current phase interpolator (HPC-PI) to achieve highly accurate error cancellation without using calibration. The maximum loop bandwidth to suppress ring-VCO phase noise is limited to one-tenth of the reference frequency. To overcome this, reference clock frequency to the fractional-N PLL is increased from 50 MHz to 500 MHz using an on-chip low-noise integer-N digital frequency multiplier. Fabricated in a 65 nm CMOS process, the prototype fractional-N frequency synthesizer consumes 11.6 mW power and generates fractional output frequency in the range of 4.25 to 4.75 GHz from a fixed 50 MHz reference clock. The proposed clock multiplier achieves an integrated jitter of 1.5 ps_{rms} with a power efficiency of 2.4 mW/GHz resulting in the figure of merit (FoM) of -225.8 dB.

The rest of this paper is organized as follows. Prior art on quantization error cancellation is briefly discussed in Section II with the goal of motivating the proposed PLL architecture presented in Section III. The circuit implementation details are described in Section IV. The measured results are presented in Section V, followed by a summary of the key contributions in Section VI.

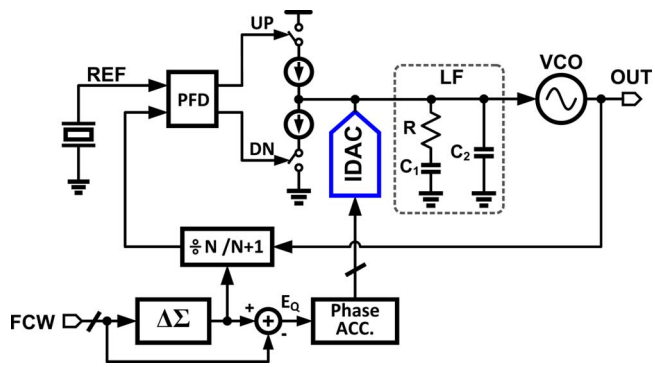

Fig. 3. Block diagram of fractional-N PLL utilizing current-mode DAC based error cancellation [2].

II. Prior Art

Quantization error cancellation is a common technique used to mitigate the bandwidth trade-off in fractional-N PLLs. As shown in Fig. 3, quantization error of the $\Delta\Sigma$ modulator (E_{Q}), is computed by subtracting its input from the output and cancelled at the output of charge pump using a current-mode digital-to-analog converter (IDAC) [2]. Because dual modulus divider acts as a phase integrator, a digital phase accumulator is needed in the cancellation path to explicitly integrate E_{Q}. In other words, IDAC outputs a current whose magnitude is equal to the amount of charge-pump current resulting from the quantization error of the $\Delta\Sigma$ modulator. Perfect cancellation of E_{Q} enables an increase in the PLL loop bandwidth to adequately suppress VCO phase noise. However in practice, the effectiveness of this approach is severely limited by gain and timing mismatch between the quantization error path through the divider, PFD, charge pump and the cancellation path through the digital phase accumulator and the IDAC. As a result, high precision analog circuitry and extensive calibration is needed to mitigate these path mismatches and to achieve acceptable performance [3].

An alternative technique shown in Fig. 4 performs quantization error cancellation at the output of the divider [4]–[6]. As before, E_{Q} is first integrated using the phase accumulator. However, in contrast to previous IDAC based approach, cancellation is performed in the phase domain by using a phase interpolator (PI), which converts phase accumulator output into phase

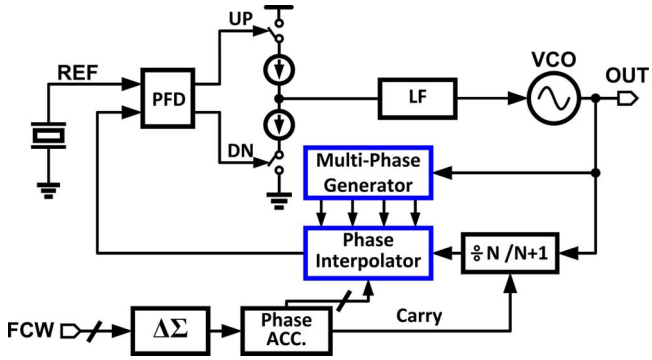

Fig. 4. Block diagram of phase interpolator based fractional-N PLL.

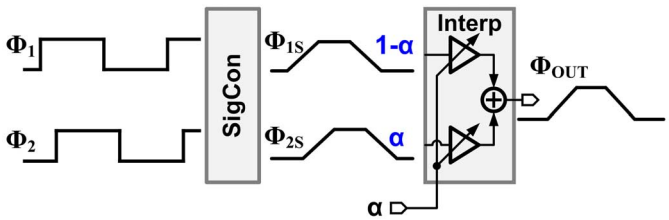

Fig. 5. Phase interpolation operation using conventional PI.

and subtracts it from the phase of the divider output. Compared to IDAC based approach, this technique is less susceptible to path mismatch because of the absence of additional phase to current conversion. Nevertheless, the effectiveness of this approach also depends on the accuracy with which cancellation path gain matches the gain of quantization error path through the divider. Therefore, the PI must be designed to have: (i) a fixed and known gain and (ii) a linear range that is large enough to cancel phase quantization error, $\Phi_{\mathrm{E_Q}}$, at the output of the divider. The range of $\Phi_{\mathrm{E_Q}}$ depends on the number of output bits of $\Delta\Sigma$ modulator. For a 1 bit output $\Delta\Sigma$ modulator, $\Phi_{\mathrm{E_Q}}$ spans one VCO period.

A PI is most commonly implemented using a two-step architecture. Two adjacent clock phases are selected from M phases based on the most significant bits (MSBs) of the input digital word. An interpolator, controlled by the remaining least significant bits (LSBs), mixes these two phases to generate the output phase. The M phases are either generated using an explicit multi-phase generator [6] or tapped off from the ring VCO itself [5].

Fig. 5 shows the basic working principle of the conventional interpolator [6]. It uses two adjacent phases Φ_1, and Φ_2, as input and generates an interpolated waveform Φ_{OUT} based on input control word, α. The interpolation operation is performed in two steps. First, inputs Φ_1, and Φ_2, are passed through a signal conditioning circuit (SigCon), which slows down the edges by increasing rise/fall times and generates outputs $\Phi_{1\mathrm{S}}$, and $\Phi_{2\mathrm{S}}$, such that both waveforms overlap during transition time. In the second step, $\Phi_{1\mathrm{S}}$, and $\Phi_{2\mathrm{S}}$, are passed through an interpolator circuit (Interp) consisting of two buffers. These buffers scale $\Phi_{1\mathrm{S}}$, and $\Phi_{2\mathrm{S}}$, by interpolation weights $1-\alpha$ and α, respectively, and the resulting buffer outputs are summed to generate the interpolated output phase, Φ_{OUT}.

An important advantage of this implementation is the gain of PI is very well defined and is equal to $2^{-\mathrm{L}} \cdot 2\pi/\mathrm{M}$ rad/LSB, where L is the number of input bits. However, the main drawback is that the PI linearity depends on several factors such as, the integral non-linearity (INL) of the multiphase generator, input waveform shapes, their rise/fall times, phase separation of the PI inputs, and the interpolator output time constant [7]. Additionally, it also depends heavily upon the inherent non-linearity of current to rise/fall time conversion process in SigCon block. The interpolation range of the conventional PI is also limited depending upon the transition time overlap between SigCon outputs, which necessitates the use of more number of phases from multi-phase generator to cover the entire interpolation range. These factors limit the PI linearity to about 4–5 bits in practice, which severely restricts the effectiveness of the PI-based quantization error cancellation approach. To overcome phase interpolator non-linearity, elaborate calibration [4] or noise-shaped segmentation techniques [8] are needed, both of which add to the design complexity.

The quantization error cancellation can also be achieved by using a delay line in-place of a phase interpolator [9] in the feedback path or in the reference clock path [10]. However, for efficient cancellation the delay line range needs to be precisely one VCO clock period. Additionally, the delay line should also be linear across the whole range of operation. To meet the gain and linearity requirements, this approach also requires additional calibration circuitry, which increases design complexity.

Even if the PLL bandwidth is extended to $\mathrm{F_{REF}}/15$ (2 MHz in [8]) using one of the above quantization error cancellation techniques, it may not be sufficient to adequately to suppress ring-VCO phase noise, especially in deep sub-micron technologies. For instance, behavioral simulations indicate integrated jitter can be as high as 2.3 $\mathrm{ps_{rms}}$ when the PLL bandwidth is chosen to be 3.5 MHz ($\mathrm{F_{REF}}/15$) and VCO phase noise is -87 dBc/Hz at 1 MHz offset. In view of these drawbacks, we present a ring-VCO based calibration-free fractional-N PLL that achieves accurate quantization error cancellation and efficient ring-VCO phase noise suppression simultaneously.

III. Proposed Architecture

A simplified block diagram of the proposed hybrid phase/current phase interpolator based fractional-N PLL is shown in Fig. 6 [11]. In addition to a conventional type-II loop filter (LF) and the ring-VCO, it consists of a HPC-PI formed by a dual modulus multi-phase divider along with XOR-based phase detector/interpolator (XOR PD-PI) block. By combining the functions of phase detection and phase interpolation in XOR PD-PI block as discussed next, this architecture eliminates the path mismatch issues associated with current-mode DAC based cancellation approach. By using a HPC-PI it mitigates the non-linearity of conventional voltage-mode phase interpolators. Thus, this architecture can accurately cancel quantization error without the need for any calibration.

A detailed block diagram of the hybrid phase/current phase interpolator is shown in Fig. 7. A divide-by-2 stage divides the VCO output and generates four equally spaced phases denoted as I, IB, Q and QB at half the VCO frequency ($\mathrm{F_{VCO}}/2$). Out

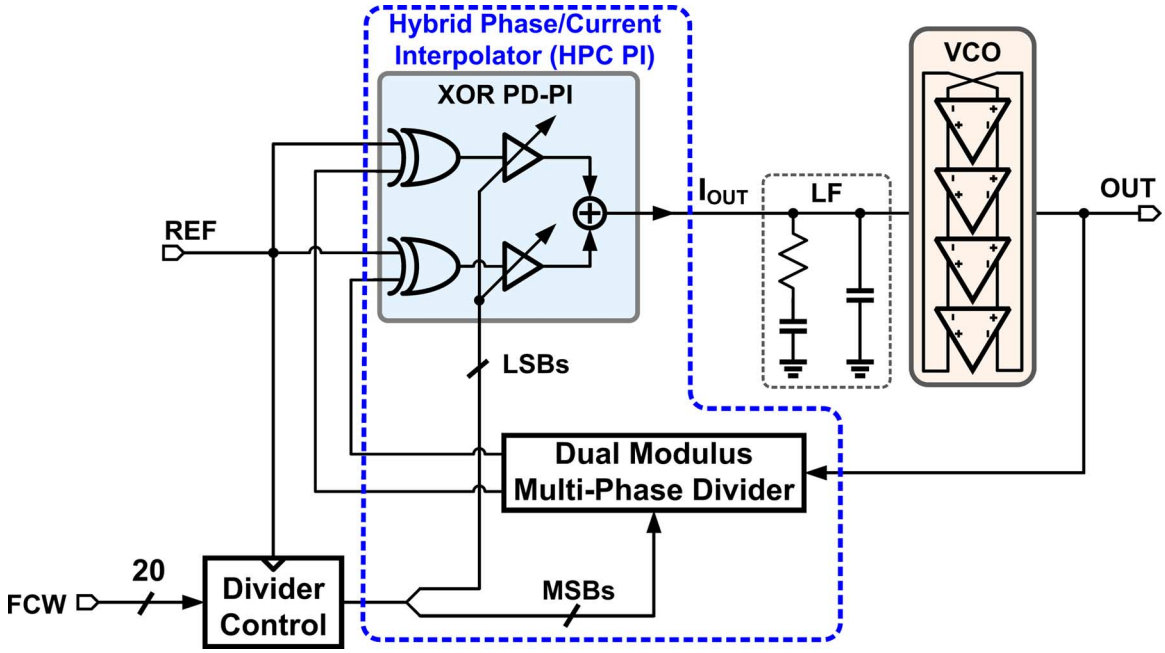

Fig. 6. Simplified block diagram of the proposed HPC-PI based PLL.

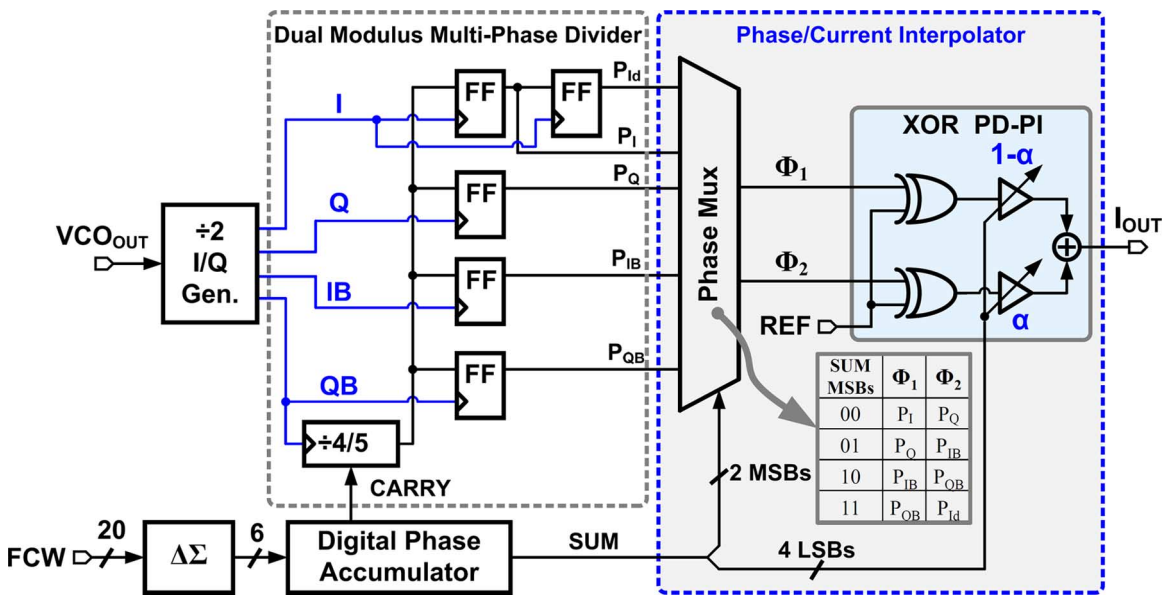

Fig. 7. Block diagram of hybrid phase/current phase interpolator (HPC-PI).

of the four phases, QB phase is fed to the dual modulus 4/5 divider that is controlled by the truncated frequency control word (FCW). A second order $\Delta\Sigma$ modulator truncates the 20 bit frequency control word into 6 bits and feeds them to a digital phase accumulator. The digital phase accumulator performs integration and modulo 2π operation to generate a 6 bit SUM output and 1 bit CARRY output. The phase accumulator can be viewed as a 1 bit first-order $\Delta\Sigma$ modulator, hence the CARRY output is used to control the divide-by-4/5 dual modulus divider. The SUM output represents the phase quantization error, Φ_{E_Q}, and is used to control the HPC-PI such that the $\Delta\Sigma$ quantization error is cancelled. This architecture maps $\Delta\Sigma$ modulator output bits directly into phase domain such that the range of quantization error is limited to $2T_{VCO}$ clock periods, irrespective of the number of bits in the modulator output.

The divider output is synchronized by all the four phases using flip-flops to generate four phases denoted as P_I, P_Q, P_{IB} and P_{QB} (see Fig. 7). Apart from theses four phases, an additional two VCO cycle delayed version of output phase P_I, called P_{Id} is also generated by synchronizing P_I again with phase I of divide-by-2 based quadrature phase generator. These phases along with the SUM output of the digital phase accumulator are fed to the HPC-PI.

The HPC-PI performs phase quantization error cancellation by interpolating between the synchronized divider output phases based on the 6 bit SUM output of the digital phase

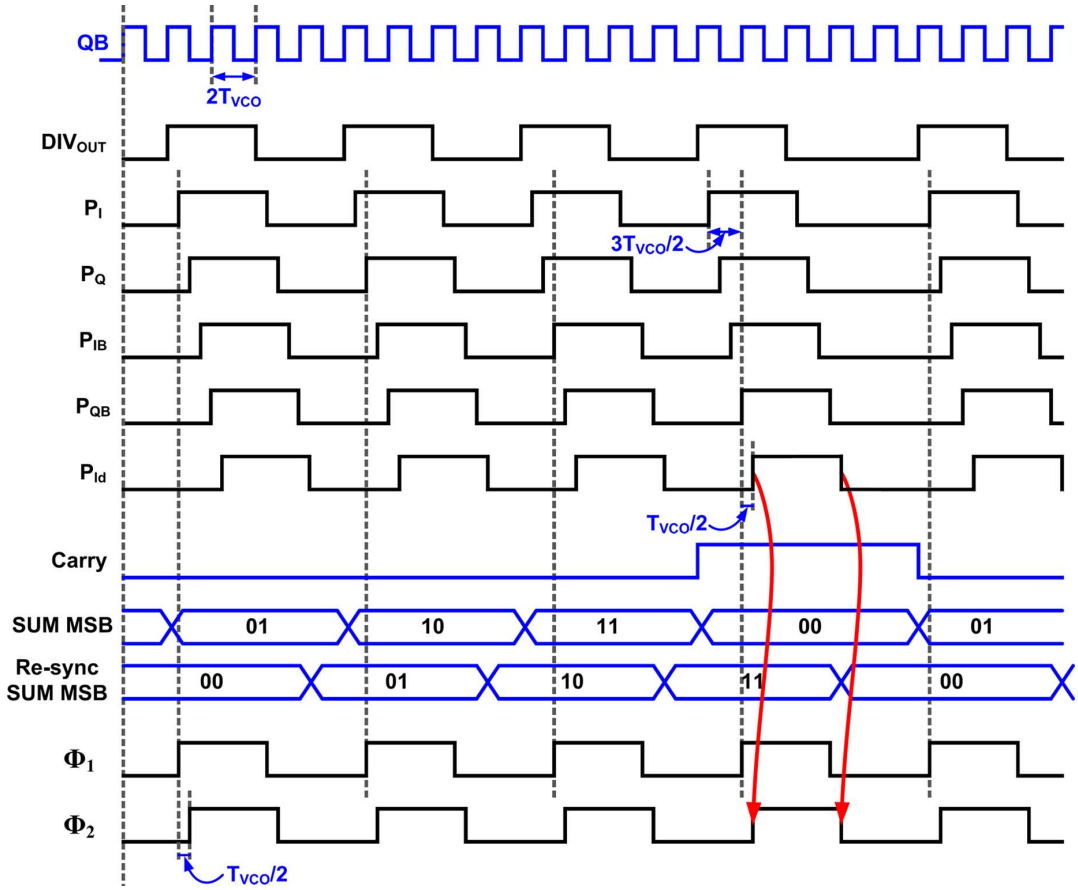

Fig. 8. Timing waveforms of the MSB interpolation using HPC-PI with divide ratio of 4.25.

accumulator. The phase interpolation itself is implemented in 2 stages. In the first stage, a 5-to-2 Phase Mux selects two adjacent phases, Φ_1 and Φ_2, from the five input phases $\mathrm{P_I}$, $\mathrm{P_Q}$, $\mathrm{P_{IB}}$, $\mathrm{P_{QB}}$ and $\mathrm{P_{Id}}$ based on 2 MSBs of the SUM signal. This phase selection operation provides 2 bit coarse error cancellation in phase domain and can generate error free fractional division ratios of 4.25, 4.5, and 4.75 with respect to half the VCO frequency. Fig. 8 shows the detailed timing waveforms of coarse error cancellation for a divide ratio of 4.25. The MSBs of the SUM signal are incremented by one code every reference period so that the Phase Mux adds quarter clock period phase shift to the divider output, resulting in a fractional division ratio of 4.25. Under this condition, phase quantization error is perfectly cancelled by the first stage coarse PI itself. For glitch-free operation the SUM signal is synchronized with the negative edge of phase $\mathrm{P_{Id}}$, so that all the four phases are at the same voltage level (0 V in this case) when the Phase Mux control signal is changed. In addition to Φ_1, its adjacent phase Φ_2, which is half the VCO period $(\mathrm{T_{VCO}}/2)$ delayed from Φ_1 is also selected for fine phase interpolation in the second stage. Note that adjacent phase, Φ_2, is readily available when either $\mathrm{P_I}$, $\mathrm{P_Q}$ or $\mathrm{P_{IB}}$ is selected as Φ_1. However, when phase $\mathrm{P_{QB}}$ is selected $(\Phi_1 = \mathrm{P_{QB}})$, then $\mathrm{P_I}$ cannot be used as adjacent phase output Φ_2. As, instead of being half the VCO period delayed in comparison to $\mathrm{P_{QB}}$, phase $\mathrm{P_I}$ is one and half VCO period $(3\mathrm{T_{VCO}}/2)$ ahead of $\mathrm{P_{QB}}$ (see Fig. 8). So instead of phase $\mathrm{P_I}$, a two VCO cycle delayed version of $\mathrm{P_I}$ denoted as $\mathrm{P_{Id}}$ is used.

Fine phase interpolation in the second stage is directly implemented inside the phase detector/interpolator (XOR PD-PI) block by scaling its output as depicted in Fig. 7. The phase detector consists of two XOR gates that compare Phase Mux outputs Φ_1 and Φ_2 with reference clock, REF. Denoting interpolation weight corresponding to the 4 LSBs of SUM signal as α, fine phase adjustment is achieved by weighting the output currents of two phase detectors by α and $1-\alpha$ and by summing them to generate the output current. Fig. 9 shows the timing waveforms for the 4 bit LSB interpolation. Similar to the 2 MSBs case in the first stage, 4 LSBs of the SUM signal are also synchronized with the negative edge of $\mathrm{P_{Id}}$ phase for glitch-free operation. Because phase interpolation is performed by scaling output currents, much better linearity can be achieved [12], [13], compared to inherently non-linear current or voltage to phase conversion based phase interpolator [14]. Slew rate controllers are also not needed. Another important advantage of this architecture is its suitability at low frequencies because of its insensitivity to Φ_1 and Φ_2 waveform shapes.

Compared to a 3-state phase and frequency detector (PFD), XOR phase detector has higher gain and is also well suited for incorporating charge-pump function needed for phase interpolation. They can also be implemented in a power efficient manner, especially at high reference frequencies. These characteristics allow the PLL to achieve large bandwidth with low power consumption. Furthermore, because XOR PD locks with a phase offset of $\pi/2$, it obviates additional circuitry needed in a PFD to

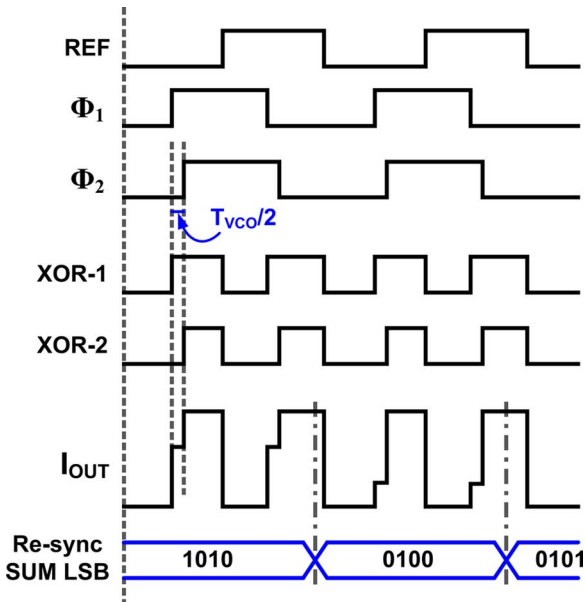

Fig. 9. Timing waveforms of the LSB interpolation using HPC-PI.

generate phase offsets to achieve linear interpolation [2], [15]. A potential drawback of the XOR PD is its sensitivity to input duty cycle. While the input range is prone to duty cycle errors, it has been demonstrated that the interpolation is immune to duty cycle errors [12].

Simulated output phase noise plot of the proposed HPC-PI based PLL is shown in Fig. 10. Thanks to the proposed noise cancellation scheme, quantization error has minimal impact on output phase noise. As a result, PLL bandwidth can be increased to as high as $F_{REF}/20$ to maximize VCO phase noise suppression. However, because of relatively poor phase noise of the ring oscillator, even with a bandwidth of 2.5 MHz ($F_{REF}/20$ at $F_{REF} = 50$ MHz), integrated jitter is dominated by the un-filtered VCO phase noise and is about 2.6 ps_{rms} (see Fig. 10). Hence, further reduction in the jitter requires either lowering the VCO phase noise or further increasing PLL bandwidth. VCO phase noise improvement comes with a large power penalty (reducing phase noise by 3 dB doubles the VCO power consumption). Instead, we explore the possibility of increasing PLL bandwidth. The maximum PLL bandwidth is limited by stability considerations to about $F_{REF}/10$, which results in a trade-off between VCO phase noise suppression and the reference frequency.

To decouple the trade-off between VCO phase noise suppression and the reference frequency, we propose to increase the *effective* reference frequency by 10x by cascading a low-noise integer-N frequency multiplier with the fractional-N PLL (see Fig. 11). This helps in increasing the PLL bandwidth by 10x so that VCO phase noise is suppressed adequately without increasing input crystal oscillator frequency beyond 50 MHz. Simulated phase noise plot of this architecture, shown in Fig. 12, illustrates that integrated jitter can be reduced to 1.4 ps_{rms}. The noise performance of integer-N frequency multiplier is crucial to the low-noise operation of the proposed architecture. It is implemented using a digital multiplying delay-locked loop to achieve low jitter as well as low power. Its implementation details are presented in Section IV.

Note that higher reference frequency also increases oversampling ratio of the $\Delta\Sigma$ modulator used in the fractional divider [16]. As a result, in-band phase quantization error is reduced, which brings the need and effectiveness of the phase noise cancellation into question. So it is instructive to evaluate the phase noise performance improvement solely because of increasing the reference frequency in the absence of cancellation. To this end, we look at the simulated output phase noise plot shown in Fig. 13 when the HPC-PI is turned off and PLL bandwidth

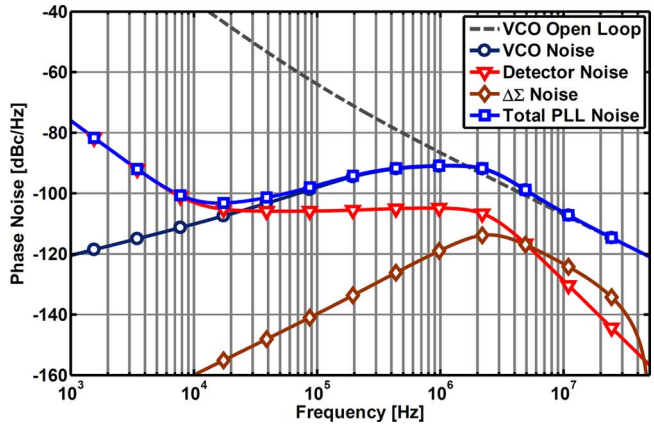

Fig. 10. Simulated phase noise plot for the proposed proposed HPC-PI based PLL.

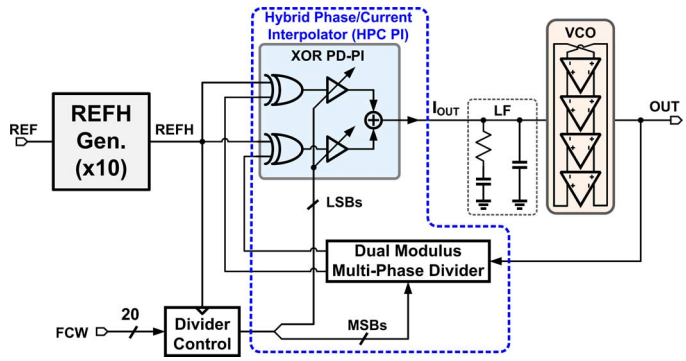

Fig. 11. Simplified block diagram of the proposed two-stage architecture.

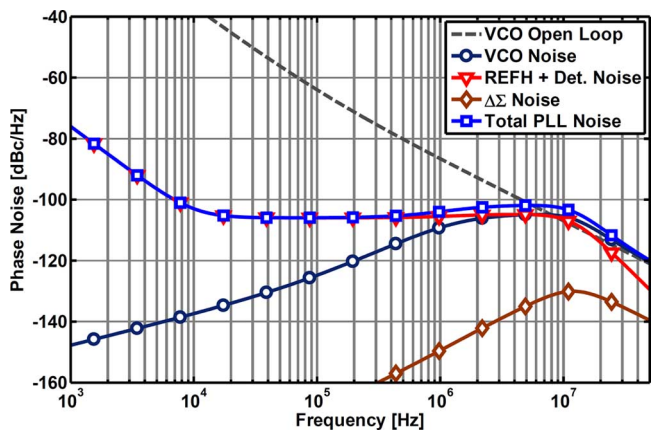

Fig. 12. Simulated phase noise plot of the proposed HPC-PI based PLL architecture with high-frequency reference clock and quantization error cancellation.

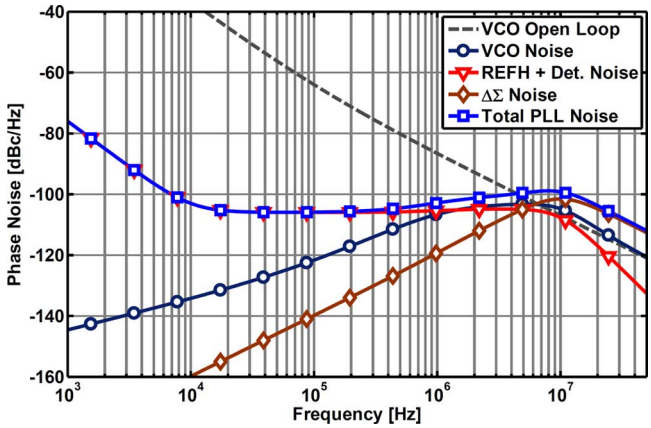

Fig. 13. Simulated phase noise plot of the proposed HPC-PI based PLL architecture with high-frequency reference clock and no error cancellation.

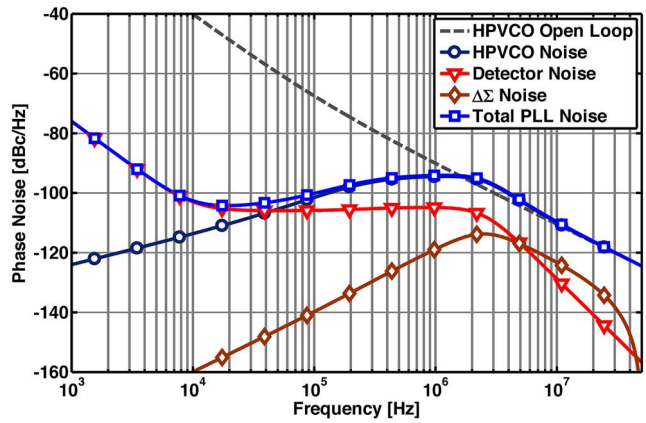

Fig. 14. Simulated phase noise plot of the proposed HPC-PI based PLL architecture with low-noise VCO and quantization error cancellation.

is readjusted for optimum noise performance. As expected, the integrated jitter improves to 2.3 ps_{rms} when the reference frequency is increased to 500 MHz. However, this is approximately 1.7x worse than the case when HPC-PI is used under the same conditions.

The high reference frequency generation also comes with additional power penalty. So the performance of the proposed two-stage architecture should also be compared to the case when the first-stage is eliminated and its power is used to improve phase noise performance of the VCO used in the fractional-N PLL. To this end, the phase noise performance was simulated using a new low-noise VCO (HPVCO) that consumes 2.5x more power. Fig. 14 shows the simulated phase noise performance with HPVCO and 50 MHz reference clock. When HPC-PI is on, integrated jitter is equal to 1.8 ps_{rms}. This indicates that HPC-PI combined with high reference frequency generator yields the lowest jitter in a ring VCO based fractional-N PLL compared to other possible design choices.

IV. Building Blocks

A. Phase Detector/Interpolator

The schematic of the XOR based phase detector/interpolator unit is shown in Fig. 15. It consists of four XOR based phase detectors (XOR 1–4) and a 4 bit current-steering DAC to scale the PD output currents. XOR-1 and XOR-2 are used to detect phase difference between REFH and feedback phases (Φ_1 and Φ_2). XOR gates are implemented using current mode logic with current source loads instead of resistive loads [13]. The use of current source loads not only eases summing of output currents but also allows the integration of charge-pump functionality into the phase detector, obviating the need for a separate charge-pump. Current weighting is performed by varying the tail current sources using a thermometer-coded 4 bit DAC. Two additional phase detectors XOR-3 and XOR-4 are used to steer the tail current when XOR-1 and XOR-2 are off. A unity gain buffer is also added between the two PMOS current sources, M_{P1} and M_{P2} to reduce the V_{DS} mismatch between them. These two techniques greatly improve the interpolation linearity. The output current I_{OUT} is then passed to the loop filter of the PLL. Fig. 16 shows the simulated static non-linearity of the XOR PD-PI, which indicates an INL of 0.6 LSB and a DNL of 0.23 LSB.

B. Ring-VCO

The schematic of the ring oscillator is shown in Fig. 17. It is composed of four pseudo differential delay cells connected in ring topology. The delay cells are implemented using two current starved CMOS inverters coupled in a feed-forward manner using resistors for differential operation. The frequency of the oscillator is controlled by varying the gate voltage of the PMOS current source, M_P. An AC coupled output buffer biased by a replica inverter is used to convert low-swing delay cell output to rail-to-rail output. The simulated spot phase noise of the ring-VCO at 1 MHz frequency offset from the carrier frequency of 4.75 GHz is -87 dBc/Hz.

C. Quadrature Phase Generation

The schematic of the quadrature phase generator is shown in Fig. 18. It is implemented using a cascade of two flip-flops, SA-FF1 and SA-FF2, which provide quadrature phases, I, IB, Q, and QB, at half the input clock frequency. To minimize phase spacing errors caused by asymmetric low-to-high and high-to-low transitions, the flip-flops are implemented using symmetric sense amplifier architecture [17]. The sense-amplifiers are sized to minimize the effect of mismatch at the expense of additional power. Note that multiple phases of the ring VCO can also be used but maintaining their phase relationship while buffering and routing the signals over long distances is difficult and power hungry. In contrast, using only differential output of the VCO as proposed eliminates this issue albeit at the expense of increased phase spacing. Thanks to the hybrid phase current interpolation technique, increased phase spacing does not degrade the linearity of the HPC-PI.

D. Dual Modulus Divider

Fig. 19 shows the schematic of divide-by-4/5 dual modulus divider. It consists of a cascade of two divide-by-2/3 stages that are implemented using digital logic standard cells. Each of the divide-by-2/3 stages consists of two active high and two active low level transparent latches (L1–L4) along with a few

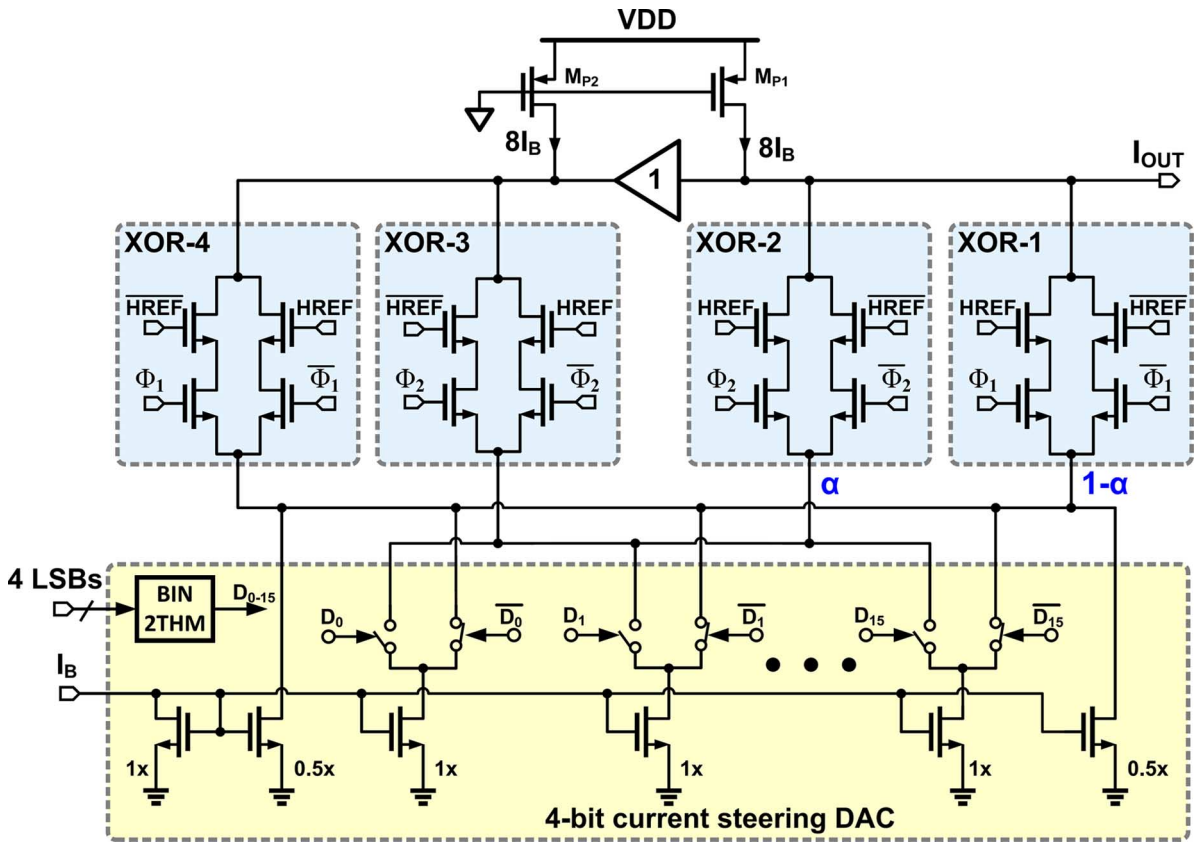

Fig. 15. Schematic of the phase detector/interpolator.

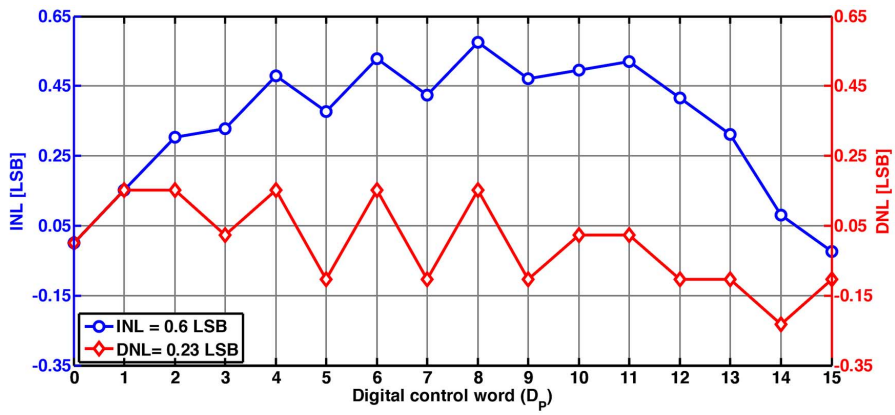

Fig. 16. Simulated non-linearity of the phase detector/interpolator.

logic gates. By selecting the control node P the divide-by-2/3 operation is performed. To achieve divide-by-4/5 operation only one divide-by-2/3 stage is controlled using $\mathrm{DIV}_{\mathrm{CTRL}}$ node with the CARRY output of digital phase accumulator while the control of the second divide-by-2/3 stage is kept at logic low. The clock input to the dual modulus divider is provided through phase QB of the quadrature phase generator and output of divider is synchronized with all four quadrature phases using flip-flops. The range of this divider can be extended to achieve higher divide ratios either by using control node P of the second divide-by-2/3 stage or by cascading more of these stages. However, dual modulus divider with a division ratio between 4.25 to 4.75 is sufficient to provide an output frequency range of 500 MHz between 4.25 GHz to 4.75 GHz because of the high reference frequency of 500 MHz and the presence of static divide-by-2 stage (used for quadrature phase generation) before the dual modulus divider.

E. High-Frequency Reference Generation

A digital multiplying delay-locked loop (MDLL) is used to generate 500 MHz reference clock for the fractional-N PLL from a 50 MHz crystal oscillator. Compared to a PLL, an MDLL offers superior phase noise due to the periodic reference injection and consumes low power due to relaxed phase noise requirements of the oscillator [18]–[20]. The block diagram of the digital MDLL is shown in Fig. 20. A D flip-flop (FF) detects

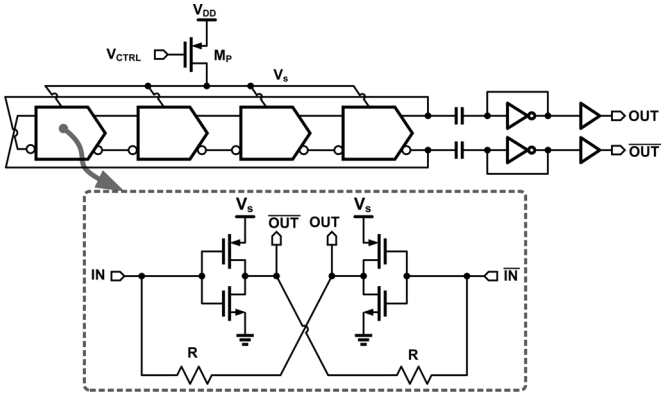

Fig. 17. Schematic of the ring VCO.

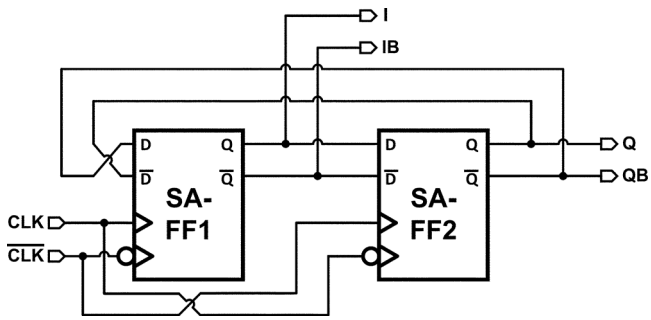

Fig. 18. Schematic of divide-by-2 quadrature phase generator.

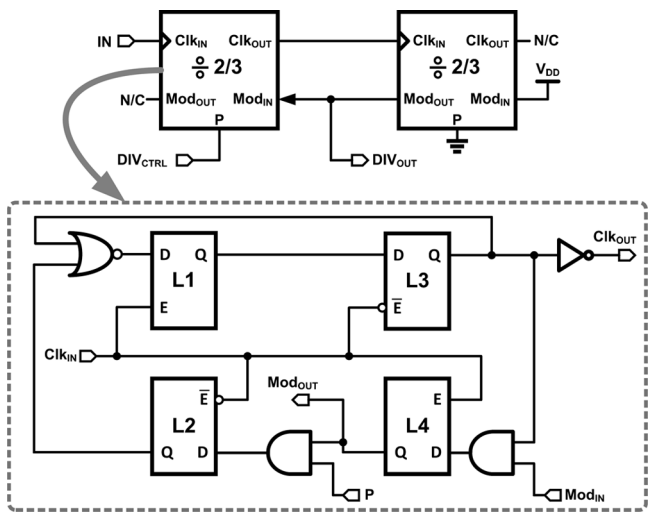

Fig. 19. Schematic of divide-by-4/5 dual modulus divider.

sign of the phase error between the reference clock and oscillator output and its output is integrated by a 16 bit accumulator. The 2 LSBs are dropped to reduce gain of the integral path and rest of the 14 bits are fed to a second order digital $\Delta\Sigma$ modulator. The modulator, clocked at 125 MHz, truncates 14 bits to 5 bits and drives binary-to-thermometer (BIN2THM) converter. The output of BIN2THM controls a 31-level thermometer coded IDAC implemented using identical stages of NMOS unit current sources. The output current of the IDAC, is then converted to voltage using a resistor. A 4th-order passive low pass filter (LPF) is used at the IDAC output to suppress out-of-band quantization noise and generate control voltage of the multiplexed

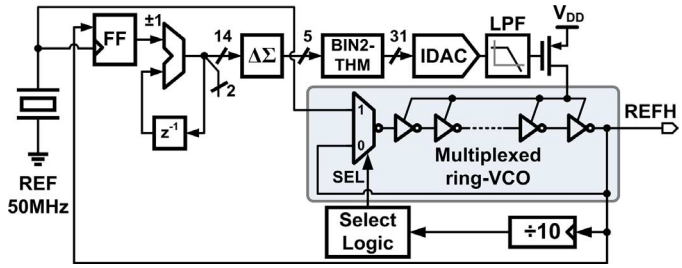

Fig. 20. Block diagram of high-frequency reference generator digital MDLL.

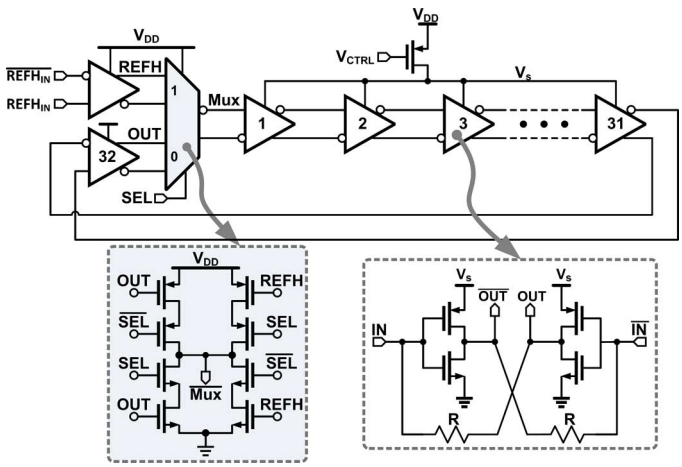

Fig. 21. Schematic of multiplexed ring-VCO used in digital MDLL.

ring-VCO. A divider along with the select logic is used for periodic injection of the reference clock into multiplexed ring-VCO. Select logic similar to the one reported in [21] is employed and is implemented using standard cells. It generates the select signal, SEL, using the divider output and an intermediate delay stage output of the oscillator.

Fig. 21 shows the schematic of the multiplexed ring-VCO used in digital MDLL. The multiplexed ring-VCO is implemented using 32 pseudo differential delay stages and a multiplexer. Since the oscillation frequency of the ring is relatively low, a large number of inverter stages are used to achieve sharp rise and fall times. Fast edge transitions help minimize pattern jitter during reference injection. The delay cells are implemented by coupling two current starved CMOS inverters in a feed-forward manner using resistors. A NAND-gate based multiplexer is used for selecting between the buffered reference clock and the oscillator output, REFH. The frequency of the multiplexed ring VCO is controlled by varying the gate voltage, V_{CTRL}, of the PMOS current source. To minimize the impact of reference injection on the VCO virtual supply voltage, V_S, multiplexer and the delay stage driving the multiplexer are connected to the supply voltage, V_{DD}, instead of V_S.

V. Experimental Results

The block diagram of the complete two-stage fractional-N PLL is shown in Fig. 22. A prototype chip fabricated in a 65 nm CMOS process and occupies an active area of 0.48 mm^2. The die micrograph is shown in Fig. 23. The die is packaged in a standard 60 pin QFN plastic package and characterized using a four-layer printed circuit board. Operating from 1.0 V

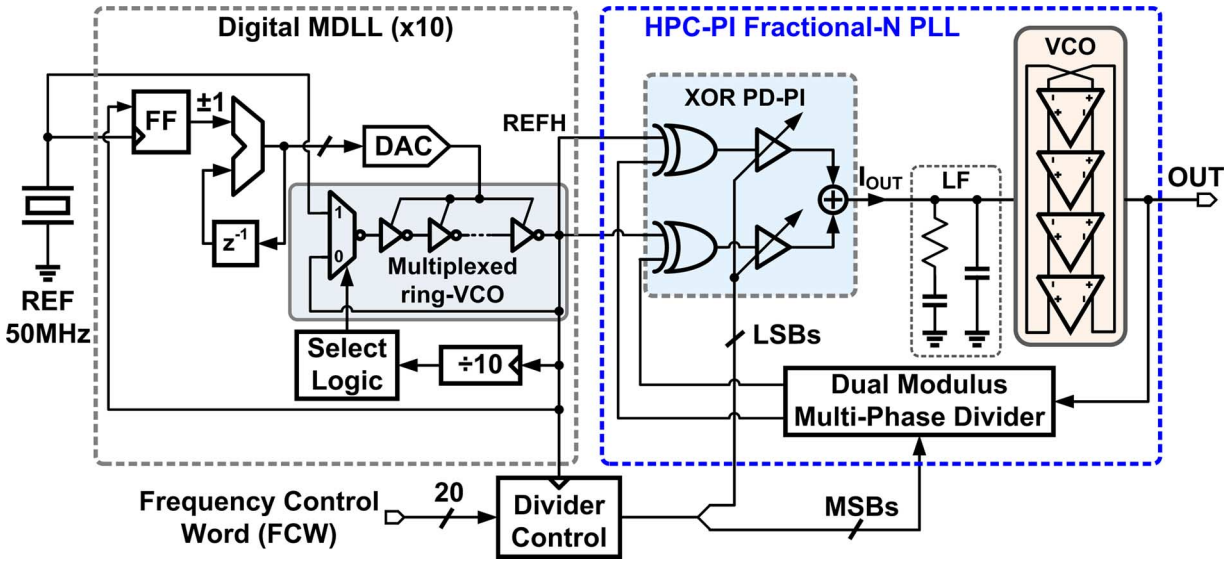

Fig. 22. Complete block diagram of the proposed architecture.

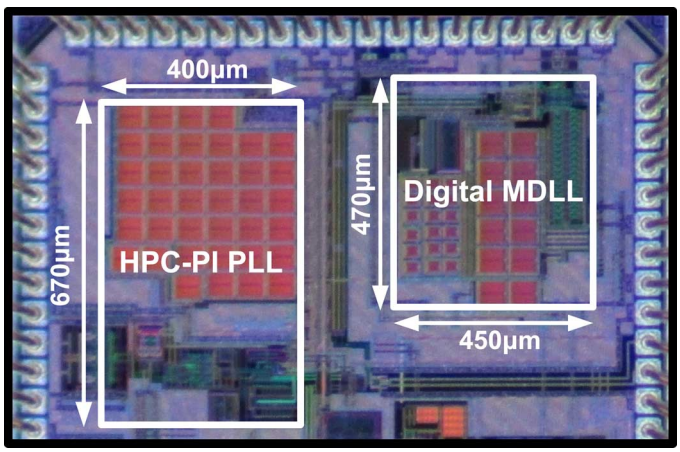

Fig. 23. Die micrograph of the proposed clock generator.

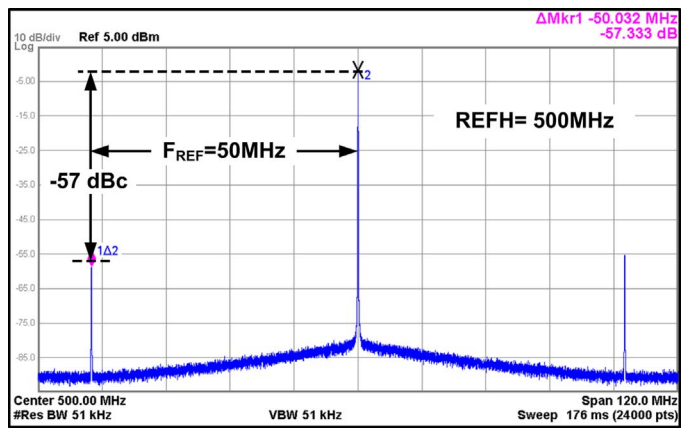

Fig. 24. Measured output spectrum of the high-frequency reference generator MDLL.

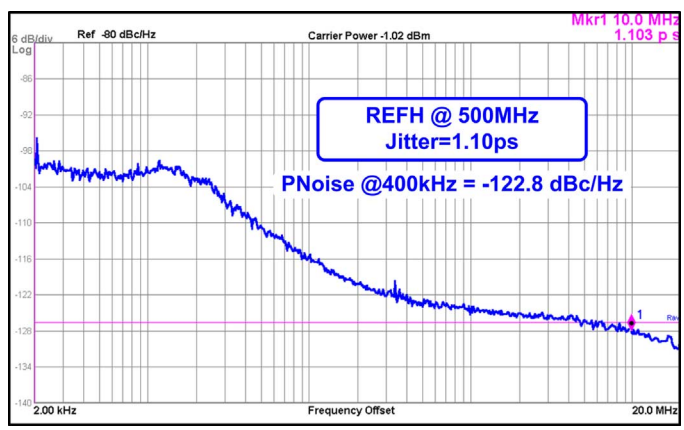

Fig. 25. Measured output phase noise plot of the MDLL used for high-frequency reference generation.

supply the proposed clock multiplier can generate fractional frequencies over a range of 4.25 to 4.75 GHz while consuming 11.6 mW power.

The spectrum of the MDLL output measured using Agilent MXA N9020A spectrum analyzer is shown in Fig. 24. Operating with a 50 MHz reference clock provided by a crystal oscillator, the MDLL generates a 500 MHz output and the measured reference spur magnitude is -57 dBc. The measured phase noise plot of the MDLL output is depicted in Fig. 25. The in-band phase noise at 400 kHz offset frequency is -122.8 dBc/Hz and the jitter obtained by integrating phase noise from 2 kHz to 20 MHz is 1.1 ps_{rms}.

Measured output phase noise plots of the complete fractional-N PLL in integer- and fractional-N modes are shown in Fig. 26. When operated in the integer-N mode at 4 GHz output frequency, in-band phase noise is -104.7 dBc/Hz at 400 kHz offset frequency and the integrated (2 kHz to 20 MHz) jitter is 1.42 ps_{rms}. When the mode of operation is changed from integer-N to fractional-N, in-band phase noise floor rises only by 0.9 dB to -103.8 dBc/Hz at 400 kHz offset indicating that the quantization noise has minimal impact on the overall noise

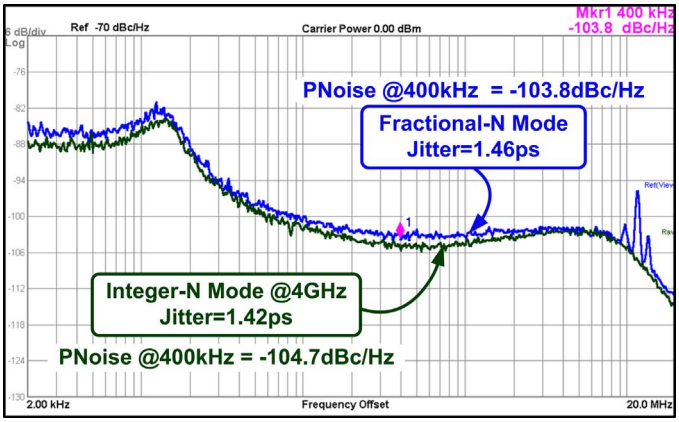

Fig. 26. Measured output phase noise plot of the proposed architecture in integer and fractional-N mode.

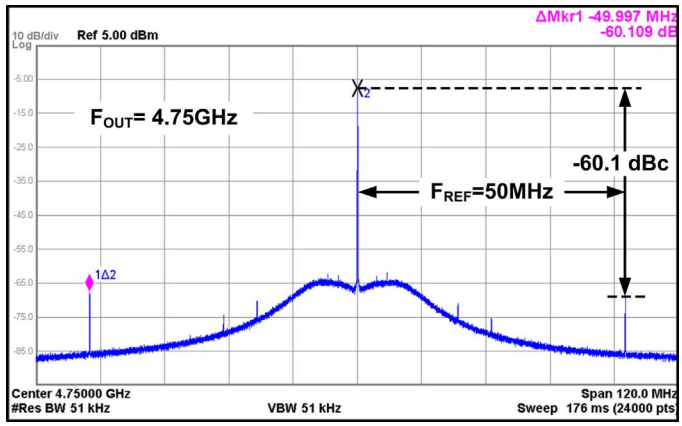

Fig. 28. Measured output voltage spectrum of the proposed architecture at 4.75 GHz.

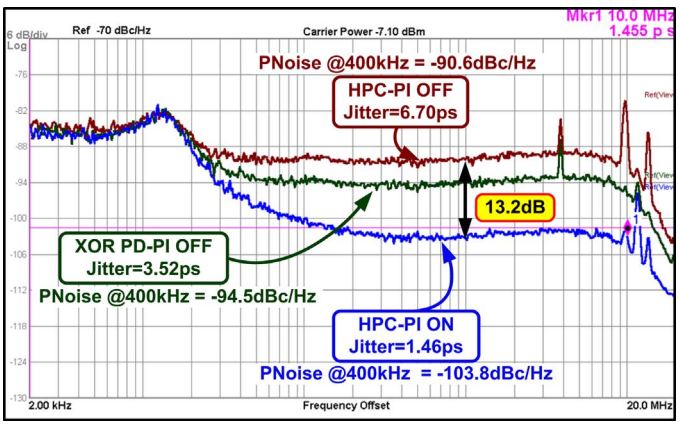

Fig. 27. Measured output phase noise plot of the proposed architecture with HPC-PI ON and OFF.

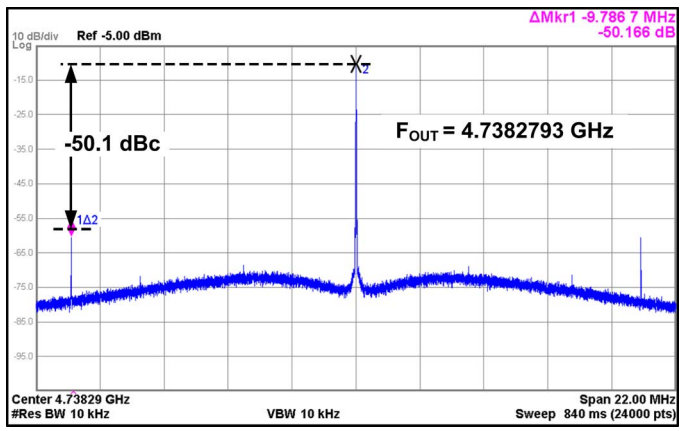

Fig. 29. Measured fractional spur of the proposed architecture.

performance. The integrated jitter also remains almost the same at 1.46 ps_{rms}.

The measured output phase noise plots shown in Fig. 27 quantify the effectiveness of different steps in the HPC-PI cancellation method. Shown in the figure are output phase noise plots in different HPC-PI states when generating fractional output frequency with a frequency control word corresponding to $4.75 - (2^{-7} + 2^{-8} + 2^{-19})$ GHz. When the HPC-PI is OFF, integrated jitter is 6.7 ps_{rms} (2 kHz to 20 MHz) and the in-band phase noise floor is -90.6 dBc/Hz at 400 kHz offset. When only 2 MSBs of the PI are turned ON (i.e only Phase Mux portion of the PI is exercised), the integrated jitter and the noise floor reduce to 3.52 ps_{rms} and -94.5 dBc/Hz, respectively. When the HPC-PI functionality is turned ON completely, integrated jitter is 1.46 ps_{rms} and noise floor reduces to -103.8 dBc/Hz, corresponding to an improvement of 13.2 dB compared to the case when the HPC-PI is disabled.

The output spectrum of the complete fractional-N PLL is shown in Fig. 28. The reference spur at 50 MHz is about -60 dBc and its magnitude depends on two factors: (a) the reference spur magnitude at the output of the MDLL and (b) the bandwidth of second stage fractional-N PLL. The leakage of the MDLL reference spur (-57 dBc in our implementation) to the output can be reduced by lowering the fractional-N PLL bandwidth. However, this exacerbates the impact of VCO phase noise on output jitter. As a compromise between the suppression of MDLL reference spur and VCO phase, the PLL bandwidth is chosen to be 12 MHz, which is about 2 times smaller than the possible maximum (recall $\text{F}_{\text{REF}}/20 = 25$ MHz for the fractional-N PLL).

With the use of a high reference frequency, REFH, of 500 MHz, along with divide-by-2 based quadrature phase generator, the fractional frequency control word ranging from only 0.25–0.75 can provide an output frequency range of 4.25 to 4.75 GHz. As a result, the frequency control word does not need to be close to the integer boundary, which greatly improves the worst case in-band spur performance. Fig. 29 shows the measured fractional spur performance at the output. With 12 MHz PLL bandwidth, the in-band fractional spur magnitude is -51 dBc.

Power breakdown of the fractional-N PLL is shown in Fig. 30. Operating from a 1.0 V supply, the proposed clock multiplier consumes the total power of 11.6 mW, of which the MDLL consumes 3.2 mW. Performance summary and comparison of key parameters with the state-of-the-art ring-based fractional-N PLLs is depicted in Table I. For fair comparison, phase noise is normalized to 4.75 GHz. The proposed clock multiplier achieves the lowest jitter and 2x power efficiency improvement compared to state-of-the-art fractional-N ring-based

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED CLOCK MULTIPLIER WITH STATE-OF-THE-ART DESIGNS.

	This Work	Kao [8] ISSCC'13	Park [22] JSSC'12	Jee [23] JSSC'12	Chen [24] JSSC'10	Yu [25] JSSC '09
Technology	65nm	90nm	130nm	130nm	65nm	0.18μm
VCO Topology	Ring	Ring	Ring	Ring	Ring	Ring
Supply Voltage [V]	1.0	2.5/1.2	N/A	N/A	1.1-1.3	1.8
Area [mm^2]	0.48	0.055	0.17	0.35	0.027	N/A
Output Frequency [GHz]	4.25-4.75	1.872-1.896	2.4	1	0.6-0.8	0.17-1.25
Reference Frequency [MHz]	50	26	32	32	26 (2-40)	24
Integrated Jitter [ps$_{\mathrm{rms}}$]	1.5	3.4	N/A	N/A	21.5	17.3
Reference Spur [dBc]	-60	-67	-60	-67	-52	N/A
In-band Phase Noise [dBc/Hz]	-103.8 @400kHz	-100 @400kHz	-97 @100kHz	-106 @100kHz	-93 @1kHz	N/A
Normalized Phase Noise @4.75GHz [dBc/Hz]	-103.8 @400kHz	-100 @400kHz	-97 @100kHz	-106 @100kHz	-93 @1kHz	N/A
Power Consumption [mW]	11.6	10	15.2	16.8	2.9-3.5	6.1
Power Efficiency [mW/GHz]	2.4	5.24	6.33	16.8	26.8	13.8
FoM* [dB]	-225.8	-219.4	-216	N/A	-207.9	-207.3

$$*\mathrm{FoM} = 10\log\left[\left(\frac{\sigma_{\mathrm{t}}}{1\mathrm{sec}}\right)^2 \frac{\mathrm{P_{PLL}}}{1\mathrm{mW}}\right]$$

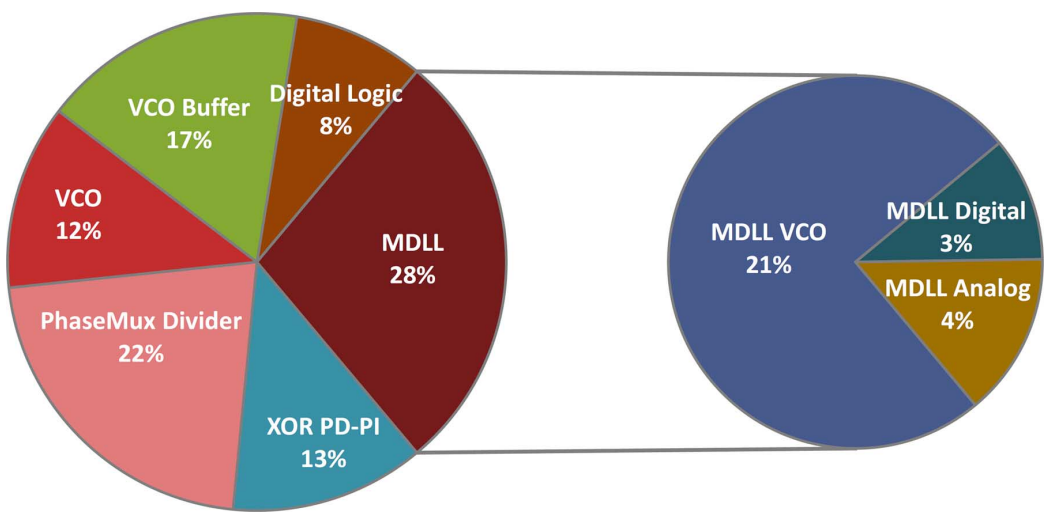

Fig. 30. Power breakdown of the proposed architecture.

PLL designs. It also achieves the best figure of merit (FoM) of -225.8 dB, defined as a metric for jitter/power efficiency, among all ring oscillator-based fractional-N PLLs.

VI. CONCLUSIONS

A hybrid phase/current phase interpolation technique is presented to improve phase noise performance of ring oscillator based fractional-N PLLs. The proposed HPC-PI alleviates the bandwidth trade-off between VCO phase noise suppression and $\Delta\Sigma$ quantization noise suppression. By combining phase detection and interpolation functions in to XOR PD-PI, the accurate quantization error cancellation is achieved without using calibration. Use of a digital MDLL in front of the fractional-N PLL helps in alleviating the bandwidth limitation due to low refer-

ence frequency, extending the PLL bandwidth further to suppress VCO phase noise and lowers the in-band noise floor. Fabricated in 65 nm CMOS process, the prototype generates fractional output frequencies from 4.25 to 4.75 GHz with in-band noise floor of −104 dBc/Hz and 1.5 ps_{rms} integrated jitter. The measured results show that the overall clock generator provides a 13.2 dB noise floor improvement. The proposed clock multiplier achieves power efficiency of 2.4 mW/GHz and the best figure of merit of −225.8 dB for ring-VCO based fractional-N PLLs reported in literature.

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