A 4.25GHz-4.75GHz Calibration-free Fractional-N Ring PLL Using Hybrid Phase/Current-mode Phase Interpolator With 13.2dB Phase noise Improvement

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Abstract

A calibration-free ring oscillator based fractional-N clock multiplier using hybrid phase/current-mode phase interpolator is presented. Fabricated in 65nm CMOS process, the prototype generates fractional frequencies from 4.25GHz-to-4.75GHz with in-band noise floor of -104dBc/Hz and 1.5ps integrated jitter. The clock multiplier achieves power efficiency of 2.4mW/GHz and FoM of -225.8dB.

Introduction

Fractional-N PLLs use phase noise cancellation/suppression techniques to alleviate tradeoffs between ΔΣ quantization error (E_Q) and VCO phase noise [1-3]. Cancelling E_Q using a DAC at the charge-pump output [1] is susceptible to inherent gain mismatch between E_Q path and cancellation-DAC path. For reasonable cancellation accuracy, high precision analog circuitry and extensive calibration are needed [1]. On the other hand, suppression techniques using phase interpolators (PI) that seek to cancel E_Q at the divider output are immune to path mismatches, but are limited by PI non-linearity [2-3]. To overcome PI non-linearity, elaborate calibration [2] or noise-shaped segmentation techniques [3] are needed, both of which add to the design complexity. Even if PLL bandwidth is extended to ≈ F_{REF}/15 (2MHz in [3]) using these techniques [2, 3], it is still inadequate to suppress ring-VCO phase noise in deep sub-micron technologies. In this paper, we present a calibration-free ring-based fractional-N PLL using hybrid phase/current-mode phase interpolator (HPC-PI). The fractional-N PLL bandwidth is decoupled from low crystal oscillator frequency reference, by cascading a low noise integer-N frequency multiplier with the fractional-N PLL. As a result, the VCO phase noise suppression bandwidth is extended to about 10MHz even when F_{REF} is as low as 50MHz. This together with the HPC-PI-based fractional divider improves output phase noise by 13.2dB and helps to achieve better than 1.5ps_{rms} integrated jitter.

Overall Architecture

Figure 1 shows the block diagram of the proposed fractional-N ring-based clock multiplier. It consists of a cascade of digital multiplying delay-locked loop (MDLL) and HPC-PI-based fractional-N PLL. MDLL, opposed to a PLL, is used because its oscillator phase noise suppression bandwidth (F_{REF}/4) is shown to be at least 2.5 times that of a PLL (F_{REF}/10) [4]. The MDLL consisting of mostly digital circuits – a flip-flop based BBPD, a digital accumulator, a CMOS inverter-based ring oscillator – generates a low noise 500MHz clock, REFH, from 50MHz crystal oscillator. By replacing the noisy VCO edge with a clean reference clock edge, the MDLL achieves in-band phase noise performance of -122.8dBc/Hz at 400kHz offset.

The second stage fractional-N PLL employs a PI-based fractional divider, pair of current-mode XOR phase detectors

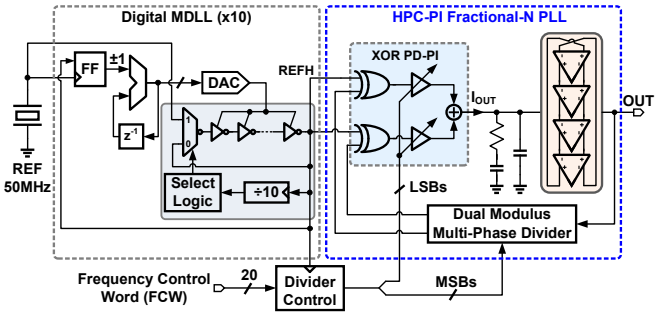

Fig. 1: Simplified block diagram of the proposed fractional-N PLL.

(XOR-PDs), loop filter and ring VCO. The currents produced by two XOR-PDs are digitally weighted, summed, and filtered to generate VCO control voltage. The PI-based fractional divider is implemented using a dual-modulus-divider (DMD) and the hybrid phase/current-mode PI (HPC-PI). By using this approach, instantaneous ΔΣ phase quantization error is reduced by 32X, from single VCO period T_{VCO} to $T_{VCO}/2^5$ and improves phase noise performance. Conventional PIs rely on the inherently non-linear voltage-to-phase conversion mechanism and require closely spaced phases with sinusoidal-shape waveform to achieve good linearity. The proposed HPC-PI on the other hand achieves superior digital-to-phase conversion linearity by indirectly introducing phase shift between two phases as a charge imbalance on the PLL loop filter and by relying on high loop gain of the PLL to suppress nonlinearity [5]. Consequently, HPC-PI obviates the need for large number of phases or slew-rate control circuits required in conventional PIs to achieve fine resolution.

Figure 2 shows the detailed schematic of proposed HPC-PI based fractional divider. The 20-bit frequency control word, FCW, is truncated to 6-bits using a second-order ΔΣ modulator to reduce word length of the digital phase accumulator (DPA). Carry and sum outputs of the DPA control 4/5 DMD and the 6-bit HPC-PI, respectively. The two MSBs of the sum output are used for quadrant selection in phase domain by selecting two adjacent phases, Φ_1 and Φ_2, out of four quadrature phases, I/IB/Q/QB, that are generated using a quadrature divider. These phases are compared with the phase of the MDLL output, REFH using two XOR phase detectors. The remaining LSBs of the PI are implemented in current domain by combining digitally controlled output currents of the two PDs [5]. The output current weights, α and 1- α, of the XOR PDs are chosen such that the combined output current I_{OUT} is equivalent to the current that would have been obtained by comparing the output of a 6-bit resolution ideal PI with REFH using one phase detector. This approach lowers the quantization error, E_Q, injected into the loop filter by 32 times. The detailed schematic of the combined XOR-based PD and PI is depicted in Fig. 3. It consists of four XOR gates, two PMOS current sources, and a 4-bit current steering DAC. Tail current

of XOR PDs is controlled by a 4-bit DAC based on its input control code. The two XOR-gates, XOR-1 and XOR-2, compare the MDLL output phase with Φ_1 and Φ_2, and generate an output current proportional to the phase error. The two complimentary phase detectors XOR-3 and XOR-4 are used to steer the current when XOR-1 and XOR-2 are OFF. PI non-linearity caused by V_{DS} mismatch between the two PMOS current sources is suppressed by using a unity gain buffer (see Fig.3).

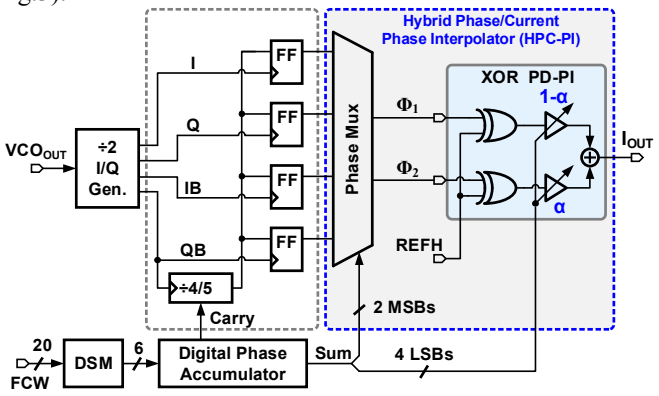

Fig. 2: Block diagram of the dual modulus divider with HPC-PI.

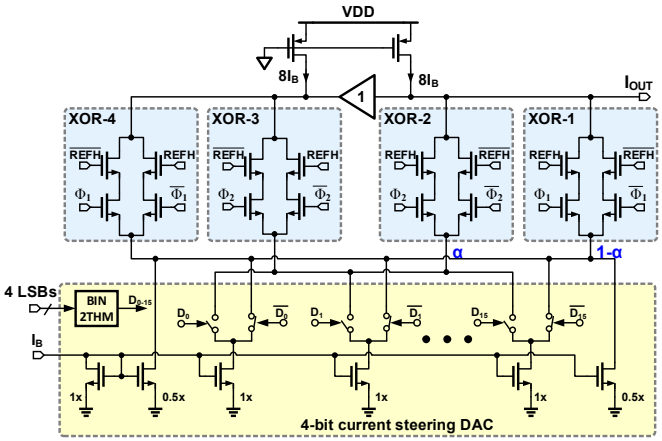

Fig. 3: Schematic diagram of XOR phase detector/interpolator.

Measurement Results

The prototype clock multiplier is fabricated in a 65nm CMOS logic process and occupies an active area of 0.55mm^2. Operating from 1V supply, it consumes a total power of 11.6mW out of which 3.2mW is consumed by the digital MDLL. Figure 4 shows the measured typical output phase noise plot without and with HPC-PI. When the HPC-PI is OFF, integrated jitter is 6.7ps$_{rms}$ (2kHz to 20MHz) and the in-band phase noise floor is -90.6dBc/Hz. When only the 2MSBs of the PI are turned ON, the integrated jitter and the noise floor reduce to 3.52ps$_{rms}$ and -94.5dBc/Hz, respectively. When the complete proposed HPC-PI is turned ON, integrated jitter is 1.46ps$_{rms}$ and noise floor reduces to -103.8dBc/Hz, which illustrates an improvement of 13.2dB compared to the conventional case when the PI disabled.

Figure 5 shows the MDLL output phase noise plot along with those of the complete clock multiplier in integer-N and fractional-N modes. The integrated jitter remains same in both modes and is equal to about 1.4ps$_{rms}$. Figure 6 shows the performance summary table and comparison with the state-of-the-art designs along with die micrograph. The proposed clock multiplier achieves the lowest jitter and 2X power efficiency improvement compared to state-of-the-art fractional-N ring-based PLL designs. It also achieves the best figure of merit (FoM) of –225.8dB, defined as jitter/power efficiency, among all ring oscillator-based fractional-N PLLs.

Acknowledgments

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References

[1] S. Pamarti, *et al.*, *JSSC*, vol. 39, pp. 49–62, Jan. 2004.
[2] M. Zanuso, *et al.*, *ISSCC Digest,* pp. 476–477, Feb. 2010.
[3] T. Kao, *et al.*, *ISSCC Digest,* pp. 416–417, Feb. 2013.
[4] R. Farjad-rad, *et al.*, *ISSCC Digest*, pp. 76–77, Feb. 2002.
[5] T. Toifl, *et al., ISSCC Digest,* pp. 410–411, Feb. 2005.

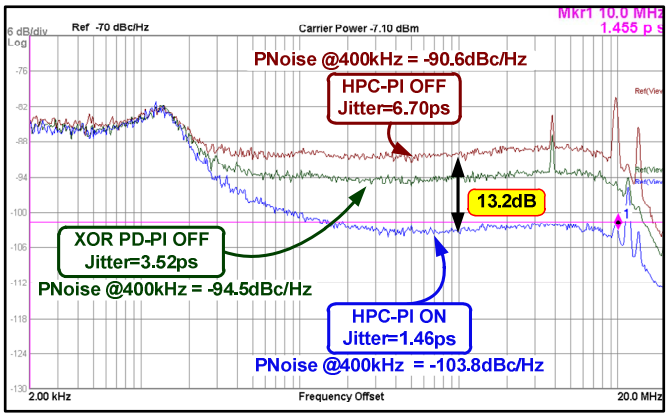


Fig. 4: Measured output phase noise plots at F_{OUT} 4.73828125GHz.

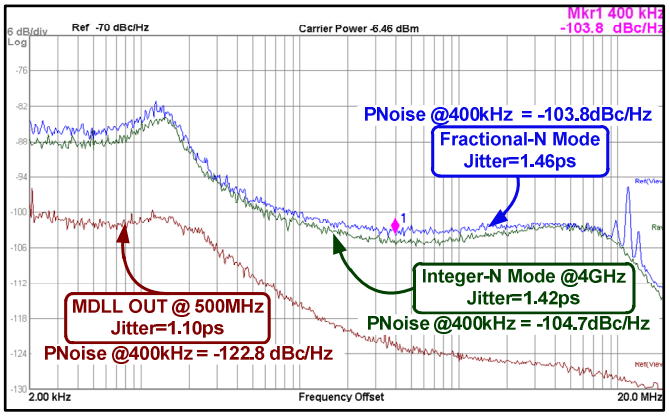
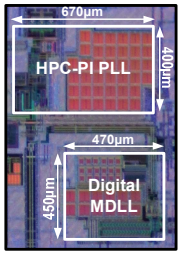


Fig. 5: Measured output phase noise plot of MDLL and the entire PLL in fractional- and integer-N modes.

	This Work	ISSCC'13 Kao et al.	JSSC'12 Park et al.	ISSCC'11 Jee et al.	ISSCC'10 Chen et al.	JSSC'09 Yu et al.
Technology	65nm	90nm	130nm	130nm	65nm	180nm
VCO topology	Ring	Ring	Ring	Ring	Ring	Ring
Supply voltage [V]	1	2.5/1.2	N/A	N/A	1.1-1.3	1.8
Area [mm^2]	0.54	0.055	0.17	0.35	0.027	N/A
Output freq. [GHz]	4.25-4.75	1.872-1.896	2.4	1	0.6-0.8	0.17-1.25
Ref. freq. [MHz]	50	26	32	32	26(2-40)	27
Integrated jitter[ps]	1.5	3.4	N/A	N/A	21.5	17.3
Ref. spur. [dBc]	-60	-67	-60	-67	N/A	N/A
In-band Pnoise [dBc/Hz]	-103.8@ 400kHz	-100@ 400kHz	-97@ 100kHz	-106@ 100kHz	-93@ 1kHz	N/A
Normalized Pnoise @4.75GHz [dBc/Hz]	-103.8@ 400kHz	-92.1@ 400kHz	-91@ 100kHz	-92.4@ 100kHz	-77.5@ 1kHz	N/A
Power [mW]	11.6	10	15.2	16.8	2.9-3.5	6.1
Power efficiency [mW/GHz]	2.4	5.24	6.33	16.8	26.8	13.8
FoM* [dB]	-225.8	-219.4	-216	N/A	-207.9	-207.3



*FoM=10 log[(σt/1s)^2 PPLL/1mW]

Fig. 6: Performance summary and die micrograph.