Continuous-rate clock-and-data recovery (CDR) circuits with automatic frequency acquisition offer flexibility in both optical and electrical communication networks, and minimize cost with a single-chip multi-standard solution. The two major challenges in the design of such a CDR are: (a) extracting the bit-rate from the incoming random data stream, and (b) designing a wide-tuning-range low-noise oscillator. Among all available frequency detectors (FDs), the stochastic divider-based approach has the widest frequency acquisition range and is well suited for sub-rate CDRs [1]. However, its accuracy strongly depends on input transition density (0 ≤ ρ ≤ 1), with any deviation of ρ from 0.5 (50% transition density) causing 2x(ρ-0.5)/10 ppm of frequency error. In this paper, we present an automatic frequency-acquisition scheme that has unlimited range and is immune to variations in transition density. Implemented using a conventional bang-bang phase detector (BBPD), it requires minimum additional hardware and is applicable to sub-rate CDRs as well. Instead of using multiple LC oscillators that are carefully designed to cover a wide frequency range [2,3], a ring-oscillator-based fractional-N PLL is used as a digitally controlled oscillator (DCO) to achieve both wide range and low noise, and to decouple the tradeoff between jitter transfer (JTRAN) bandwidth and ring-oscillator-noise suppression.

Figure 8.7.1 depicts the developed digital CDR architecture. It is composed of a frequency-locked loop (FLL), and a delay- and phase-locked loop (D/PLL). Both the FLL and D/PLL are used in the following early/late (E/L) signals and are dedicated to the PLL to control the input frequency range. The path containing divide-and accumulator ACCO contains an additional clock to bias the mid-delay point in steady state by the path containing gain block KO and accumulator ACCO. The path containing divide-by-H and accumulator ACCH is used to prevent false locking as discussed later. The accuracy of the frequency detection scheme depends on ρ and data/clock jitter (ϕ), as quantified by the tabulated frequency error in Fig. 8.7.2. However, setting Nth corresponding to ρ = 1 (i.e., Nth = FDIN/2FP) ensures that residual frequency error will always be smaller than ΔF, for any ρ. For example, Nth = 500 ensures that the DCO is always locked within 1000ppm to target data rate. Interestingly, ΔF improves accuracy as it is equivalent to setting a larger Nth, with ϕ = 0. Very large ΔF can cause false updates of the DCO frequency, which can be prevented by not incrementing ACC when the peak value of ΔΦCD is smaller than its previous peak. Potential false locking caused by some degenerate input patterns manifests as reduced ΔΦCD count. Therefore, separately counting the number of transitions using divisor H and ACCH, and comparing to ΔΦCD, can detect false locking. Under this condition, incrementing the DCO frequency will pull the CDR away from false locking.

The DCO is implemented using a fractional-N PLL as shown in Fig. 8.7.3. Frequency control word (FCW), provided by the CDR logic, tunes the fractional-N PLL output frequency by varying its feedback divider from 4 to 15. When operated with a 500MHz reference clock, this translates to a wide DCO tuning range of 5.5GHz (2 to 7.5GHz). Since more than 2x frequency range is achieved, lower data rates can be easily accommodated using a divider chain [2]. Further, using a high reference clock extends the PLL bandwidth sufficiently to adequately suppress ring-oscillator phase noise while maintaining the same quantization error of the fractional divider [4], and provides the freedom to use small JTRAN to filter input noise without degrading performance due to DCO phase noise. An on-chip digital multiplying DLL (MDDL) generates the 500MHz reference clock in a 50MHz crystal. It is important to note the crystal oscillator does not aid frequency acquisition, as its frequency has no relation to the input data rate. Fractional-N PLL helps suppress oscillator phase noise and can be eliminated if the ring oscillator meets JGEN specification (FCW drives ring oscillator directly in that case). Compared to using multiple LC oscillators [2,3], this approach covers a wide range with only one ring oscillator and has a linear relationship between FCW and data rate. A second-order ΔΣ modulator is used to truncate FCW and drive the feedback divider. A 2nd-order loop filter along with the 3rd pole located at the drain of current-source transistor, Mth, is used to suppress ΔΣ truncation error.

The prototype CDR is implemented in a 65nm CMOS process, occupies an active area of 1.63mm², and is packaged in an 8088 package. At 10g/s, the CDR consumes 22.5mW and achieves a BER < 10^-12. Measured residual frequency error versus locking threshold Nth (Fig. 8.7.4) shows that the PLL is immune to transition density. With Nth > 600, the frequency error is always less than 500ppm. Jitter transfer curves measured with different input jitter amplitudes illustrate that JTRAN bandwidth is independent of jitter amplitude even when using a BBPD (Fig. 8.7.5). The measured JTOL plot in Fig. 8.7.5 indicates a corner frequency of about 9MHz, which is much larger than JTRAN bandwidth of 0.13μm, which is limited by DCO range, and low-frequency JTOL is restricted to 2MHz with a 10MHz. The JTOL frequency is determined by limiting the JTOL parameter, and with 10MHz, JTOL is restricted to 2MHz due to limit instrument. Figure 8.7.6 tabulates the performance summary and the comparison. Compared to the results cited in the table, this work achieves the highest power efficiency, and lowest jitter while using ring-based oscillators. The die micrograph is shown in Fig. 8.7.7.

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References:
Figure 8.7.1: Block diagram of the continuous-rate digital CDR architecture.

Figure 8.7.2: Principle of the automatic frequency acquisition using BBPD outputs and the sensitivity to transition density and jitter.

Figure 8.7.3: Schematic of fractional-N PLL-based wide-range DCO.

Figure 8.7.4: Measured residual frequency error versus locking threshold N_th at different transition densities.

Figure 8.7.5: Measured jitter transfer with different input jitter amplitudes, and jitter tolerance with PRBS7 data (BER threshold of 10^-4).

Figure 8.7.6: CDR performance summary and comparison.
Figure 8.7.7: Digital CDR die micrograph.