A 0.951 ps_{rms} Period Jitter, 3.2% Modulation Range, DSM-Free, Spread-Spectrum PLL

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***Abstract* - This work presents a delta-sigma modulator free in-loop-bandwidth spread-spectrum clock generator. The proposed charge-based discrete-time loop filter with a digital-to-current converter enables wide range spread-spectrum frequency modulation with significantly relaxed PVT sensitivity. A correlated double sampling technique is leveraged to minimize 1/f noise in the proposed discrete-time loop filter. This work achieves 3.2% spread-spectrum modulation range and 26.51dB spectrum attenuation at 352MHz output frequency. A 142% change in K_{VCO} results in less than 298ppm modulation range error. Implemented in a 0.18µm CMOS, this work achieves 951fs_{rms} period jitter while consuming 9.93mW with a 1.8V supply.**

Keywords - phase-locked loop, spread-spectrum clocking.

I. Introduction

Spread-spectrum clock (SSC) generation is known to be a primary way to manage electromagnetic interference (EMI) issues in consumer products. One such system is a multifunctional print module, which requires an exceptionally demanding SSC specification such as more than 3% modulation range (Δf_{SSC_range}) with 10kHz modulation rate (f_{SSC_rate}) on multiple clock phases.

There are three popular ways to create a spread spectrum modulation: (1) out-of-loop-bandwidth direct SSC modulation, (2) in-loop-bandwidth SSC modulation, and (3) two-point SSC modulation. In the out-of-loop-bandwidth direct modulation technique, the SSC modulation signal directly modulates the control voltage of a voltage-controlled oscillator (VCO) [1]. Because this SSC modulation signal is injected above the loop bandwidth (BW), this scheme requires narrow loop BW, which results in prohibitively large loop filter and limited suppression of VCO noise. Another critical drawback of the direct modulation technique arises because the modulation range changes as the VCO gain (K_{VCO}) varies due to PVT variations.

The in-loop-bandwidth SSC modulation technique employs either frequency domain SSC modulation with a delta-sigma modulator (DSM) [2] or phase domain SSC modulation with a time-to-digital converter (TDC) in all-digital PLLs [3]-[4]. In this technique, the SSC modulation rate is inside the PLL loop BW. The in-loop-bandwidth SSC technique can achieve robust SSC frequency modulation with respect to PVT variations. This is due to the fact that both the DSM based fractional frequency divider and the digitally controlled phase accumulation guarantees the desired frequency division ratio between the input reference frequency (f_{REF}) and the output frequency (f_{OUT}). To achieve both faster SSC modulation rate and larger suppression of the VCO phase noise requires wide PLL loop BW. In case of the DSM based SSC modulators, wide loop BW results in an increase of the in-band shaped DSM noise and in-band spurious tones. In case of phase domain SSC modulation scheme in all-digital PLLs, wide loop BW increases quantization noise from the TDC and digitally controlled oscillator. One can avoid the problem by reducing the loop BW with a low noise LC VCO instead of a ring VCO. However, limited frequency tuning range, area overhead, and inability to create multiple output phases limit the use of the LC VCO for the desired application.

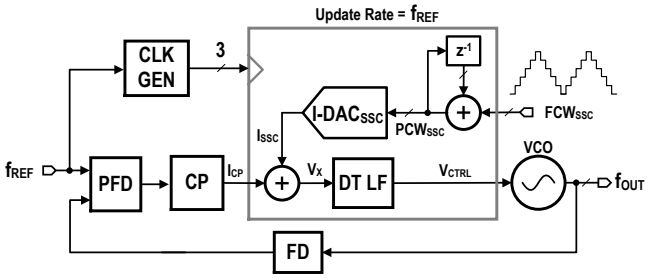


Fig. 1. Proposed spread-spectrum PLL block diagram.

The two-point SSC modulation technique is a combination of both the out-of-loop-bandwidth and in-loop-bandwidth SSC modulation techniques [5]. Two-point SSC modulation technique breaks the trade-off between the PLL loop BW and the modulation rate. However, matching the SSC modulation gains for two different modulation injection points is not trivial, and the out-of-loop-bandwidth SSC modulation gain is still susceptible to the PVT variations of the K_{VCO}.

In view of these limitations of the existing techniques, we present a 352MHz in-loop-bandwidth ring oscillator based SSC generator with a charge-based discrete-time loop filter. Without using a DSM or TDC, the proposed PLL achieves 3.2% in-loop-bandwidth SSC modulation, with significantly reduced PVT sensitivity. The proposed SSC scheme and the correlated double sampling scheme are discussed in Section-II. The measurements and conclusions are given in Section-III and -IV, respectively.

II. Proposed SSC Architecture

Fig.1 shows the block diagram of the proposed spread-spectrum PLL. This proposed architecture consists of phase frequency detector (PFD), charge pump (CP), discrete time

978-1-5090-5191-5/17/$31.00@2017 IEEE

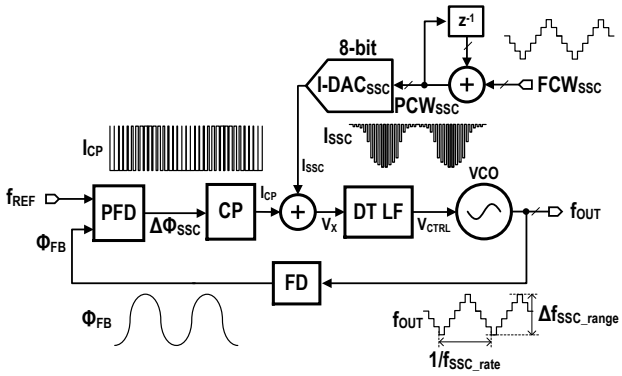


Fig. 2. Proposed in-loop-bandwidth SSC modulation technique.

loop filter (DT-LF), SSC return-to-zero (RZ) current digital-to-analog converter (I-DAC_{SSC}), digital integrator, ring VCO, and frequency divider (FD). The CLK GEN block creates three clock phases for the DT-LF and I-DAC_{SSC} at the rate of f_{REF}. The SSC frequency control word (FCW_{SSC}) is a triangular spread-spectrum modulation signal, and this FCW_{SSC} is digitally accumulated to convert to a phase domain modulation signal (PCW_{SSC}). This accumulated PCW_{SSC} drives the I-DAC_{SSC}, which injects the phase domain spread-spectrum modulation signal inside the loop. The charge-based DT-LF combines both the I-DAC_{SSC} modulation current (I_{SSC}) and charge pump current (I_{CP}), and updates V_{CTRL}.

A. Proposed In-Loop-Bandwidth SSC Modulation

Fig. 2 shows the proposed in-loop-bandwidth SSC modulation technique. The SSC modulation of the output clock is achieved by providing a triangular ramp on the FCW_{SSC}. The digitally accumulated PCW_{SSC} is converted to the return-to-zero I_{SSC} in I-DAC_{SSC}. The magnitude is proportional to PCW_{SSC} and the width is fixed to 50% of the reference period (T_{REF}). Due to the SSC frequency modulation of the VCO, a SSC phase difference ($\Delta\phi_{SSC}$), which is the difference between the divided VCO phase output (ϕ_{FB}) and the input reference frequency phase (ϕ_{REF}), is created. This SSC phase difference $\Delta\phi_{SSC}$ results in the pulse-width modulated I_{CP} at the output of the charge pump. Since this SSC charge pump current I_{SSC} cancels a part of the I-DAC_{SSC} current I_{CP}, the residual current is integrated and converted to a charge signal on a sampling capacitor in the proposed DT LF. This sampled charge signal is filtered to generate a triangular SSC signal at V_{CTRL}, which modulates the VCO output frequency.

The input-output relationship of FCW_{SSC} and VCO output frequency at low frequencies can be approximated as:

$$\frac{f_{OUT}}{FCW_{SSC}} \cong \frac{I_{SSC-LSB}/2}{I_{CP}/M} \times f_{REF} \quad (1)$$

where $I_{SSC\text{-}LSB}$ is the least-significant bit current in the I-DAC_{SSC}, and M is the frequency division ratio in the frequency divider. Please note that (1) does not depend on either design parameters in the proposed DT LF or K_{VCO}. This is because any perturbations on them due to PVT variations are attenuated by the PLL loop gain. This is the key advantage of the proposed technique over the out-of-loop-bandwidth direct SSC and two-point SSC modulations, where any change in the K_{VCO} directly appears at the output. Therefore, the proposed technique achieves superior modulation in the presence of PVT variations without using either a DSM or TDC.

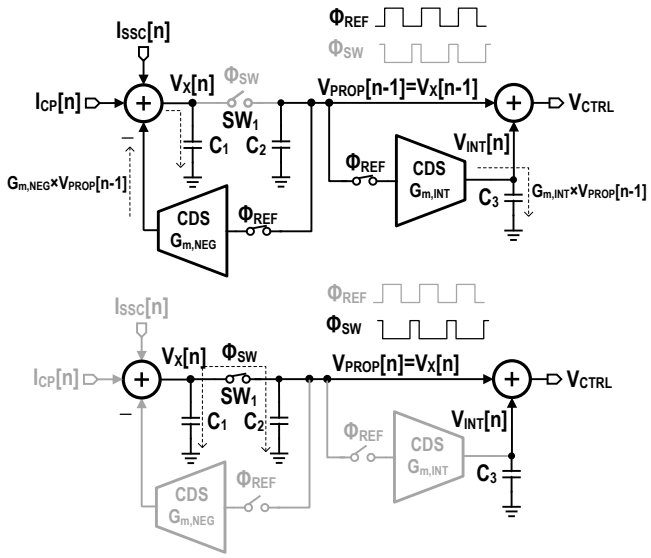


Fig. 3. The block and timing diagrams of the proposed charge-based DT LF.

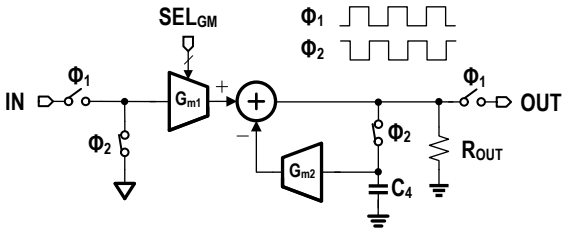


Fig. 4. The correlated double sampling scheme in the transconductors.

The maximum achievable frequency spread spectrum range is limited by the total accumulated $\Delta\phi_{SSC}$ at the PFD input. For proper operation of this spread spectrum PLL, the $\Delta\phi_{SSC}$ must not exceed the reference period T_{REF}. This is because the maximum range for effective phase cancellation from the charge pump and I-DAC_{SSC} in the proposed DT LF is only $\pm\pi$. If the total accumulated $\Delta\phi_{SSC}$ is greater than this limit, it could corrupt the next update sample in the proposed DT LF. Therefore, to achieve wider spread spectrum modulation range, one needs to use lower f_{REF}, indicating that f_{REF} is inversely proportional to the modulation range. Since the maximum loop BW is typically less than $f_{REF}/10$ due to stability concern, lowering f_{REF} reduces the maximum achievable loop BW and results in less suppression of the VCO phase noise. In this work, we demonstrate this trade-off by changing f_{REF} and measure the corresponding spread-spectrum modulation range.

In the proposed architecture, the loop filter input is the sum of I_{SSC} and I_{CP}. The I_{SSC} is a return-to-zero current pulse, whereas the I_{CP} is a pulse-width modulated current pulse. Filtering these two different types of current signals with a conventional passive loop filter creates unacceptable spurs at the output, which destroys the shape of the spread spectrum. Therefore, we propose a charge-based DT LF.

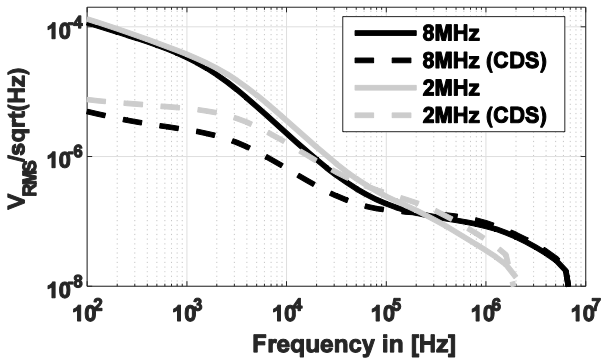


Fig. 5. The proposed DT LF sampled noise at V_{CTRL} for f_{REF}=2MHz and 8MHz, when the CDS is enabled and disabled.

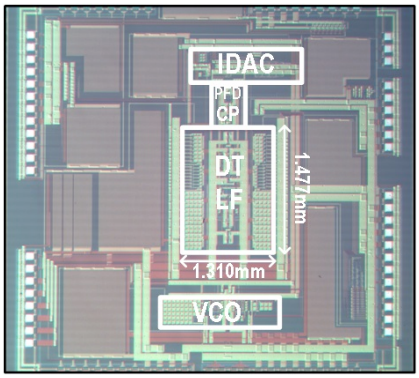


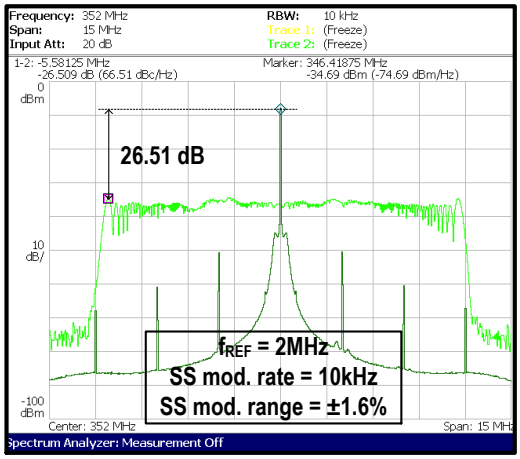
Fig. 6. Die microphotograph.

B. Proposed Charge-Based Discrete-Time Loop-Filter

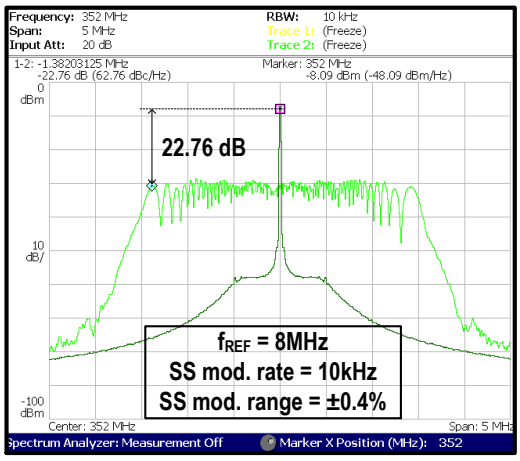
Fig. 3 shows the block and timing diagrams of the proposed DT LF. It consists of two transconductors ($G_{m,NEG}$ and $G_{m,INT}$), three capacitors (C_1, C_2, and C_3), and three switches (SW_1, SW_2 and SW_3). The negative feedback $G_{m,NEG}$ is added to synthesize a stabilizing zero in the loop. This negative feedback loop also reduces the swing on the node V_X, improving the linearity of the charge pump and I-DAC_{SSC}. In addition, the G_{m_INT} integral path makes the proposed PLL a Type-II PLL. The proposed DT LF operates in two phases: ϕ_{REF} and ϕ_{SW}. During ϕ_{REF}, the currents from $I_{SSC}[n]$, $I_{CP}[n]$, and the negative feedback current ($G_{m\_NEG}\times V_{PROP}[n-1]$) are accumulated on the capacitor C_1. At the same time, the SW_3 is closed and the current from G_{m_INT} ($G_{m\_INT}\times V_{PROP}[n-1]$) is integrated on the capacitor C_3. During ϕ_{SW}, the voltage $V_X[n]$ on capacitor C_1 is transferred to C_2 ($C_1 \approx 10C_2$). This switched mode operation of the proposed DT LF helps to isolate the node V_{CTRL} from the large transients, which appear at node V_X during ϕ_{REF}. Therefore, with the help of linear charge domain signal filtering, the proposed DT LF achieves in-loop-bandwidth phase domain SSC modulation without a DSM.

C. Correlated Double Sampling (CDS) Transconductor

The use of active elements in the proposed DT LF results in undesirable offset and 1/f noise. Therefore, the correlated double sampling scheme in [6] is implemented in $G_{m,NEG}$ and $G_{m,INT}$ blocks, as shown in Fig. 4. The CDS transconductor consists of the main and auxiliary transconductor G_{m1} and G_{m2}



(a)



(b)

Fig. 7. Output spectrum when the SSC is enabled and disabled for: (a) f_{REF}=2MHz, (b) f_{REF} = 8MHz.

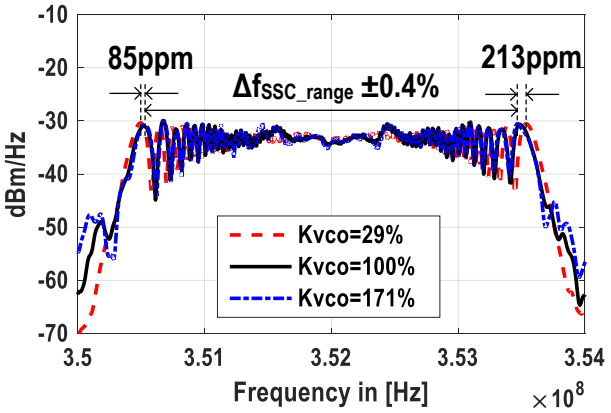
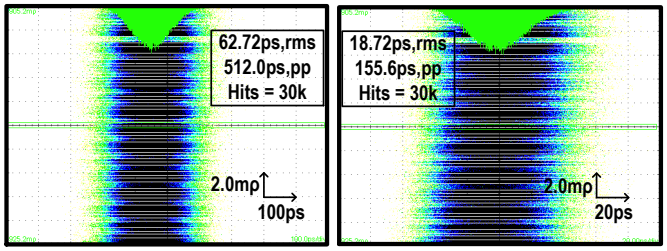


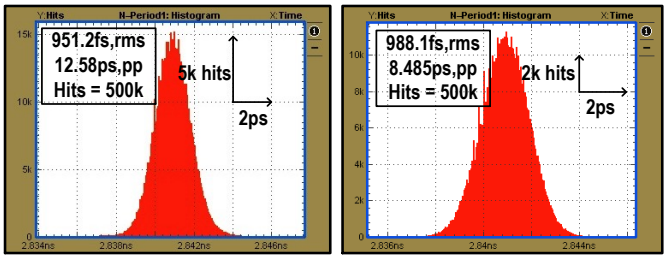
Fig. 8. Measured SSC output spectra for various K_{VCO} values in f_{REF}=8MHz.

with a sampling capacitor C_4. First, the auxiliary G_{m2} forms a negative feedback to sample the offset and 1/f noise during ϕ_2. Then the auxiliary G_{m2} loop compensates the sampled offset and 1/f noise during ϕ_1. Fig. 5 shows the simulated sampled noise at node V_{CTRL} for two different reference frequencies (f_{REF}=2MHz and 8MHz). When the CDS scheme is enabled, a significant reduction of 1/f noise is observed for both references.



(a) (b)

Fig. 9. Absolute jitter measurements for: (a) f_{REF}=2MHz, (b) f_{REF}=8MHz.



(c) (d)

Fig. 10. Period jitter measurements for: (a) f_{REF}=2MHz, (b) f_{REF}=8MHz.

TABLE I. Summary and comparison with state-of-the-art

	This work		[2]	[4]	[3]
Architecture	**Integer-N**		Fract.-N	AD-PLL	AD-PLL
Technology	**180nm**		150nm	65nm	22nm
f_{OUT} [GHz]	**0.352**		1.5	0.375~3.0	0.6~3.6
f_{REF} [MHz]	**2**	**8**	20~40	25	25~200
SSC Scheme	**In-LBW (DT LF)**		In-LBW (DSM)	In-LBW	In-LBW
f_{SSC_rate} [kHz]	**≥ 10**		≥ 31.3	≥ 33	≥ 25
Δf_{SSC_range} [%]	**3.2**	**0.8**	0.5	0.5	2
EMI Atten [dB]	**26.5**	**22.76**	20.3	NA	< 20
Jitter type	**Period**		250 cycle	Period	N-cycle
rms jitter [ps,rms]	**0.951**	**0.988**	8.1	8.16	10.0
P-P Jitter [ps,pp]	**12.6**	**8.49**	NA	75	NA
Supply [V]	**1.8**		1.5	1.1	1.0
Power [mW]	**9.93**		54	2.92 (375MHz)	18.4 (3.6GHz)
Area [mm^2]	**3.01**		0.42	0.38	0.29

III. Measurement Results

The proposed in-LBW SSC PLL was fabricated in a 0.18μm CMOS. The die micrograph is shown in Fig. 6. The proposed PLL consumes 9.93mW total power, while operating from a 1.8V supply. The proposed DT LF dissipates approximately 10% of the total power, and the power penalty due to the I-DAC_{SSC} is less than 5% of the total power.

Fig. 7 shows the measured output spectra for both unmodulated and modulated modes. The SSC attenuation of 26.51dB (f_{REF}=2MHz) and 22.76dB (f_{REF}=8MHz) is achieved. When f_{REF} is increased from 2MHz to 8MHz, the maximum Δf_{SSC_range} is reduced from ±1.6% to ±0.4%, and this reduction demonstrates the trade-off between T_{REF} and Δf_{SSC_range}. To demonstrate PVT insensitive operation, measured SSC outputs are plotted in Fig. 8 for various K_{VCO} values. In f_{REF}=8MHz with the desired ±4000ppm modulation range, a 142% change (from 13.4 to 90.7MHz/volt in 53MHz/volt nominal K_{VCO}) in K_{VCO} results in less than 298ppm change in Δf_{SSC_range}. Measured absolute and period jitters for f_{REF}=2MHz and 8MHz are shown in Fig. 9 and Fig. 10, respectively. For f_{REF}=8MHz, the absolute and period jitters are 18.7ps_{rms} and 988fs_{rms}, respectively. For f_{REF}=2MHz, the absolute and period jitters are 62.7ps_{rms} and 951fs_{rms}, respectively. Finally, Table 1 summarizes the results and compares them with the state-of-the-art PLLs which employ a ring VCO. Thanks to the proposed DT LF, operating at an order of magnitude lower f_{REF}, the proposed PLL achieves an order of magnitude lower period jitter performance, without increasing the power consumption. This work achieves a 3.2% Δf_{SSC_range} with 26.5dB attenuation using the 8-bit I-DAC_{SSC}, whereas the work in [3] requires a 24-bit FCW_{SSC} to deliver a 2% Δf_{SSC_range} with less than 20dB attenuation.

IV. Conclusions

This work proposes a DSM-free in-loop-bandwidth SSC modulation scheme. The proposed in-LBW scheme can maximize the LBW to increase the phase noise suppression of a ring VCO. The I-DAC_{SSC} with the proposed charge-based DT LF establishes the wide spread-spectrum frequency modulation, and this work obtains significantly relaxed PVT sensitivity for the SSC modulation. Finally, the 1/f noise and offset of the proposed DT LF is cancelled using the CDS scheme. This work achieves a 3.2% Δf_{SSC_range} and 26.5dB spread-spectrum attenuation with sub-ps_{rms} period jitter, while consuming 9.93mW with a 1.8V supply. The measured SSC range error is 298ppm with 142% K_{VCO} variation.

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