An 8 Gb/s–64 Mb/s, 2.3–4.2 mW/Gb/s Burst-Mode Transmitter in 90 nm CMOS

Mrunmay Talegaonkar, Student Member, IEEE, Amr Elshazly, Member, IEEE, Karthikeyan Reddy, Student Member, IEEE, Praveen Prabha, Student Member, IEEE, Tejasvi Anand, Student Member, IEEE, and Pavan Kumar Hanumolu, Member, IEEE

Abstract—A burst-mode transmitter achieves 6 ns turn-on time by utilizing a fast frequency settling ring oscillator in digital multiplying delay-locked loop and a rapid on-off biasing scheme for current mode output driver. The resistor tuning-based ring oscillator avoids the use of bias voltages and thereby eliminates the related settling time overhead. The calibrated rapid-on-off biasing circuit utilizes a fast charging technique to achieve bias voltage settling time of 4 ns, resulting in 30X improvement over a diode-connected bias circuit. Fabricated in 90 nm CMOS process, the prototype achieves 2.29 mW/Gb/s energy efficiency at peak data rate of 8 Gb/s. A 125X (8 Gb/s to 64 Mb/s) change in effective data rate results in 67X (18.29 mW to 0.27 mW) change in transmitter power consumption corresponding to only 2X (2.29 mW/Gb/s to 4.24 mW/Gb/s) degradation in energy efficiency for 32 byte long data bursts. We also present an analytical bit error rate (BER) computation technique for rapid on-off links, which uses MDLL settling measurement data in conjunction with always-on transmitter measurements. This technique indicates that the BER bathtub width for $10^{-12}$ BER is 0.65 UI and 0.72 UI during rapid on-off operation and always-on operation, respectively.

Index Terms—Bit error rate, current mode logic (CML) output driver, digital multiplying delay-locked loop (MDLL), digitally-controlled ring oscillator (DCO), energy-proportional operation, fast turn-on clock multiplier, rapid on-off bias.

I. INTRODUCTION

ENERGY efficiency has become a key performance metric for electronic systems ranging from mobile devices to high performance computers. High speed chip-to-chip links consume a significant portion of system power due to continuously increasing data bandwidth requirements. Consequently, design of low power chip-to-chip links has garnered large interest recently. With aggressive use of active power reduction techniques, links with better than 5 pJ/bit energy efficiency at peak data rate have been reported [1]–[3]. In practice, most systems exhibit a wide variety of workload patterns that under-utilize the bandwidth of chip-to-chip links. As a result, low energy per bit operation at peak data rate does not necessarily translate to overall low energy operation.

In accordance with the “energy-proportional performance” design paradigm [4], it is desirable to maintain a constant energy per bit performance of the link over a wide range of data bandwidth requirements instead of constant peak power consumption. Additionally, how quickly a link can respond to changes in data bandwidth requirements heavily influences the amount of energy that can be saved while maintaining acceptable data transfer latency. Adaptive-supply links [5], [6] and burst-mode techniques [7], [8] have been proposed to scale link power consumption based on data bandwidth requirement. Supply voltage is scaled with data rate in adaptive-supply links to achieve better than linear scaling of link power consumption. But, such links have long response time due to slow settling of supply voltage regulators, which introduces a trade-off between response time and supply voltage ripple [9]. Decreasing supply voltage trend in scaled CMOS technologies also limits the range of data rates over which link circuitry can be designed to operate. On the other hand, burst-mode techniques achieve linear scaling of power consumption by putting the link in a low power inactive state when the link is idle. The low power inactive state(s) can be obtained by turning off one (or more) constituent blocks of a link. The turn-on time taken by these blocks, to go from such a low-power inactive state to the active state, decides the response time of the link. While active, the link operates at a fixed data rate. This results in a low complexity link control, and the circuits can be optimized for a fixed data rate operation. In many contemporary chip-to-chip interfaces the bandwidth requirements vary across a wide range within very short time intervals. In such cases, links utilizing fast response time burst-mode techniques can provide more energy savings compared to adaptive-supply links. In this paper, we present a transmitter architecture that seeks to meet the requirements of energy proportional operation using burst-mode techniques.

Two main impediments to realization of rapid on-off transmitters are: (a) slow settling response of clock multiplier, and (b) slow settling bias circuitry. In this paper, we propose techniques that alleviate these issues. To demonstrate the efficacy of these techniques, an 8 Gb/s transmitter with 3-tap feed-forward equalizer (FFE) is designed and the prototype chip is fabricated in 90 nm CMOS process. When operated with 6 ns turn-on
The output driver en-
is DXRO time period and
Fig. 3 show the sim-
reference time
to create three, 8 Gb/s inputs
analysis technique. The paper
discusses the rapid on-off
transmitter architecture in Section II, Section III
details the rapid on-off clock multiplier architecture and its
implementation. The output driver architecture and the proposed
fast settling bias circuit are explained in Section IV. Effect of
supply voltage and temperature drift on rapid on-off operation
is discussed in Section V. The measurement results of the proto-
type chip are given in Section VI along with the proposed BER
analysis technique. The paper concludes with Section VII.

II. PROPOSED ARCHITECTURE

The proposed transmitter architecture is shown in Fig. 1. A
digital multiplying delay-locked loop (MDLL), used as fast
locking clock multiplier, generates 4 GHz clock output MCK
from 500 MHz input reference (REF). Power down signals
PNDB and PDNB_TX are used to turn off the MDLL and output
driver, respectively. A 2:1 serializer combines two 4 Gb/s data
inputs (D_odd, D_even) to create three, 8 Gb/s inputs (D_1, D_0 and D_1) for a CML output driver with 3-tap feed-forward
equalization. The current source bias voltage (VB) for the CML
output driver is obtained using a rapid on-off bias (ROOB)
circuit. ROOB circuit overcomes the trade-off between power
consumption and area of conventional biasing circuits and its
implementation details are discussed in Section IV.

MDLLs provide many advantages such as reduced jitter ac-
cumulation, low sensitivity to power supply noise [10], [11] and
have also been shown to have the benefit of fast power-on time
[12]. These advantages are derived by selectively replacing oscil-
lator edge with the reference edge that resets the oscillator
phase every reference clock cycle. Oscillator phase reset caused
by this selective edge replacement can be used to establish a
fixed phase relationship between oscillator phase and reference
input, thereby alleviating slow phase settling transients common
in conventional PLLs. However, in practice, turn-on time of the
MDLL is limited by the slow frequency settling response of the
oscillator [12]. We further elucidate this issue and propose tech-
niques to overcome it next.

III. DESIGN OF RAPID ON-OFF CLOCK MULTIPLIER

A. MDLL Architecture

The proposed digital MDLL architecture is shown in Fig. 2.
A 500 MHz reference clock (REF) is multiplied by a factor
of 8 to generate a 4 GHz output clock (OUT). A power-down
signal (PNDB) is used to gate the REF input when MDLL is
needed to be turned off. The PDNB signal is retimed with re-
spect to the REF input to avoid any glitches on the gated ref-
ence clock, REFG. Under locked condition, DXRO oscillates
at 4 GHz to provide frequency-multiplied clock output. Select
signal for multiplexer that replaces every 8th DXRO positive
edge with positive edge of REFG is generated using the SELG
block. A D flip-flop (DFF) is used as a bang-bang phase de-
tector for the DXRO frequency tuning loop. The DFF output
is demodulated by a factor of 8 using a majority voting (MV)
block. The early/late outputs from the MV block are fed into
an 11 bit digital accumulator (ACC), clocked at much lower
frequency of 62.5 MHz. This reduces the power consumed in
the ACC block at the expense of slower frequency acquisition
of the DXRO tuning loop. The 11 bit output of ACC is further
truncated to reduce the steady state dithering of the ACC output
and the resulting output jitter. An 8 bit digital input D_CTRL to
the DXRO tunes its frequency to 8 \( F \_REF \). Fig. 3 shows the sim-
ulated waveforms for initial frequency acquisition and subse-
quent rapid on-off operation of the MDLL. During slower initial
frequency acquisition, MDLL uses classical negative feedback
loop to acquire lock. After this initial lock acquisition, MDLL
cannot be used for rapid on-off operation by exploiting the fast-on
property of MDLL as discussed next.

To briefly illustrate fast turn-on property of MDLL, consider the
timing diagram shown in Fig. 4. In steady state, the MDLL
is locked and DXRO control ensures that \( 8T \_DSC = T \_REF \),
where \( T \_DSC \) is DXRO time period and \( T \_REF \) is reference
time period. The SEL signal is generated once every reference cycle
to pass the positive edge of REFG to the DXRO. In the absence
of reference edge, the MDLL waits for positive edge on REFG
when SEL signal is logic HIGH. As the ring oscillator loop is
open in this condition, the DXRO output does not oscillate and
remains at a fixed voltage level. Under these circumstances, the

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Fig. 1. Block diagram of the proposed transmitter.

Fig. 2. Block diagram of the proposed digital MDLL architecture.
MDLL is considered to be off. When the positive edge on REFG arrives, it is propagated through the DXRO delay chain and the SEL signal is de-asserted to close the ring oscillator loop. If the DXRO frequency is exactly restored to its steady state value, the MDLL achieves instantaneous phase locking.

B. Digitally Controlled Multiplexed Ring Oscillator (DXRO)

Turn-on time of the MDLL is governed by how quickly DXRO settles to the desired steady state output frequency during the turn-on transient. A DXRO used in the fast-locking MDLL design must fulfill the following requirements: (a) fast frequency settling, (b) output state retention in off-state, and (c) ultra-low power consumption in off-state. CMOS inverter-based pseudo-differential delay cells are well suited for implementing DXROs as they can maintain the logic state while consuming only leakage power in the off-state. They also exhibit better steady-state phase noise performance owing to their large output swing. Therefore, we focus on their frequency settling properties.

The frequency settling of the oscillator mainly depends on the frequency tuning circuitry. A common method for digital control of frequency is by current-starving the delay cells as shown in Fig. 5 [12]. During MDLL turn-on, the oscillator tuning control voltage \( V_{CTRL} \) experiences large variations. Large drain to gate parasitic capacitor of \( M_{p} \) (\( C_g \) in Fig. 5(a)) couples \( V_{CTRL} \) to \( V_{DAC} \) and increases settling time, as illustrated in Fig. 5(c). Similar behavior is observed in case of current-starved ring-oscillator-controlled using current-mode DAC shown in Fig. 5(b). To minimize this disturbance, the output impedance of voltage mode DAC in Fig. 5(a) (BIASGEN in case of Fig. 5(b)) needs to be very low, resulting in increased power consumption. Alternatively, using a large decoupling capacitor on the \( V_{DAC} \) node increases area. In addition, the current-starved oscillator also consumes current in the off-state in the always-on DAC or the always-on BIASGEN circuit. In view of these drawbacks, we propose to use a digitally controlled resistor based tuning that does not require analog bias voltages, and thereby eliminates the related settling time of bias generation.

The circuit diagram of the variable delay stage is shown in Fig. 7(a). It uses feed-forward resistors \( R_{x} \) to achieve pseudo-differential operation. Digitally controlled MOS capacitors, controlled using 2 bit code \( D_{CONFUSE} \), are used for coarse frequency tuning across process corners. Fig. 7(b) shows the circuit diagram of the swing restore stage. The back-to-back connected inverters provide pseudo-differential operation as well as rudimentary duty cycle correction. Dummy multiplexer and delay stages are used to ensure identical loading during edge replacement mode as well as closed loop oscillator mode of operation of DXRO. The use of swing restore stage matches the reference clock waveform to oscillator output waveform, and eliminates any disturbance to variable delay stage supply voltages due to reference injection. This reduces reference spur without using an explicit decoupling capacitor at nodes \( V_{CP} \) and \( V_{CN} \), which in turn improves settling time.

The RDACs influence many important MDLL performance metrics such as frequency tuning range and settling time, loop dynamics, output jitter due to frequency (or equivalently period) quantization error. For an RDAC-based tuning, the period quantization error, \( \Delta T_Q \), is given by

\[
\Delta T_Q \approx k \Delta R_{RDAC}
\]

where \( k \) is a constant of proportionality decided by delay cell circuit parameters and supply voltage, and \( \Delta R_{RDAC} \) is the RDAC resistance step size. The deterministic jitter, \( T_{DQ} \), due to quantization error for frequency multiplication factor,
The most area efficient way to obtain variable resistance using MOS transistors is to use a parallel combination of identical MOS transistors as digitally switched unit elements. However, as MOS transistor resistance \( R_{\text{on}} \) is inversely proportional to its width, using a parallel combination of identical MOS transistors results in \( 1/x \) RDAC transfer characteristic, which degrades period quantization error performance of DXRO. To avoid this degradation, a linear RDAC transfer characteristic is desired. To this end, multiple banks of parallel MOS devices are used, as depicted in Figs. 8(a) and 8(b), to improve RDAC linearity using piece-wise linear approximation. The devices in each bank are identically sized to closely match a linear RDAC transfer characteristic in a narrow code-range. A linear RDAC transfer characteristic over all the codes is obtained by combining piece-wise linear characteristics of individual banks. Thermometer coding is utilized to ensure monotonicity even in the presence of mismatch between unit resistors. The simulated DXRO period as function of input digital code of the RDAC is shown in Fig. 9, and the period resolution of the DXRO is less than 300 fs under typical conditions. This quantization error would result in worst case peak to peak jitter of 2.4 ps. From Fig. 9, the simulated frequency tuning range of the DXRO is observed to be from 3.78 GHz to 4.34 GHz, for a single coarse control code. Simulations also indicate that the overall frequency tuning range, obtained by utilizing coarse tuning code \( D_{\text{COARSE}} \), is from 3 GHz to 4.72 GHz under typical conditions. Compared to [13], [14], which utilize a series-parallel combination of MOS
transistors to improve RDAC linearity, this work uses only parallel combination of MOS transistors to minimize area.

As illustrated in Fig. 8(c), the RDAC resistance affects the poles associated with DXRO frequency settling, and therefore plays an important role in deciding the frequency settling time. The simulated transient settling waveforms for the DXRO turn-on event are shown in Fig. 10. When DXRO is turned off, $V_{CP}$ and $V_{CN}$ reach the supply and ground voltages, respectively. After DXRO is turned on, it starts oscillating at higher frequency and, $V_{CP}$ and $V_{CN}$ nodes start settling with time constants given by

$$\tau_P = R_{RDAC,P} \cdot C_{PAR,P}$$
$$\tau_N = R_{RDAC,N} \cdot C_{PAR,N}$$

where $R_{RDAC,P}$ and $R_{RDAC,N}$ are resistances of P-RDAC and N-RDAC, respectively. $C_{PAR,P}$ and $C_{PAR,N}$ are parasitic capacitances on nodes $V_{CP}$ and $V_{CN}$, respectively. The initial faster DXRO oscillations result in input multiplexer select signal SEL going high early. Consequently, DXRO waits longer for reference input edge. During this period, DXRO current consumption reduces and node voltages $V_{CP}$ and $V_{CN}$ ramp up and down, respectively (see Fig. 10). Longer DXRO waiting time results in larger disturbance on $V_{CP}$ and $V_{CN}$ node voltages, which further increases the settling time. Therefore, for faster DXRO frequency settling, it is desirable to have $\tau_P, \tau_N < T_{REF}$.

IV. DESIGN OF 3-TAP OUTPUT DRIVER

Fig. 11 shows the top level block diagram of the output driver. A half rate architecture [15] with a 3-tap 2:1 serializer and a segmented CML output driver is used. In this work, use of CML output driver is preferred over a low swing voltage mode output driver. Use of low swing voltage mode output driver entails additional supply regulator based impedance control loop [1] for its output driver and pre-driver. This increases the complexity for rapid on-off operation. On the other hand, CML output driver utilizes passive terminations and does not need...
additional supply regulators for impedance control. The efficiency benefits of the voltage mode drivers are also diminished when additional pre-driver overhead and pre-emphasis is considered [16]. A ROOB circuit provides the bias voltage \( V_{BB} \) for the CML output driver tail current sources. The ROOB block turns off the CML output driver when transmitter is inactive and rapidly turns it back on when transmitter is required to be active. The 3-tap 2:1 serializer multiplexes two 4 Gb/s bit-streams \((D_{ODD}, D_{EVEN})\) using the 4 GHz MDLL output clock MCK to generate pre-cursor \((D_{-1})\), main cursor \((D_0)\), and post-cursor \((D_1)\) data outputs at 8 Gb/s. The implementation details of CML output driver and ROOB block are described in following subsections.

A. CML Output Driver

The power dissipation of the CML output driver is split between the final output driver stage and the pre-driver stage. While the power consumption of the final stage can be scaled with output swing requirement, pre-driver stage power consumption cannot be easily scaled. Segmentation provides a way to coarsely scale pre-driver power consumption with outputs swing requirement by turning on only a required number of segments while other segments are turned off. In this work, the main tap is connected to 4 segments while the pre-cursor and post-cursor taps are connected to 1 and 2 segments, respectively. The 2 bit tail current source in each segment can be used to set FFE coefficient and/or to control output swing of the output driver.

The circuit diagram of a unit segment is shown in Fig. 12. It consists of a CMOS to CML converter [17] that increases the common mode level of CMOS inputs coming from the 2:1 serializer and drives the CML pre-driver stage. To turn off the segment, the input to the CMOS to CML converter is gated such that both its inputs are at logic LOW level and ENB is pulled to logic HIGH level. This cuts off the current steering devices of the output driver stage. The tail current sources of the output driver stage are also turned off by applying logic LOW input to EN[3:0].

B. Rapid On-Off Biasing Scheme

The amplitude settling of the CML output driver mainly depends on its tail current source bias voltage settling during on-off operation. The conventional diode-connected MOS transistor based circuit used for current source biasing is shown in Fig. 13(a). If bias current \( I_{BB} \) is cut off when transmitter is off, the turn on settling time of the bias voltage node VB is proportional to \( \frac{1}{g_{n,nn}} \), where \( g_{n,nn} \) is the transconductance of the diode-connected transistor \( M_{NB} \). To achieve faster settling, we either need to increase the bias current \( I_{BB} \) or decrease decoupling capacitance \( C_B \). Increasing \( I_{BB} \) results in an increased power consumption. On the other hand, \( C_B \) helps in mitigating effects such as coupling from other stray signals and inter-symbol interference (ISI) due to coupling between tail node voltage variations of CML stages and bias voltage node VB. Therefore reduction in \( C_B \) adversely affects output signal integrity.

To overcome this problem, we propose a calibrated ROOB circuit that provides an additional charging path for \( C_B \) resulting in faster settling. The proposed circuit occupies very small area and does not consume any static current. As illustrated in Fig. 13(b), the basic principle behind operation of the ROOB circuit is to rapidly charge the capacitor \( C_B \) through \( M_{PC} \) until voltage of node VB reaches a value of \( V_{Tresh} \). In the proposed circuit, \( V_{Tresh} \) is identified using simple digital calibration and the comparator is implemented using CMOS.
logic circuits. Referring to Fig. 13(c), the ROOB circuit operation can be described as follows. In off state, PDNB_{TX} and its complementary signal $\bar{PDNB}_{TX}$ are logic LOW and logic HIGH, respectively. As a result, $C_B$ is completely discharged ($V_B = 0$) and node VX is pulled high. Consequently, the signal VFB is also pulled high. When ROOB is turned on by driving PDNB_{TX} to logic HIGH, the diode connected transistor $M_{NH}$ starts sinking current, and VB node voltage starts rising. After PDNB_{TX} goes HIGH, VFB goes to logic LOW, turning on the fast charging PMOS transistor $M_{PC}$. It helps VB node voltage to approach its steady state value rapidly, as indicated by the simulated waveform labeled $V_{B\text{ROOB}}$ in Fig. 14. It can also be seen that using only diode connected transistor would result in much slower settling similar to the waveform labeled $V_{B\text{Diio}}$ in Fig. 14. To avoid excessive overshoot on VB node voltage, a variable threshold inverter formed by a programmable load and $M_{NC}$ is used. When node VB reaches the voltage where $M_{NC}$ can overcome the pull up load, node VX is pulled low. As a result VFB goes to logic HIGH and the additional charging path provided by $M_{PC}$ is turned off. Subsequently ROOB circuit behaves similar to a conventional diode-connected bias circuit as shown in the region marked “Bias Diode-like Settling” in Fig. 14. A 4 bit thermometer coded programmable load is used that provides around 10% initial settling accuracy after 4 ns with threshold calibration. The programmable load consists of a PMOS transistor $M_{PL}$ and an NMOS transistor $M_{NL}$. The total resistance of the load is dominated by $M_{NL}$ and $M_{PL}$ is used to enable or disable the load branch. Use of NMOS transistor as main load provides better tracking of temperature variation compared to a PMOS only load.
During initial calibration of the programmable load, \( M_{PC} \) is disabled and the programmable load resistance is set to its lowest value. Beginning with completely discharged \( C_B \), the diode connected transistor \( M_{NB} \) is allowed to slowly pull VB node to its steady state value. Due to stronger pull-up load, \( M_{NC} \) cannot pull the node VX down to ground. The state of VX node is detected by sampling signal VFB. The programmable load resistance is then increased and \( C_B \) is discharged. The diode connected transistor \( M_{NB} \) is again allowed to slowly pull VB node to its steady state value. This procedure is repeated until \( M_{NC} \) can pull the node VX down to ground. Corresponding code for load strength is used for subsequent rapid on-off operation of the transmitter. In current implementation, the initial calibration is performed manually but an automatic digital state machine based calibration can be easily implemented.

V. EFFECT OF SUPPLY VOLTAGE AND TEMPERATURE DRIFT ON RAPID ON-OFF OPERATION

In typical electronic systems, supply voltage and temperature drift are the result of many factors such as long term stability of voltage references, ambient temperature, and on-chip power dissipation. For example, the study in [18] measured thermal time-constants, \( \tau_{TH} \), between 5 ms and 300 ms for die temperature changes caused by variations in power dissipation. Such long time constants have little impact on the performance of burst-mode operation if the off durations \( (T_{OFF}) \) are relatively small \( (T_{OFF} \ll \tau_{TH}) \). For a very large \( T_{OFF} \), it becomes necessary to intermittently turn on the interface to compensate for variations in operating conditions, albeit at a slightly reduced energy efficiency. Such system level techniques to reduce the impact of supply voltage and temperature drift on a burst-mode on-off interface are being actively explored [19]. In the following, we quantify the temperature and voltage dependence of the MDLL and ROOB.

A. Effect on MDLL

The simulated sensitivities of the DXRO period to drift in supply voltage and temperature are \(-258 \text{ fs/mV}\) and \(303 \text{ fs/°C}\), respectively. In the on-state, MDLL’s frequency tuning loop tracks these drifts. However, in the off-state no such tracking is possible. As a result, when the MDLL is turned-on, the DXRO period not only depends on the previous state of digital loop filter but also on the drift in supply voltage and temperature. Denoting the additional period change caused by drifts as \( \Delta T_{drift} \), the initial deterministic period jitter is equal to \( 8\Delta T_{crit} \). This jitter reduces as MDLL corrects the DXRO period error at a rate governed by the loop parameters, which is equal to approximately 1.1 fs/ns in this design.

B. Effect on Rapid On-Off Biasing Circuit

The simulated typical ROOB settling error after 4 ns is found to be 11.12% and changes at the rate of 0.74%/mV, and \(-0.005%/°C\), with drift in supply voltage and temperature, respectively. The ROOB exhibits good tolerance to temperature variations due to use of NMOS programmable load device. The sensitivity of ROOB to supply voltage can be attributed to change in threshold voltages of programmable load inverter as well as subsequent logic gate delays due to supply variation.
performance of the equalizer is limited by the duty cycle error amplification due to channel loss. The output driver, including the 2:1 serializer, consumes 14.56 mW power in 1-tap mode and 16.45 mW power in 3-tap mode for a 500 mV output swing.

B. On-Off Measurements

To test the on-off behavior of the MDLL, an arbitrary waveform generator (Tektronix AWG7122B) is used to generate the reference clock (REF) as well as the power down signal (PDNB). PDNB is also used to trigger the real-time oscilloscope (Tektronix TDS6804B) and equivalent time oscilloscope (Tektronix DSA8200) waveform capture. Fig. 19(a) depicts the measured MDLL output settling waveform captured using the equivalent time oscilloscope. The MDLL time period deviation during settling, relative to its steady-state mean time period, is computed from the waveform data captured using real-time oscilloscope and is shown in Fig. 19(b). The period error is always less than ±5% during the settling transient, demonstrating the efficacy of the proposed DXRO architecture. After three reference cycles, period error is very close to the steady-state period jitter of the MDLL. Comparison of MDLL performance with the state of the art, shown in Table I, illustrates that this work achieves superior jitter and power efficiency performance compared to conventional analog MDLL-based clock multipliers [10], [20] in addition to being amenable to rapid on-off operation.

The transmitter settling transient during turn-on, with and without the proposed ROOB circuit, is shown in Fig. 20(a). The measurements indicate that it takes more than 120 ns to settle without the ROOB circuit, and around 4 ns when the ROOB circuit is utilized (Fig. 20(b)), representing a nearly 30X improvement.

Fig. 21(a) depicts the block-wise measured power consumption of the transmitter in always-on and off-state. The total on-state power is 18.29 mW (2.29 mW/Gb/s) whereas the off-state power is 0.11 mW in 1-tap mode. The off-state power is dominated by the sub-threshold leakage current in MDLL and serializer both of which use CMOS circuits and low-V_t transistors for high speed operation. The average power consumption for 4, 8, 32, and 128 byte long bursts as a function of effective output data rate for 6 ns turn-on time is plotted in Fig. 21(b). All the measurements are made with PRBS-7 data output, 1-tap transmitter mode and without any additional PCB channel. As illustrated in Fig. 21(c), for each burst mode transfer, total on-time of the transmitter is decided by initial turn-on latency time and data transfer time. For example, to achieve 2 Gb/s effective data rate with 4 byte long burst, the transmitter is on for first 10 ns, out of which 6 ns is turn-on latency time and data transfer time is 4 ns at the data rate of 8 Gb/s. The transmitter is turned off for the following 6 ns. Owing to the short turn-on time, the transmitter power consumption is proportional to effective data rate translating to almost constant energy efficiency. When the effective data rate is changed by 125X (8 Gb/s to 64 Mb/s), transmitter power consumption scales by 67X (18.29 mW to 0.27 mW) resulting in only 2X degradation in energy efficiency (2.29 mW/Gb/s to 4.24 mW/Gb/s) for 32 byte data bursts. At ultra-low effective data rates, the off-state power starts dominating and therefore energy efficiency degrades at much faster rate. The transmitter transition energy is computed to be 95 pJ. Beneﬁts of operating all the blocks in rapid on-off mode are evident from Table II, which shows estimated energy efﬁciency that can be achieved by selectively operating one or more blocks in rapid on-off mode for 32 byte long burst-mode transfer at an average data rate of 64 Mb/s. Table III compares the transmitter with state-of-the-art CML output driver based
transmitters. The energy efficiency of the transmitter in always-on state is comparable to other transmitters, while further energy savings can be obtained by rapid on-off operation of the proposed transmitter.
TABLE I

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<td>Architecture</td>
<td>DMDLL</td>
<td>PLL</td>
<td>MILO</td>
<td>MILO</td>
<td>DMDLL</td>
<td>MDLL</td>
<td>MDLL</td>
</tr>
<tr>
<td>Area [mm²]</td>
<td>0.1</td>
<td>—</td>
<td>—</td>
<td>0.149b</td>
<td>0.16</td>
<td>0.025</td>
<td>0.05</td>
</tr>
</tbody>
</table>

* Deterministic jitter  
  b Includes output drivers

TABLE II

<table>
<thead>
<tr>
<th>Mode</th>
<th>O/P Driver</th>
<th>MDLL</th>
<th>ROOB</th>
<th>Est. Energy Eff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>Rapid On-Off</td>
<td>Always-On</td>
<td>Always-On</td>
<td>62.7 pJ/b</td>
</tr>
<tr>
<td>P2</td>
<td>Rapid On-Off</td>
<td>Rapid On-Off</td>
<td>Always-On</td>
<td>5.9 pJ/b</td>
</tr>
<tr>
<td>All Rapid On-Off</td>
<td>Rapid On-Off</td>
<td>Rapid On-Off</td>
<td>Rapid On-Off</td>
<td>4.2 pJ/ba</td>
</tr>
</tbody>
</table>

* Measured energy efficiency

C. Analytical On-Off BER Computation

While MDLL period error settling characteristic indirectly indicates how quickly an on-off interface can return to its steady state, it does not provide information about the settling time after which the link can be used to obtain the required BER performance. Based on information obtained from measurements, we can statistically predict the effect of MDLL settling characteristic on the transmitter performance for the simplified link architecture shown in Fig. 22(a). We also make the following assumptions. (a) The on-off data transmission does not affect the receiver sampling phase which is nominally at the center of data in steady-state. (b) The effect of ROOB settling is neglected and the output driver swing does not change during on-off operation. (c) Data is transferred in bursts consisting of a fixed number of bits N_B. (d) Data dependent jitter (DDJ) probability distribution function (pdf) remains the same. The effect of MDLL period settling due to on-off operation on receiver sampling is illustrated in Fig. 22(b). Due to initial frequency settling of the MDLL, the receiver can not sample the data in the middle of the data bit. If the MDLL zero crossing time instants \( t[i] \) are known, time instants corresponding to the middle of each data bit can be calculated. As shown in Fig. 22(b), we denote the difference between middle of the data bit and the corresponding receiver clock zero crossing time instant by \( \varepsilon_a[i] \). The sequence \( \varepsilon_a[i] \) represents the receiver sampling error due to imperfect frequency settling of the MDLL. Further, if we also know the steady-state
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Fig. 21. (a) Power consumption of the transmitter for on and off states, (b) power consumption and energy efficiency of the transmitter for varying effective data rate, and (c) illustration of data transfer pattern used for varying effective data rate in measurement.

Fig. 22. (a) Link configuration used to analyze effect of on-off operation on link BER, and (b) illustrated sampling errors induced by MDLL frequency settling with ideal receiver clock.

total jitter pdf of the data at the receiver, we can construct a statistical BER bathtub using the following equation for bit error probability:

\[
P_{\text{hit}}(\phi) = \frac{1}{2N_{\phi}} \sum_{i=1}^{N_{\phi}} \left( 1 - F_T \left( 0.5 - \frac{\epsilon_x[i]}{T_{\text{bit}}} - \phi \right) + F_T \left( -0.5 - \frac{\epsilon_x[i]}{T_{\text{bit}}} - \phi \right) \right)
\]

where \(F_T(\phi)\) is the cumulative distribution function (CDF) of total jitter at a phase offset \(\phi\), normalized to unit interval (UI), from the middle of the data eye in always-on condition. The ideal bit period is denoted as \(T_{\text{bit}}\).

The 80SJNB software tool [21] in conjunction with Tektronix DSA8200 is used to obtain \(F_T(\phi)\) under always-on condition for PRBS-7 data output at 8 Gb/s. MDLL period settling characteristic shown in Fig. 19(b) is used to compute the BER bathtub characteristics for varying burst lengths and turn-on latency, \(T_{\text{lat, on}}\).
TABLE III
TRANSMITTER PERFORMANCE COMPARISON.

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>VLSI’11 [8]</th>
<th>JSSC’08 [16]</th>
<th>JSSC’10 [3]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90 nm</td>
<td>40 nm</td>
<td>65 nm</td>
<td>45 nm</td>
</tr>
<tr>
<td>Supply [V]</td>
<td>0.95/1.0</td>
<td>–</td>
<td>0.85/1.2</td>
<td>0.80</td>
</tr>
<tr>
<td>Output Data rate [Gb/s]</td>
<td>8.0</td>
<td>5.6</td>
<td>10.0</td>
<td>10.0</td>
</tr>
<tr>
<td>O/P Swing[mVpp]</td>
<td>500</td>
<td>–</td>
<td>100</td>
<td>150</td>
</tr>
<tr>
<td>Tx Equalization</td>
<td>3-Tap FIR</td>
<td>None</td>
<td>3-Tap FIR + Pass. RL</td>
<td>2-Tap FIR</td>
</tr>
<tr>
<td>Tx Power [mW]</td>
<td>14.56a / 16.45b</td>
<td>–</td>
<td>17</td>
<td>5.28</td>
</tr>
<tr>
<td>Tx Eff. [mW/Gb/s]</td>
<td>1.82a / 2.06b</td>
<td>–</td>
<td>1.70</td>
<td>0.53</td>
</tr>
<tr>
<td>Rapid On-Off Bias</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>(Settling Time)</td>
<td>(~4 ns)</td>
<td>(&lt;2 ns)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Eff. [mW/Gb/s]</td>
<td>2.29b / 2.52b</td>
<td>2.4d</td>
<td>3.6e</td>
<td>1.40f</td>
</tr>
</tbody>
</table>

a 1-Tap mode  b 3-Tap mode  c Includes 1 Tx lane with 1 MDLL  d Extrapolated for 8 Tx+Rx links  e Includes 1 lane Tx+Rx  f Includes 47 lane Tx+Rx, 1 lane fwd. clock, 1 IL-VCO

Fig. 23(a) shows such computed BER bathtub characteristics for 32 byte, and 128 byte long bursts for \(T_{\text{lat, on}}\) of 6 ns, for a 32 byte burst with \(T_{\text{lat, on}}\) of 12 ns, and the always-on BER bathtub characteristic. It can be seen that the BER bathtub width for \(10^{-12}\) BER is strongly affected by \(T_{\text{lat, on}}\) whereas burst length, \(N_B\), plays only a minor role. The BER bathtub width marginally improves with increasing \(N_B\). To further illustrate the effect of \(T_{\text{lat, on}}\) on width of BER bathtub, a plot of BER bathtub width as a function of \(T_{\text{lat, on}}\) for 32 byte long transfers is shown in Fig. 23(b). Further analysis suggests that the transmitter BER settling is mostly unaffected in presence of longer PRBS sequence length or higher channel loss. This is because initial timing errors are mainly dominated by MDLL frequency settling rather than data dependent jitter (DDJ). It should be noted that the steady-state BER bathtub width will be smaller with larger DDJ, similar to conventional always-on transmitters.

VII. CONCLUSION
We have presented a rapid on-off transmitter that, owing to its short turn-on time, has power consumption proportional to its effective data rate, translating to an almost constant energy efficiency over a wide range of utilization levels. The transmitter operates over a 125X range (8 Gb/s to 64 Mb/s) with energy efficiency variation of only 2X (2.29 to 4.24 mW/Gb/s) for 32 byte data bursts. A fast frequency settling DXRO architecture and a rapid on-off biasing circuit have been proposed
to achieve this performance. The DXRO architecture uses resistor-based tuning and avoids the use of bias voltages for fast frequency settling. The fast charging technique used for ROOB circuit shows almost 30X improvement in its settling time compared to a diode-connected bias circuit. We have also proposed an analytical BEK derivation method to evaluate the impact of transmitter rapid on-off operation on the BER performance of the link using MDLL settling measurements and always-on transmitter measurements.

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REFERENCES


Mrunmay Talegaonkar (S’10) received the B.Tech. degree in electrical engineering and the M.Tech. degree in microelectronics and VLSI design from the Indian Institute of Technology Madras, Chennai, India, in 2007. He is currently pursuing the Ph.D. degree at University of Illinois, Urbana-Champaign, IL, USA.

Between 2007 and 2009, he worked as a design engineer at Analog Devices, Bangalore, India, where he was involved in design of digital-to-analog converters. During 2009–2010, he was a project associate at Indian Institute of Technology Madras, working on high speed clock and data recovery circuits. From 2010 to 2013, he was a research assistant, working on high speed links, at the Oregon State University, Corvallis, OR, USA. His research interests include high speed I/O interfaces and clocking circuits.

Amr Elshazy (S’04–M’13) received the B.Sc. (Hons.) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2003 and 2007, respectively, and the Ph.D. degree from the Oregon State University, Corvallis, OR, USA, in 2012, all in electrical engineering.

He is currently a Design Engineer at Intel Corporation, Hillsboro, OR, USA, developing high-performance high-speed I/O circuits and architectures for next generation process technologies. From 2004 to 2006, he was a VLSI Circuit Design Engineer at AIA/T, Inc. working on the design of RF building blocks. From 2006 to 2007, he was with Mentor Graphics Inc., Cairo, designing multi-standard clock and data recovery circuits. His research interests include high-speed serial-links, frequency synthesizers, digital phase-locked loops, multiplying delay-locked loops, clock and data recovery circuits, data converter techniques, and low-power mixed-signal circuits.

Dr. Elshazy received the Analog Devices Outstanding Student Designer Award in 2011, the Center for Design of Analog-Digital Integrated Circuits (CADIC) Best Poster Award in 2012, and the Graduate Research Assistant of the year Award in 2012 from the College of Engineering at the Oregon State University. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, IEEE
Karthikeyan Reddy (S’11) received the B.E. degree in electronics and communication engineering from the College of Engineering, Chennai, India, in 2004, the M.S. degree from the Indian Institute of Technology, Madras, India, in 2008, and the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 2014. From 2008 to 2010, he was a Design Engineer with Texas Instruments, Bangalore, India. He was a Design Intern with Silicon Labs, Austin, during the summer of 2012. Presently, he is with Linear Technology. His research interest is in the area of high speed delta sigma modulators and precision DACs.

Praveen Prabha (S’12–M’14) received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology, Calicut, India, in 2006, and the M.S. degree in electrical engineering from Oregon State University, OR, USA, in 2014. From 2006 to 2011, he was with Texas Instruments, Bangalore, India, where he designed low power integrated circuits for audio applications. From 2011 to 2013, he was a research assistant in Mixed Mode Integrated Circuits group at Oregon State University where he worked on VCO based ADCs for sensor applications. He is currently with the Precision Mixed Signal team at Broadcom, Irvine, CA, USA, where he is focused on integrated circuits for audio codecs. His research interests include low power data converters, power management circuits and frequency synthesizers.

Tejasvi Anand (S’12) is currently pursuing the Ph.D. degree at the University of Illinois at Urbana-Champaign, IL, USA. He received the M.Tech. degree (first class with distinction) in electronics design and technology from the Indian Institute of Science, Bangalore, India, in 2008. From 2008 to 2010, he worked as an Analog Design Engineer at Cosmic Circuits (now a part of Cadence), Bangalore, on the design of analog-to-digital converters. From 2010 to 2011, he worked as a Project Associate at Indian Institute of Science, Bangalore, where he was involved in the design of neural recording system and RF building blocks. His research interests are in energy efficient high-speed wireline communication systems, frequency synthesizers, data converters and energy efficient sensors. Mr. Anand received the Analog Devices Outstanding Student Designer Award in 2013.

Pavan Kumar Hanumolu (S’99–M’07) is currently an Associate Professor in the Department of Electrical and Computer Engineering and a Research Associate Professor with the Coordinated Science Laboratory at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, Corvallis, in 2006, where he subsequently served as a faculty member till 2013. Dr. Hanumolu’s research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion. Dr. Hanumolu received the National Science Foundation CAREER Award in 2010. He currently serves as an Associate Editor of the JOURNAL OF SOLID-STATE CIRCUITS, and is a technical program committee member of the VLSI Circuits Symposium, and International Solid-State Circuits Conference.