A 5 GHz Digital Fractional-*N* PLL Using a 1-bit Delta–Sigma Frequency-to-Digital Converter in 65 nm CMOS

Mrunmay Talegaonkar, *Member, IEEE*, Tejasvi Anand, *Member, IEEE*, Ahmed Elkholy, *Member, IEEE*, Amr Elshazly, *Member, IEEE*, Romesh Kumar Nandwana, *Student Member, IEEE*, Saurabh Saxena, *Member, IEEE*, Brian Young, Woo-Seok Choi, *Member, IEEE*, and Pavan Kumar Hanumolu, *Member, IEEE*

***Abstract*— A highly digital two-stage fractional-*N* phase-locked loop (PLL) architecture utilizing a first-order 1-bit ΔΣ frequency-to-digital converter (FDC) is proposed and implemented in a 65 nm CMOS process. Performance of the first-order 1-bit ΔΣ FDC is improved by using a phase interpolator-based fractional divider that reduces phase quantizer input span and by using a multiplying delay-locked loop that increases its oversampling ratio. We also describe an analogy between a time-to-digital converter (TDC) and a ΔΣ FDC followed by an accumulator that allows us to leverage the TDC-based PLL analysis techniques to study the impact of ΔΣ FDC characteristics on ΔΣ FDC-based fractional-*N* PLL (FDCPLL) performance. Utilizing proposed techniques, a prototype PLL achieves 1 MHz bandwidth, −101.6 dBc/Hz in-band phase noise, and 1.22 ps_{rms} (1 kHz–40 MHz) jitter while generating 5.031 GHz output from 31.25 MHz reference clock input. For the same output frequency, the stand-alone second-stage fractional-*N* FDCPLL achieves 1 MHz bandwidth, −106.1 dBc/Hz in-band phase noise, and 403 fs_{rms} jitter with a 500 MHz reference clock input. The two-stage PLL consumes 10.1 mW power from a 1 V supply, out of which 7.1 mW is consumed by the second-stage FDCPLL.**

***Index Terms*— ΔΣ frequency-to-digital converter (FDC), digital PLL, fractional divider, fractional-*N* PLL, multiplying delay-locked loop (MDLL), phase interpolator (PI).**

I. Introduction

HIGHLY digital architectures for fractional-*N* PLLs have recently gained popularity due to their portability, reconfigurability, and compatibility with manufacturing processes that are optimized for digital circuits. Use of a digital loop filter (DLF) in fractional-*N* PLLs obviates the need for external loop filter components, providing area and cost benefits over their analog counterparts. Additionally, digital PLL architectures are more amenable to quantization noise cancellation [1]. To leverage these benefits, various digital fractional-*N* PLL architectures have been proposed. These can be broadly classified in the following four categories: 1) PLLs with integer ΔΣ dividers and time-to-digital converters (TDCs) [1], [2]; 2) fractional divider-based PLLs utilizing digital-to-time converters (DTCs) [3]–[5]; 3) fractional counter-based PLLs [6], [7]; and 4) ΔΣ frequency-to-digital converter (FDC)-based PLLs [8]–[10]. Most of these implementations of low-noise digital fractional-*N* PLL architectures require a high-resolution TDC or DTC with calibrated gain for effective quantization noise cancellation, which may increase the power consumption or implementation complexity.

In this paper, we present a low-power PLL architecture that achieves low output jitter without using either a high-resolution TDC or DTC and does not utilize any calibration. This is achieved by using a fractional divider-based 1-bit first-order ΔΣ FDC. Use of a phase interpolator (PI) for fractional division improves the performance of the 1-bit phase quantizer (PQ), while the first-order ΔΣ FDC reduces design complexity. We also propose the use of multiplying delay-locked loop (MDLL)-based integer-*N* reference multiplication to exploit the benefits of oversampling in a ΔΣ FDC. The rest of this paper is organized as follows. We discuss the first-order 1-bit ΔΣ FDC in more detail and propose improvements to conventional architecture in Section II. Section III provides the details of the proposed two-stage PLL architecture and its circuit implementation. Measurement results are shown in Section IV. We conclude by summarizing the findings of this paper in Section V.

II. ΔΣ Frequency-to-Digital Converter

A. Background

Principles of oversampling and noise shaping are commonly used in analog-to-digital and digital-to-analog converters. ΔΣ FDCs utilize the same principles to achieve high-resolution

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M. Talegaonkar is with Inphi Corporation, Irvine, CA 92618 USA (e-mail: mrunmayvt@gmail.com).

T. Anand is with the Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97330 USA.

A. Elkholy, W.-S. Choi, and P. K. Hanumolu are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

A. Elshazly is with Intel Corporation, Hillsboro, OR 97124 USA.

R. K. Nandwana is with Cisco Systems, Allentown, PA 18195 USA.

S. Saxena is with the Department of Electrical Engineering, IIT Madras, Chennai, TN 600036 India.

B. Young is with ON Semiconductor, Corvallis, OR 97333 USA.

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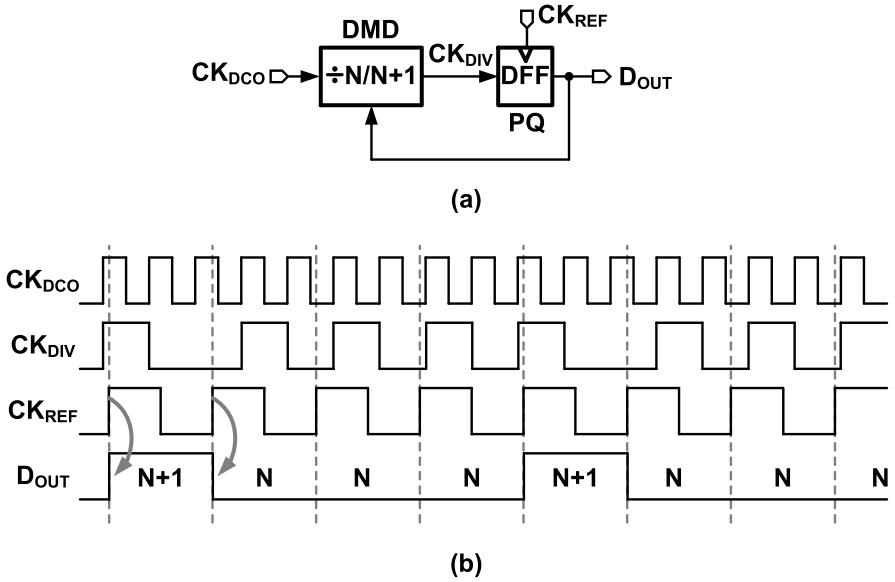


Fig. 1. (a) Block diagram of a basic 1-bit first-order ΔΣ FDC. (b) Illustrative waveforms for $F_{\rm DCO} = 2.25F_{\rm REF}$, $N = 2$.

frequency-to-digital conversion while utilizing a coarse quantizer. Some of the earlier ΔΣ FDC implementations include a ΔΣ FDC with digitally controlled oscillator (DCO) in the feedback [11], a ΔΣ FDC utilizing a divider in the feedback [12], and a ΔΣ FDC implemented using a subtractor with no feedback [13], [14]. Compared with subtractor-based ΔΣ FDC, divider feedback-based ΔΣ FDC has a wide bandwidth feedback loop around PQ that minimizes phase error at the quantizer input [15]. Therefore, divider feedback-based ΔΣ FDC architecture is chosen in this paper. As shown in Fig. 1(a), a basic 1-bit first-order ΔΣ FDC consists of a dual-modulus divider (DMD) controlled by the output of a D flip-flop (DFF) [12]. A high-frequency clock, $\rm CK_{DCO}$, is divided by a factor of N or $N+1$ based on the DFF output, $D_{\rm OUT}$. The output of DMD is used as D input of the flip-flop, while reference clock input ($\rm CK_{REF}$) is used as its sampling clock. In this loop, the DMD acts as a phase integrator and the DFF acts as a 1-bit PQ. Therefore, this loop resembles a first-order 1-bit ΔΣ modulator. Illustrative steady-state waveforms when frequency of $\rm CK_{DCO}$ ($F_{\rm DCO}$) is 2.25 times the frequency of $\rm CK_{REF}$ ($F_{\rm REF}$) and $N = 2$ are shown in Fig. 1(b). When $\rm CK_{REF}$ lags the divider output $\rm CK_{DIV}$, the division ratio is changed to 3; otherwise, it is equal to 2. In steady state, FDC loop operates such that the average phase difference between $\rm CK_{DIV}$ and $\rm CK_{REF}$ is zero. Under this condition, it can be shown that the basic first-order ΔΣ FDC satisfies the following equation [12]:

$$D_{\rm OUT,avg} = \frac{F_{\rm DCO,avg}}{F_{\rm REF,avg}} - (N + 0.5) \tag{1}$$

where $D_{\rm OUT,avg}$ is the average digital output of the ΔΣ FDC.

Fig. 2 shows how a ΔΣ FDC may be used to achieve fractional-N frequency multiplication [9], [10]. The DCO output clock ($\rm CK_{DCO}$) as well as the reference clock ($\rm CK_{REF}$) are fed to ΔΣ FDC. In steady state, output of the ΔΣ FDC equals the fractional frequency difference between

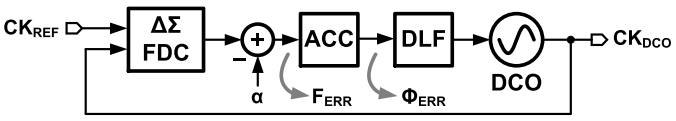


Fig. 2. Simplified block diagram of an FDCPLL.

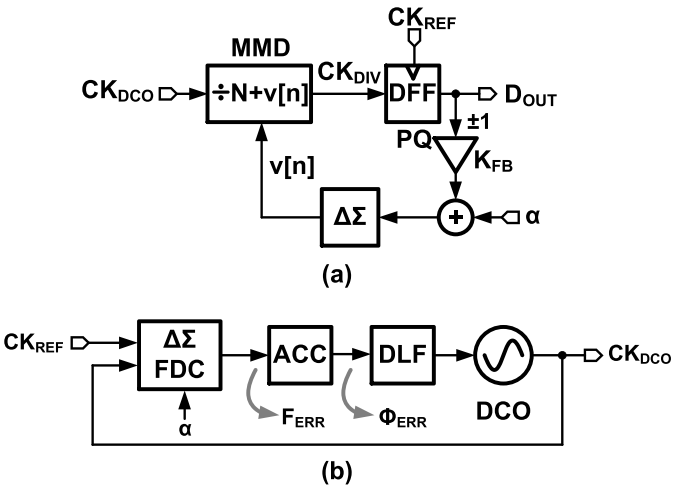


Fig. 3. Simplified block diagrams of (a) zero input ΔΣ FDC with feedback gain scaling [15] and (b) FDCPLL with zero input ΔΣ FDC.

$\rm CK_{DCO}$ and $\rm CK_{REF}$. Frequency error signal, $F_{\rm ERR}$, is obtained by subtracting the expected fractional frequency offset, $\alpha \in (-0.5, 0.5)$ from ΔΣ FDC output. A digital accumulator (ACC) accumulates $F_{\rm ERR}$ to estimate phase error, $\Phi_{\rm ERR}$. A DLF processes the phase error and controls the DCO, such that the following condition is ensured in steady state:

$$F_{\rm DCO,avg} = (N + 0.5 + \alpha)F_{\rm REF,avg}.$$

It should be noted that for ΔΣ FDC shown in Fig. 1(a), feedback gain of the PQ, and consequently, the quantization

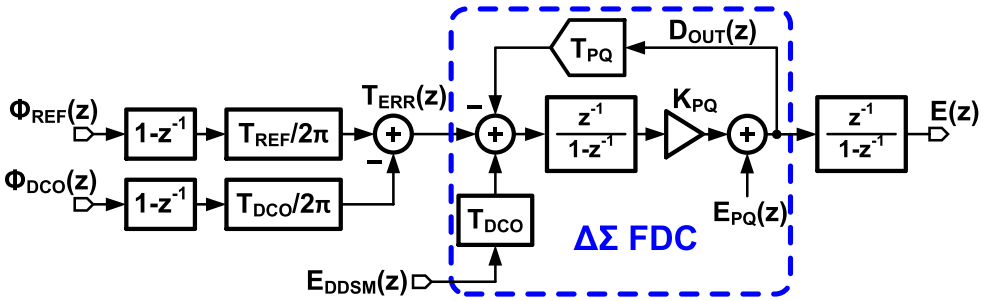


Fig. 4. Detailed small signal model for a cascade of ΔΣ FDC and accumulator.

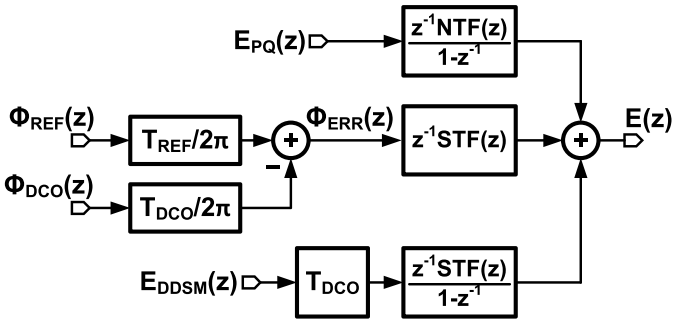


Fig. 5. Simplified small signal model with ΔΣ transfer functions for a cascade of ΔΣ FDC and accumulator.

noise of ΔΣ FDC, depends on the DMD resolution. A modification to ΔΣ FDC, shown in Fig. 3(a), overcomes this limitation [15]. The output of PQ is scaled by a factor, $K_{\mathrm{FB}} < 1$, and added to the fractional frequency control input, α, of a digital ΔΣ modulator (ΔΣ) that generates the multi-modulus divider (MMD) modulus, $v[n]$. As before, the MMD, acting as a phase integrator, in conjunction with the PQ makes this loop similar to a ΔΣ modulator. Furthermore, based on the PQ output, the digital ΔΣ modulator changes the average division ratio by a fractional value, K_{FB} rather than an integer value as in the case of ΔΣ FDC shown in Fig. 1(a). Consequently, it can be shown that the steady-state output of such ΔΣ FDC is

$$D_{\mathrm{OUT,avg}} = \frac{F_{\mathrm{DCO,avg}} - (N+\alpha)F_{\mathrm{REF,avg}}}{K_{\mathrm{FB}}F_{\mathrm{REF,avg}}}. \tag{2}$$

It is important to note that the use of digital ΔΣ modulator and MMD enables use of $K_{\mathrm{FB}} < 2^{-1}$, which improves the quantization noise performance of ΔΣ FDC by reducing the effective feedback gain. When used in an FDC-based fractional-N PLL (FDCPLL), as shown in Fig. 3(b), the input to ΔΣ FDC is zero in steady state. Therefore, we refer to this ΔΣ FDC architecture as "zero input" ΔΣ FDC. We note that the first-order ΔΣ FDC can also be thought of as a phase domain Δ modulator [15] to arrive at the same conclusions. As we will show later, the performance of a 1-bit "zero input" ΔΣ FDC architecture can be improved significantly by using a PI-based fractional divider. To understand the impact of ΔΣ FDC on FDCPLL performance and the need for PI-based fractional divider, we delve into transfer function analysis of "zero input" ΔΣ FDC in Section II-B.

B. TDC Analogy for ΔΣ FDC

It is useful to observe that the cascade of ΔΣ FDC and digital accumulator is analogous to a high-resolution TDC. Therefore, by deriving equivalent TDC characteristics, we can utilize well-known TDC-based PLL analysis techniques to predict the impact of ΔΣ FDC characteristics on FDCPLL performance.

A detailed small signal model of the ΔΣ FDC along with an accumulator at its output is shown in Fig. 4. The quantization error added by the digital ΔΣ modulator is denoted as $E_{\mathrm{DDSM}}(z)$, while $E_{\mathrm{PQ}}(z)$ denotes the quantization error of PQ. The linearized gain of the 1-bit PQ is denoted as K_{PQ}, and the equivalent feedback DAC gain is denoted as T_{PQ}. We denote signal transfer function (STF) of the ΔΣ FDC as STF(z) and phase quantization noise transfer function (NTF) as NTF(z). Therefore

$$\mathrm{STF}(z) \triangleq \frac{D_{\mathrm{OUT}}(z)}{T_{\mathrm{ERR}}(z)}$$

$$\mathrm{NTF}(z) \triangleq \frac{D_{\mathrm{OUT}}(z)}{E_{\mathrm{PQ}}(z)}.$$

A simplified small signal model using the above-mentioned transfer functions is shown in Fig. 5. Contributions of reference phase noise, DCO phase noise as well as digital ΔΣ, and phase quantization error to the digital phase error output can be found if STF and NTF of the ΔΣ FDC are known.

A simplified small signal equivalent model shown in Fig. 6(a) can be used to calculate STF and NTF of the ΔΣ FDC. PQ is modeled as a constant gain block with gain K_{PQ}. Equivalent gain of the feedback DAC, T_{PQ}, is equal to $K_{\mathrm{FB}}T_{\mathrm{DCO}}$. Assuming that there is no overloading of the ΔΣ FDC and that phase quantization noise power spectral density is white, STF is given by

$$\mathrm{STF}(z) = \frac{K_{\mathrm{PQ}}z^{-1}}{1-(1-K_{\mathrm{PQ}}T_{\mathrm{PQ}})z^{-1}}. \tag{3}$$

Note that the dc gain of STF does not depend on the linearized PQ gain, K_{PQ}. In contrast to bang–bang fractional-N PLLs [3], this property of ΔΣ FDC obviates the need for dc gain calibration despite using a 1-bit PQ [15].

NTF of the ΔΣ FDC can be shown to be

$$\mathrm{NTF}(z) = \frac{1-z^{-1}}{1-(1-K_{\mathrm{PQ}}T_{\mathrm{PQ}})z^{-1}}. \tag{4}$$

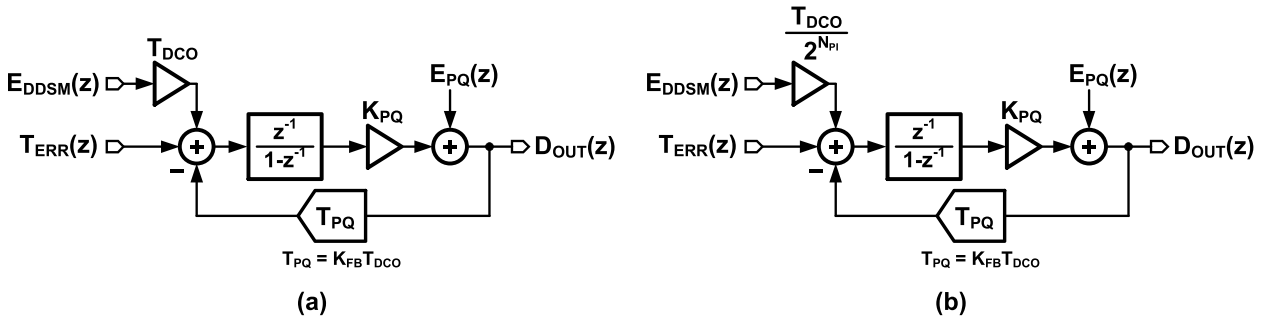


Fig. 6. Simplified small signal equivalent block diagrams for (a) zero input ΔΣ FDC with feedback gain scaling [15] and (b) proposed PI-based ΔΣ FDC.

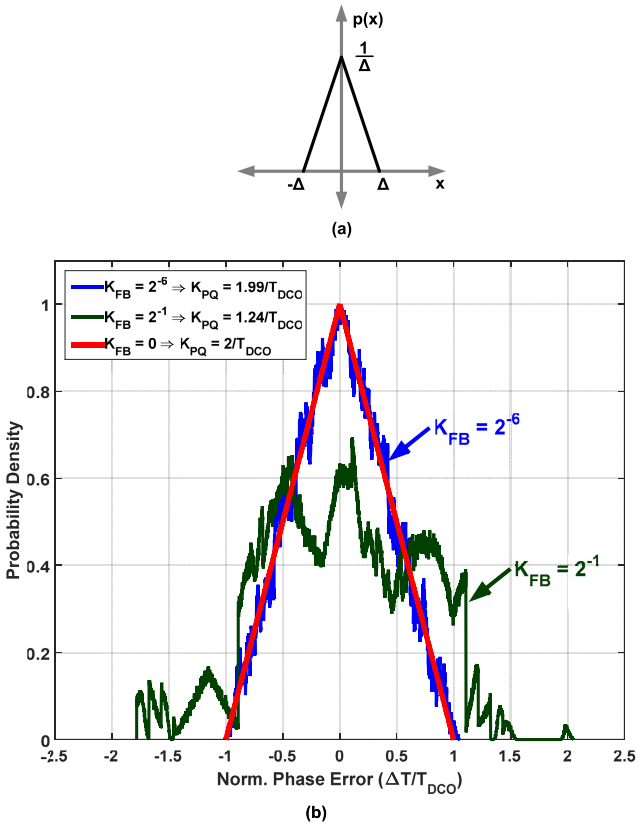


Fig. 7. (a) Probability density function (pdf) of the running sum of a second-order digital ΔΣ modulator output quantizer error with quantization step size of Δ and (b) pdf of simulated PQ input phase error for ΔΣ FDC with and without feedback.

It can also be shown that for low frequencies, quantization noise power spectral density referred to $\Phi_{\mathrm{ERR}}(z)$ input, $E_{Q,\mathrm{In}}(z)$, is given by

$$E_{Q,\mathrm{In}}(z) \approx \frac{E_{\mathrm{PQ}}(z)}{K_{\mathrm{PQ}}} \quad \mathrm{sec}^2/\mathrm{Hz}. \tag{5}$$

Clearly, a larger K_{PQ} results in lower input referred quantization noise.

It is interesting to note that while the dc gain of the STF does not depend on PQ gain, both STF bandwidth as well as low-frequency NTF gain depend on it. The effective linear gain of the 1-bit PQ can be calculated using the following equation [16]:

$$K_{\mathrm{PQ}} = \frac{E\{\mathrm{sgn}(\Delta t)\Delta t\}}{E\{\Delta t^2\}} \tag{6}$$

where $\Delta t[n]$ is the phase error at the input of PQ. In the steady state, the phase error caused by digital ΔΣ modulator at the PQ input is given by [17]

$$\Delta t[n] = \Delta \sum_{k=0}^{n} e[k]$$

where Δ is the quantization step size of the digital ΔΣ modulator and $e[n]$ is the quantization error at its output. Therefore, for small values of K_{FB}, probability density function (pdf) of Δt is the same as pdf of the running sum of the quantization error at the output of second-order digital ΔΣ modulator with constant input. In the cases where the quantization error of digital ΔΣ modulator behaves as a uniformly distributed random variable with white spectrum, the pdf of running sum of quantization error at the output of a second-order digital ΔΣ modulator with a step size of Δ is a triangular pdf, as shown in Fig. 7(a). Using this pdf, K_{PQ} is calculated to be $2/\Delta$. Note that this sets the upper bound on the value of K_{PQ}. In practice, various non-idealities and additional sources of jitter result in a lower K_{PQ}.

Fig. 7(b) shows the simulated pdf of the PQ input for $K_{\mathrm{FB}} = 2^{-6}$ and $K_{\mathrm{FB}} = 2^{-1}$ overlaid on the pdf of running sum of digital ΔΣ modulator with quantization step size, $\Delta = T_{\mathrm{DCO}}$ (equivalent to $K_{\mathrm{FB}} = 0$). It can be seen that large K_{FB} increases PQ input span, which decreases K_{PQ}. Clearly, to maximize K_{PQ}, K_{FB} must be reduced. However, there are two issues with reducing K_{FB} below a certain limit. First, because full-scale range of the ΔΣ FDC is $2T_{\mathrm{PQ}} = 2K_{\mathrm{FB}}T_{\mathrm{DCO}}$, a smaller value of K_{FB} reduces full-scale range, which may result in increased in-band phase noise due to overloading. Second, STF bandwidth reduces with reduction in K_{FB}, which is undesirable as it limits the bandwidth of the FDCPLL. To understand this, consider the continuous time approximation of STF, given by

$$\mathrm{STF}(s) \approx \frac{1}{T_{\mathrm{PQ}}\left(1 + \frac{sT_{\mathrm{REF}}}{K_{\mathrm{PQ}}T_{\mathrm{PQ}}}\right)}. \tag{7}$$

The expression for its −3 dB bandwidth, $\omega_{\text{-3 dB}}$, is given by

$$\omega_{\text{-3 dB}} = \frac{K_{\mathrm{PQ}}T_{\mathrm{PQ}}}{T_{\mathrm{REF}}} = \frac{K_{\mathrm{PQ}}K_{\mathrm{FB}}T_{\mathrm{DCO}}}{T_{\mathrm{REF}}} \tag{8}$$

which scales in proportion to K_{FB}. Fig. 8(a) shows the simulated and estimated input-to-output transfer functions for various values of K_{FB}, which confirm our analysis. Note that (6) and phase error statistics obtained from behavioral

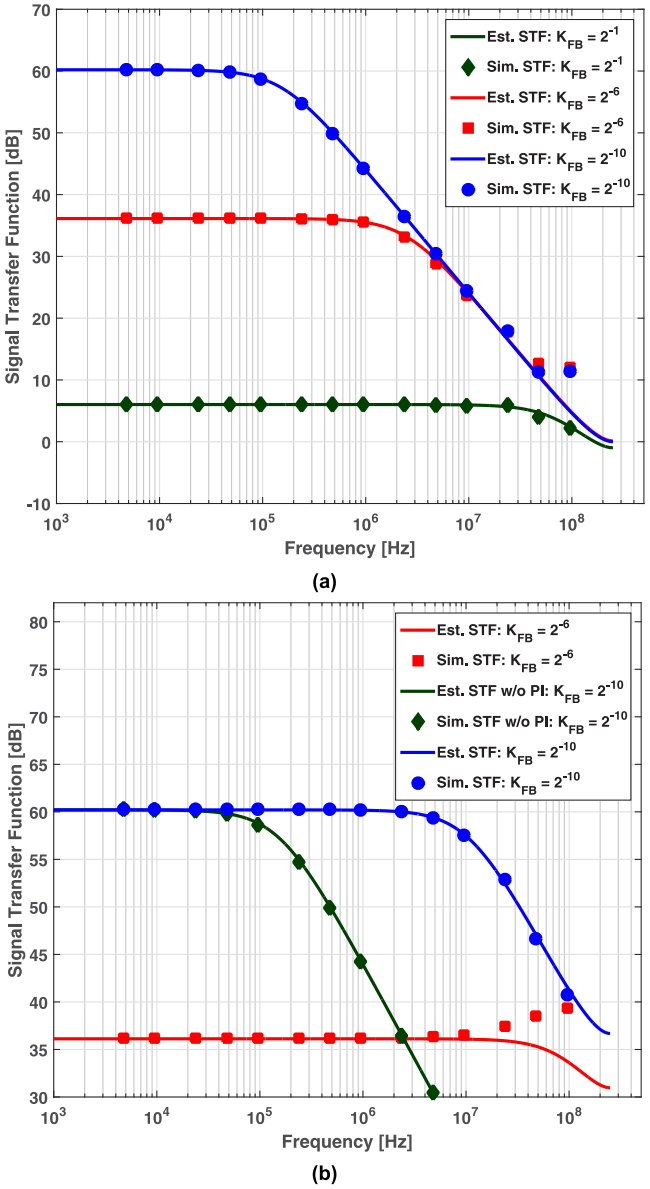


Fig. 8. Simulated and estimated FDC input-to-output STF for various values of K_{FB} for (a) $\Delta\Sigma$ FDC with feedback gain scaling and (b) proposed PI-based $\Delta\Sigma$ FDC.

simulations are used to arrive at K_{PQ} values for estimating transfer functions in Fig. 8(a) as well as all the subsequent estimated transfer function plots. It is also seen that for low K_{FB}, the PQ gain mostly depends on $\Delta\Sigma$ quantization step size. When used in conjunction with an integer MMD, the quantization step size of digital $\Delta\Sigma$ modulator is as large as T_{DCO}, which limits the maximum value of K_{PQ} to $2/T_{DCO}$.

To be able to use the first-order 1-bit $\Delta\Sigma$ FDC in a wide bandwidth fractional-N PLL, a large F_{REF} and and a large K_{PQ} are needed [see (8)]. Discussion in this section indicates that it is necessary to reduce the input span of the PQ to increase K_{PQ}. To this end, we propose a fractional divider-based first-order 1-bit $\Delta\Sigma$ FDC that utilizes a PI for fractional division [18].

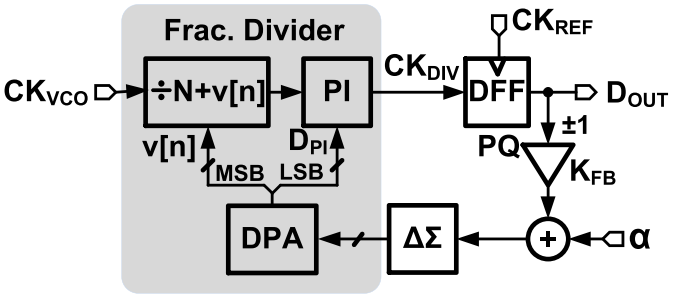


Fig. 9. Simplified block diagram of the proposed fractional divider-based $\Delta\Sigma$ FDC.

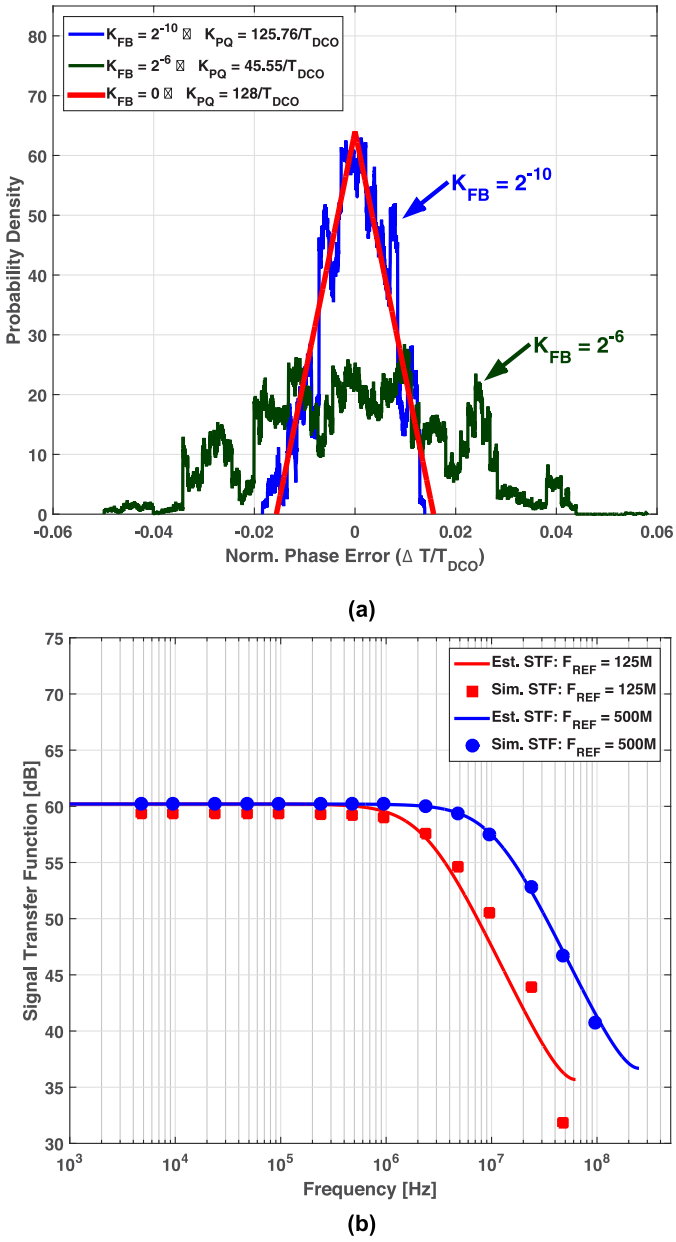


Fig. 10. (a) Probability density function (pdf) of simulated PQ input phase error for PI-based $\Delta\Sigma$ FDC. (b) Simulated and estimated FDC STF for various values of F_{REF} for a PI-based $\Delta\Sigma$ FDC.

C. Proposed PI-Based $\Delta\Sigma$ FDC

Reduction of PQ input span using a high resolution fractional divider in the context of bang–bang fractional-N PLLs was demonstrated in [3] and [4]. We employ similar technique

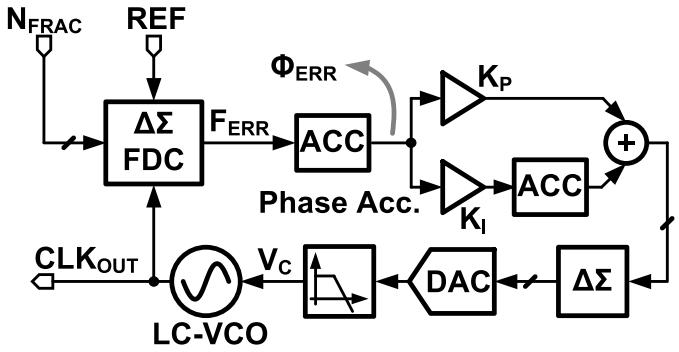


Fig. 11. Block diagram of the proposed FDCPLL.

in ΔΣ FDC, with a PI-based fractional divider chosen over a DTC-based fractional divider as it does not require gain calibration. An $N_{\rm PI}$ bit PI can cancel the residual quantization error of an MMD, resulting in fractional division with $N_{\rm PI}$ bit resolution. Consequently, the input span of the PQ is limited to $T_{\rm DCO}/2^{N_{\rm PI}-1}$ [3]. A simplified block diagram of the proposed ΔΣ FDC is shown in Fig. 9. The digital ΔΣ modulator output is accumulated using a digital phase accumulator (DPA). The integer part of the DPA output controls an MMD, while the fractional part is used to control the PI to cancel the MMD quantization error. Fig. 6(b) shows a small signal equivalent block diagram of the proposed PI-based ΔΣ FDC. It is the same as that of a feedback gain-scaled FDC except for one crucial difference. The quantization step size of the digital ΔΣ modulator is reduced from $T_{\rm DCO}$ to $T_{\rm DCO}/2^{N_{\rm PI}}$. Note that the fractional divider contributes no additional quantization error if the digital ΔΣ modulator output resolution is the same as PI resolution. A pdf based on simulated histogram of the PQ input phase error for a 6-bit PI-based ΔΣ FDC, shown in Fig. 10(a), indicates that the input span of the PQ is reduced by a factor of 64. Therefore, the effective linear gain of the PQ, $K_{\rm PQ}$, increases to

$$K_{\rm PQ} \approx \frac{2^{N_{\rm PI}+1}}{T_{\rm DCO}} \tag{9}$$

in case of an $N_{\rm PI}$ bit PI-based FDC when $K_{\rm FB}$ is small. Simulations indicate that $K_{\rm PQ}$ changes from $45/T_{\rm DCO}$ to $126/T_{\rm DCO}$ when $K_{\rm FB}$ is reduced from 2^{-6} to 2^{-10}. The plot of estimated and simulated input-to-output STF is shown in Fig. 8(b). The increase in STF bandwidth with the use of a PI-based fractional divider is evident from this plot.

Equation (8) also indicates that the STF bandwidth can be increased by increasing ΔΣ FDC reference input frequency, $F_{\rm REF}$. Large $F_{\rm REF}$ has an added benefit of reducing in-band power spectral densities of both digital ΔΣ modulator quantization noise as well as PQ quantization noise. In view of these benefits, we present a two-stage PLL architecture where a first-stage integer-*N* clock multiplier is used to increase the reference frequency input of a second-stage fractional-*N* FDCPLL. The details of the PLL architecture and its circuit implementation are provided in Section III.

III. PLL Architecture and Implementation

A. Proposed PLL Architecture

Fig. 11 shows the block diagram of a fractional-*N* PLL utilizing the proposed ΔΣ FDC. The output of ΔΣ FDC, $F_{\rm ERR}$, is accumulated to produce the phase error, $\Phi_{\rm ERR}$. A conventional proportional-integral type DLF generates a digital control word for the DCO. A ΔΣ modulator-based DAC followed by a low-pass filter (LPF) is used to generate the control voltage V_C for an LC voltage-controlled oscillator (*LC*-VCO). A type II loop is chosen, as it offers superior suppression of the VCO flicker noise. Fig. 12 shows the simplified small signal equivalent block diagram of the proposed FDCPLL. The small signal model derived for cascade of ΔΣ FDC and digital accumulator in Section II-B is used to simplify the analysis of the FDCPLL. The digital phase error signal $E(z)$ is filtered with DLF transfer function $H(z)$ and used to control frequency of the DCO with a gain of $K_{\rm DCO}$ Hz/LSB. Frequency quantization error of the DCO is denoted as $E_{\rm Q,DCO}(z)$, while the DCO phase noise is denoted as $\Phi_{\rm N,DCO}(z)$. $\Phi_{\rm DCO}(z)$ and $\Phi_{\rm REF}(z)$, respectively, denote the output and input of the FDCPLL. The loop gain of the FDCPLL is given by

$$\begin{aligned} {\rm LG}(z) &= \frac{T_{\rm REF}^2 K_{\rm DCO}}{N_{\rm nom}} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot {\rm STF}(z) \cdot H(z) \qquad (10)\\ &\approx \frac{T_{\rm REF}^2 K_{\rm DCO}}{N_{\rm nom}} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot \frac{K_{\rm PQ} z^{-1}}{1-(1-K_{\rm PQ}T_{\rm PQ})z^{-1}} \\ &\quad \cdot \left(K_P + \frac{K_I z^{-1}}{1-z^{-1}}\right) \qquad (11) \end{aligned}$$

where we have assumed $H(z)$ is a conventional proportional-integral type DLF. We have also ignored any other parasitic poles present in the loop. To simplify the analysis, consider the continuous time approximation, LG(s), of LG(z). It can be shown that

$${\rm LG}(s) = \frac{K_{\rm DCO}K_I}{T_{\rm REF}K_{\rm FB}} \cdot \frac{\left(1+\frac{sT_{\rm REF}K_P}{K_I}\right)}{s^2\left(1+\frac{sT_{\rm REF}}{K_{\rm PQ}K_{\rm FB}T_{\rm DCO}}\right)}. \tag{12}$$

An approximate expression for unity gain frequency, ω_u, is given by

$$\omega_u = \frac{K_{\rm DCO}K_P}{K_{\rm FB}}. \tag{13}$$

To ensure good phase margin, $\omega_u << \omega_{\text{-3 dB}}$, where $\omega_{\text{-3 dB}}$ is the pole introduced by STF of cascade of ΔΣ FDC and an accumulator, and is given by (8). As mentioned in Section II-B, a higher reference frequency improves PLL stability by increasing $\omega_{\text{-3 dB}}$.

For noise analysis, we follow the parameterization method described in [19]. We define closed loop parameterization function, $G(z)$, as

$$G(z) = \frac{{\rm LG}(z)}{1+{\rm LG}(z)}. \tag{14}$$

Let the power spectral densities of digital ΔΣ quantization noise, ΔΣ FDC quantization noise, DCO quantization noise, DCO phase noise, and reference phase noise be denoted as $S_{Q,\rm DDSM}(z)$, $S_{\rm PQ}(z)$, $S_{Q,\rm DCO}(z)$, $S_{N,\rm DCO}(z)$, and $S_{N,\rm REF}(z)$,

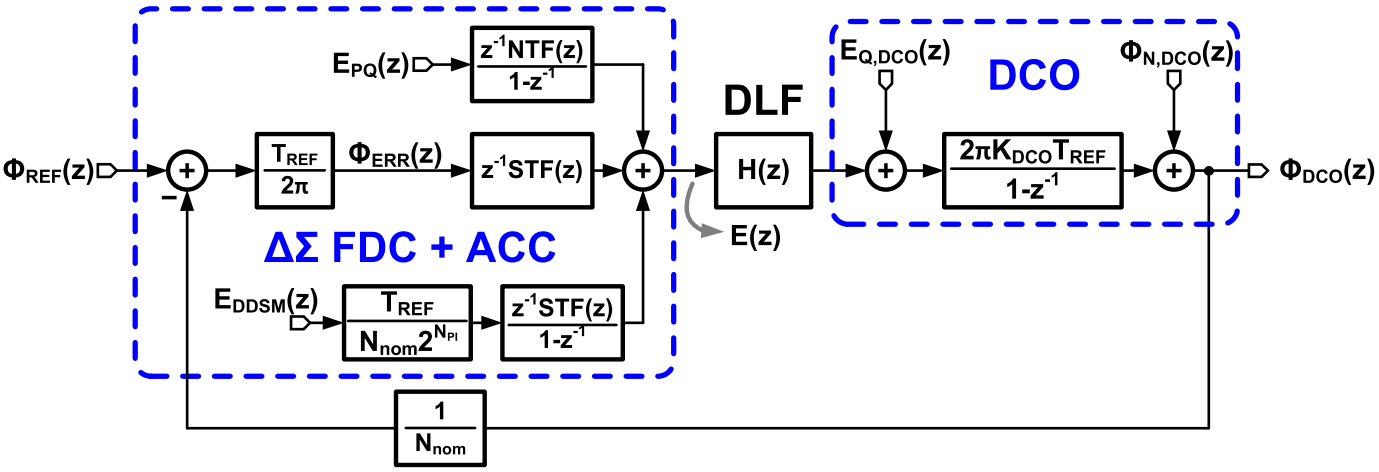


Fig. 12. Simplified small signal equivalent block diagram of the proposed FDCPLL.

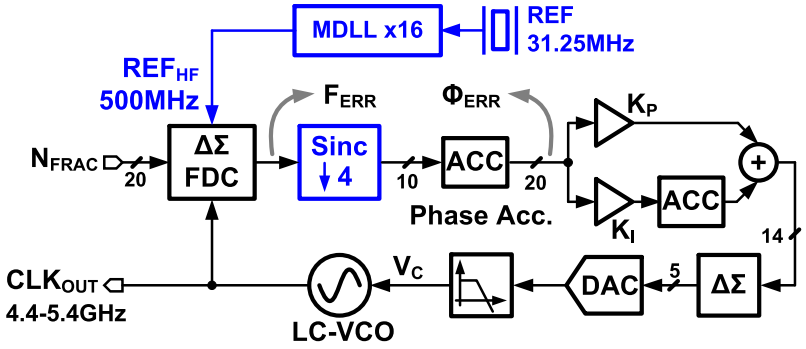


Fig. 13. Block diagram of the proposed two-stage PLL.

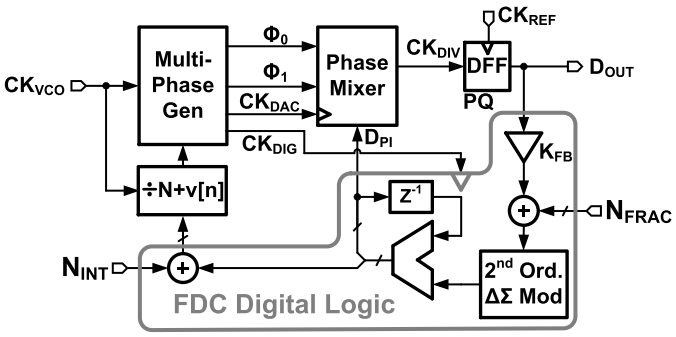


Fig. 14. Block diagram of the proposed PI-based ΔΣ FDC implementation.

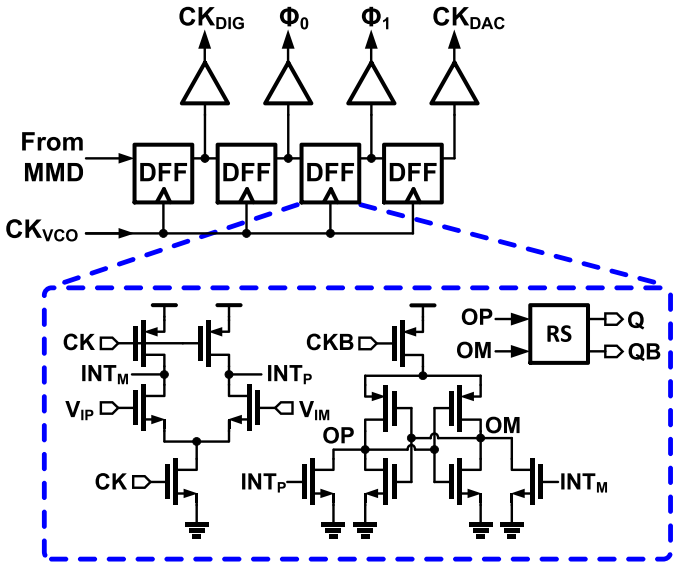


Fig. 15. Block diagram of shift register-based multi-phase generator (MPG).

respectively. The overall output noise power spectral density is given by

$$S_{N,\mathrm{DCO}}(z) = \left|\frac{2\pi}{2^{N_{\mathrm{PI}}}}\cdot G(z)\right|^2 S_{Q,\mathrm{DDSM}}(z) + \left|\frac{2\pi}{T_{\mathrm{REF}}}\cdot\frac{\mathrm{NTF}(z)}{(1-z^{-1})\mathrm{STF}(z)}\cdot N_{\mathrm{nom}}\cdot G(z)\right|^2 S_{\mathrm{PQ}}(z) + \left|\frac{2\pi K_{\mathrm{DCO}}T_{\mathrm{REF}}}{1-z^{-1}}\cdot(1-G(z))\right|^2 S_{Q,\mathrm{DCO}}(z) + |(1-G(z))|^2 S_{N,\mathrm{DCO}}(z) + |N_{\mathrm{nom}}\cdot G(z)|^2 S_{N,\mathrm{REF}}(z). \quad (15)$$

The in-band phase noise of this PLL is limited by the ΔΣ FDC quantization error, $E_{\mathrm{PQ}}(z)$. As explained previously, a larger reference frequency input to FDCPLL results in both wideband operation as well as lower quantization noise. Larger reference frequency also pushes the quantization noise of the digital ΔΣ modulator present in ΔΣ FDC to higher frequencies [20]. The effect of using a larger input reference frequency on ΔΣ FDC STF is shown in Fig. 10(b). Behavioral simulations confirm that a higher reference frequency improves STF bandwidth of the ΔΣ FDC. To take advantage of the improved

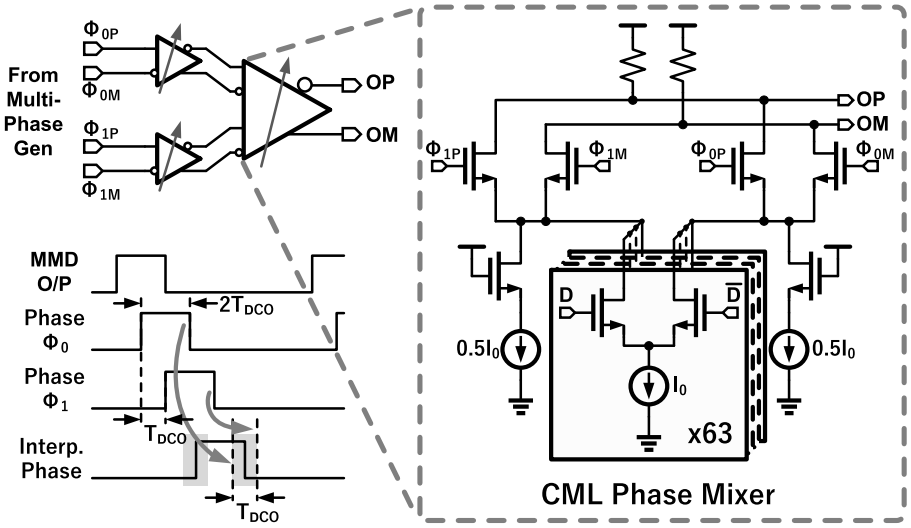


Fig. 16. Block diagram of the phase mixer.

performance of the ΔΣ FDC-based PLL with higher input reference frequency, we propose the use of a two-stage PLL architecture shown in Fig. 13. The first-stage digital MDLL generates a 500 MHz high-frequency reference (REF_{HF}) from a 31.25 MHz external crystal oscillator. The choice of MDLL is influenced by its excellent low-frequency phase noise performance due to reference injection mechanism [21]. REF_{HF} is used as a reference input for the proposed PI-based ΔΣ FDC in the second-stage FDCPLL. The output of ΔΣ FDC is decimated by a factor of 4 to obtain 10-bit frequency error (F_{ERR}), which is accumulated to generate the phase error word (Φ_{ERR}). While the first-stage MDLL improves the performance of FDCPLL by increasing its reference frequency, it also adds phase noise. Therefore, careful design of the MDLL is necessary for achieving good overall performance. It is worth mentioning that the MDLL can be shared among multiple on-chip fractional-*N* PLLs, thus amortizing its power consumption. The increase in power consumption of the ΔΣ FDC digital blocks due to higher reference frequency will not be significant in highly scaled CMOS processes. In Section III-B, we describe the implementation of important circuits blocks in the proposed PLL.

B. Circuit Implementation

A simplified block diagram of the proposed PI-based ΔΣ FDC implementation is shown in Fig. 14. The PI is implemented using a multi-phase generator (MPG) followed by a current-mode logic-based (CML) phase mixer [22]. As an *LC*-VCO is used in the second-stage FDCPLL, generation of quadrature phases for a PI placed before the MMD would have required I/Q phase dividers resulting in twice the quantization step size. On the other hand, the choice of placing PI after the divider avoids the need for quadrature phases. It also obviates the need for extra logic that would, otherwise, be needed for large phase shifts [4] and relaxes timing constraints for the PI control circuitry, albeit at the cost of worse linearity. A DFF implemented using double-tail latch type sense amplifier circuit [23] acts as 1-bit PQ. The output of the PQ is scaled and added to 20-bit fractional frequency control word N_{FRAC}.

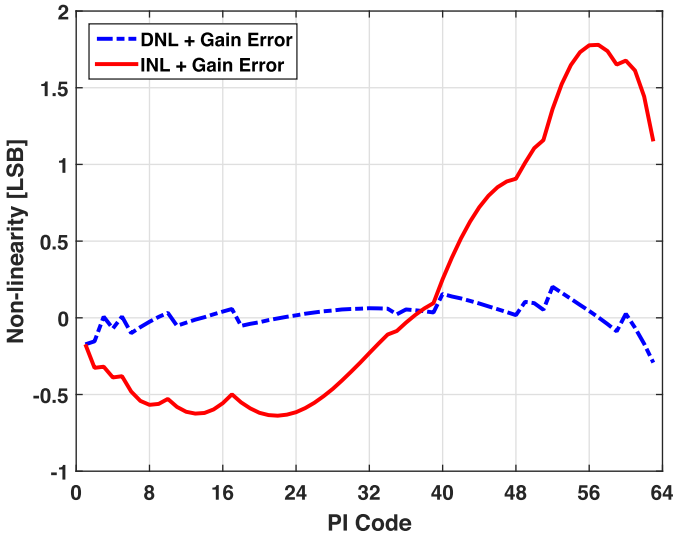


Fig. 17. Simulated phase mixer non-linearity under typical conditions at 5 GHz.

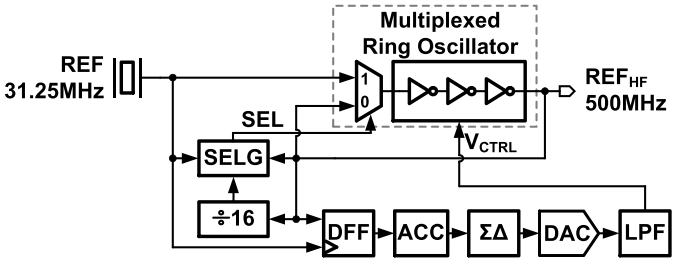
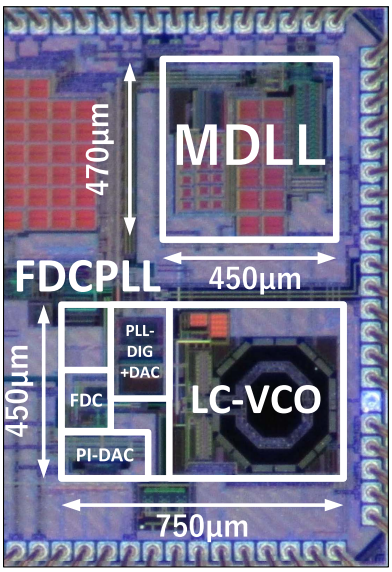


Fig. 18. Block diagram of the digital MDLL.

A second-order digital ΔΣ modulator quantizes this input to generate a 6-bit output. An accumulator used as DPA generates control words for 6-bit phase mixer as well as multi-modulus integer divider. Integer division control word, N_{INT}, is added to DPA output before feeding it to the MMD. It should be noted that this implementation introduces feedback loop delay of around four reference cycles. The impact of this loop delay is found to be negligible from behavioral simulations.



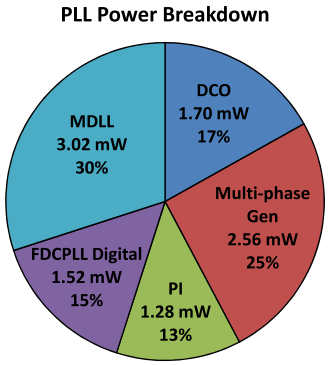


Fig. 19. Die micrograph and detailed power breakdown of the two-stage PLL.

The simplified block diagram of the MPG is shown in Fig. 15. A shift register generates coarse clock phases (Φ_0, Φ_1) that are subsequently used in the phase mixer for interpolation. In addition, clocks for synthesized digital logic (CK_{DIG}) and phase mixer DAC (CK_{DAC}) are also generated by the MPG. To generate these signals, output of the MMD is sampled by using DFFs that are clocked by high-frequency clock output from DCO. As a result, outputs of the shift register DFFs are ideally spaced apart by DCO period, T_{DCO}. In practice, clock-to-Q delays of DFFs also influence the phase spacing. Maintaining the phase spacing between Φ_0 and Φ_1 is important, as these phases are used by the phase mixer for fine phase interpolation. Any spacing error between these phases contributes to gain error in the PI characteristic. To minimize the spacing error, clock-to-Q delay mismatch of these flip-flops is minimized by matching their input as well as output parasitic capacitance loading. Furthermore, extra DFFs inserted at the beginning and at the end of the shift register ensure better matching between Φ_0 and Φ_1 waveforms at the cost of extra power. The outputs of these extra DFFs are used for clocking the digital logic as well as phase mixer DAC. Note that the phase spacing is not critical for these clock signals.

The phase mixer schematic is shown in Fig. 16. As described before, phases Φ_0 and Φ_1, which are T_{DCO} apart,

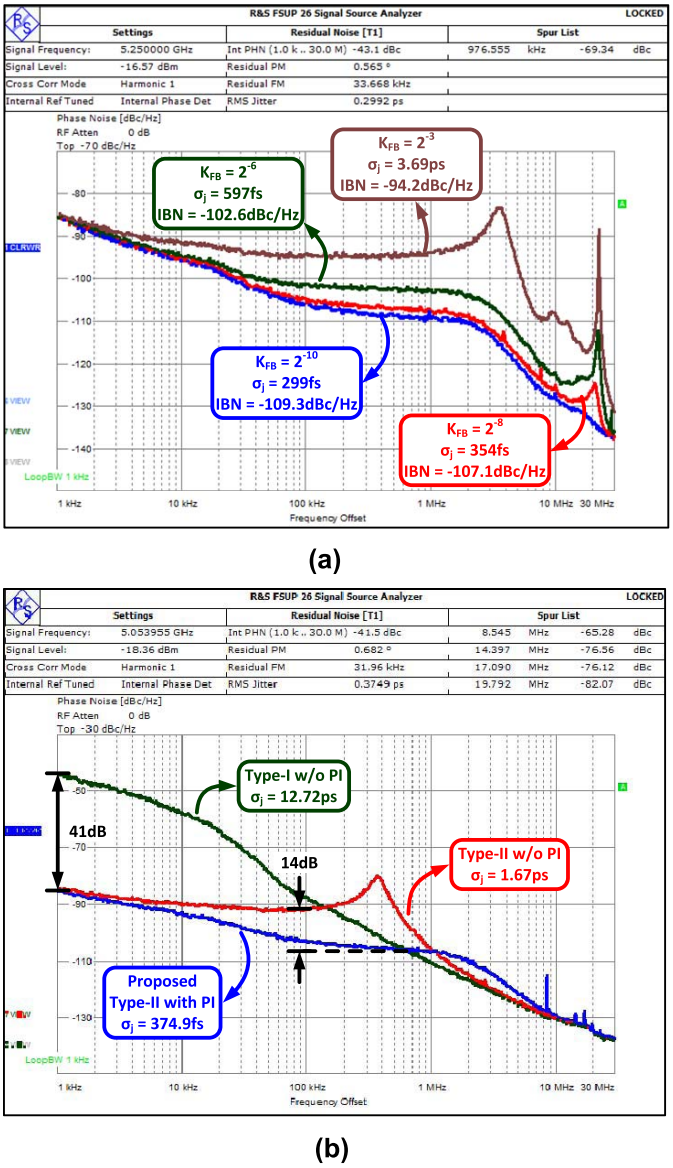


Fig. 20. (a) Measured output phase noise, integrated jitter (σ_j), and in-band phase noise floor for various K_{FB} values when proposed FDCPLL operates at an output frequency of 5.25 GHz. (b) Measured output phase noise for various FDCPLL configurations for an output frequency of 5.053955 GHz.

are generated by the MPG. As the MMD output waveform has a pulsewidth of $2T_{DCO}$, the waveforms for Φ_0 and Φ_1 inherit this pulsewidth. These pulses, spaced by T_{DCO}, are passed through slew rate control buffers to a CML phase mixer. The mixer performs phase interpolation between Φ_0 and Φ_1 according to the 6-bit control word D_{PI}. A 63-element thermometer-coded current steering DAC is used to control the interpolation weight in a monotonic fashion. PI linearity greatly impacts the spur performance of the FDCPLL. Therefore, interpolation linearity is improved by pre-distorting the DAC unit elements and controlling the rise/fall times of Φ_0 and Φ_1 [24]. We note that the pre-distortion of DAC unit elements is carried out during the design process, and no calibration is performed post-fabrication. As the duty cycle of MMD output is not equal to 50%, use of positive or negative edges of Φ_0 and Φ_1 waveforms for interpolation shows

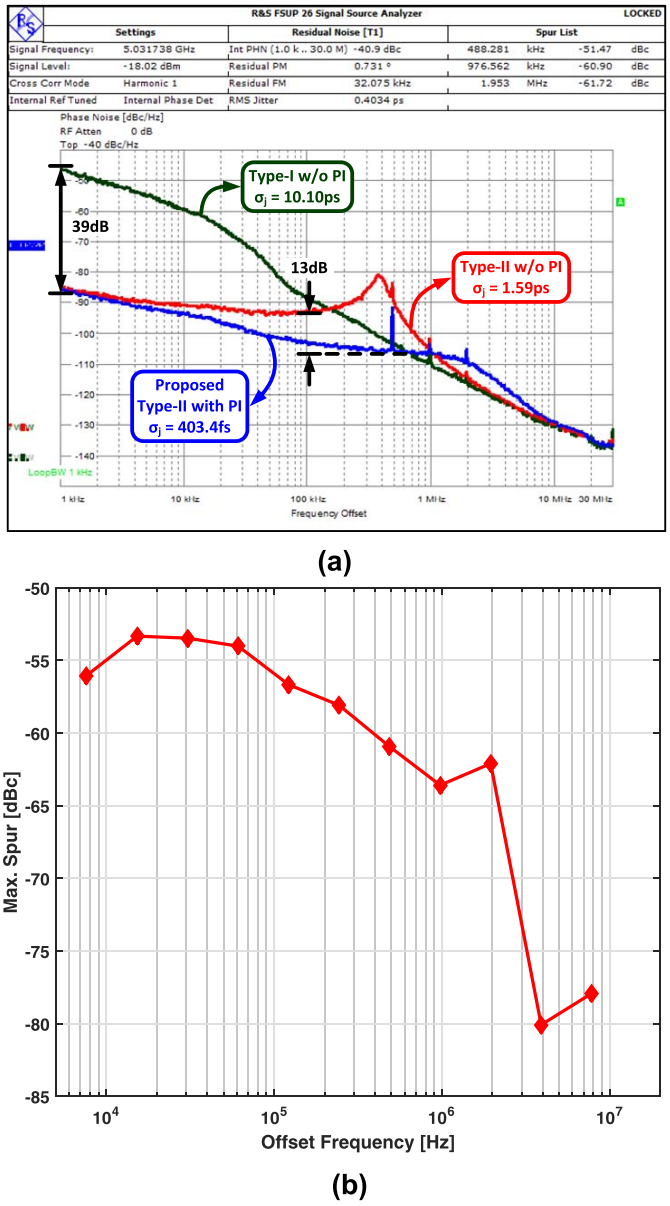


Fig. 21. (a) Measured output phase noise for various FDCPLL configurations for an output frequency of 5.031738 GHz. (b) Measured maximum output spur for fractional frequencies offset from 5.03125 GHz.

significantly different linearity performance. Use of negative edges results in clock waveforms that are similar to those of 50% duty cycle quadrature clocks near interpolation edge and, therefore, shows better phase linearity. Additionally, two fixed half LSB current sources in the phase mixer DAC ensure that current is never zero in both the CML mixer branches, which improves mixer phase settling time [24]. Fig. 17 shows the simulated typical non-linear characteristics including gain error of the phase mixer.

The block diagram of the first-stage digital MDLL is shown in Fig. 18 [25]. The MDLL utilizes a highly digital architecture. The reference edge is injected into the multiplexed ring oscillator using a select logic block, denoted as SELG in Fig. 18, and a divider. Low output frequency of the MDLL eases the design of the edge injection circuitry. A DFF acts as a 1-bit PQ to detect the phase difference between the reference input and MDLL output. A digital accumulator followed by a ΔΣ modulator-based DAC and LPF generates the control voltage for the multiplexed ring oscillator. The edge injection mechanism of the MDLL achieves low jitter by suppressing jitter accumulation in the multiplexed ring oscillator.

For the FDCPLL, DCO is implemented using hybrid approach as described in [5]. The phase accumulator, decimation filter, and digital proportional–integral loop filter are implemented using automatic synthesis and place/route tools. In Section IV, we provide prototype chip measurements that demonstrate the efficacy of the architecture and implementation techniques described so far.

IV. Measurement Results

The die micrograph of the proposed two-stage PLL is shown in Fig. 19. The prototype chip is fabricated in a 65 nm CMOS process. It operates with a supply voltage of 1 V. The first-stage MDLL and the second-stage FDCPLL occupy an active area of 0.22 and 0.32 mm^2, respectively. The total power consumption when generating 5.053955 GHz output from a 31.25 MHz reference input is 10.1 mW, out of which the MDLL consumes 3 mW. The detailed breakdown of two-stage PLL power consumption is shown in Fig. 19.

We first describe the second-stage FDCPLL measurements using an external 500-MHz reference clock. The impact of varying the ΔΣ feedback gain, K_{FB}, on FDCPLL performance at 5.25-GHz output frequency is shown in Fig. 20(a). At this frequency, the digital ΔΣ modulator input is zero in the present implementation. This is similar to measuring the performance of a TDC-based PLL for integer multiplication factor. We observe that for large K_{FB} values, the FDCPLL loop phase margin is low, resulting in peaking and limit cycles. This is attributed to reduced K_{PQ} and lower STF bandwidth for ΔΣ FDC. As K_{FB} is reduced, K_{PQ} as well as STF bandwidth increase. This results in improved phase margin as well as lower input referred quantization noise of the ΔΣ FDC. Consequently, integrated jitter reduces from 3.69 ps_{rms} to 299 fs_{rms}, and in-band phase noise at 600-kHz offset reduces from −94.2 to −109.3 dBc/Hz, as K_{FB} is reduced from 2^{-3} to 2^{-10}. It is also interesting to note that for sufficiently low K_{FB} values, FDCPLL bandwidth remains almost constant and is independent of jitter. However, FDCPLL bandwidth is still sensitive to the DCO gain variation, as is the case with conventional PLLs.

Fig. 20(b) shows the PLL output phase noise spectra with different configurations at an output frequency of 5.053955 GHz when the fractional spur is out-of-band. These configurations include a type I PLL with a gain-scaled ΔΣ FDC without PI, a type II PLL with a gain-scaled ΔΣ FDC without PI, and a type II PLL with the proposed PI-based ΔΣ FDC. The benefits of the type II loop are evident at low frequencies, as the PLLs using type II loop offer 41-dB higher suppression of the DCO flicker noise at 1 kHz. Furthermore, the large PQ non-linearity present in type II PLL with gain-scaled ΔΣ FDC without PI appears at the output in the form of increased in-band phase noise and peaking. For exactly the same loop parameters, the proposed PI-based ΔΣ FDC results in 14 dB better noise floor as well as wider

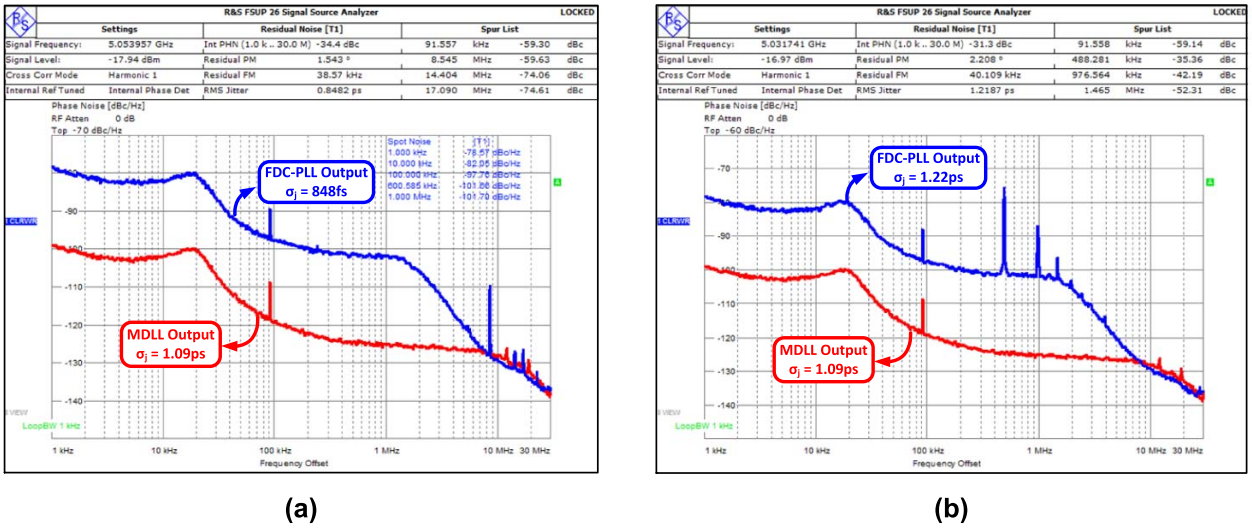


Fig. 22. Measured two-stage PLL output phase noise for output frequency of (a) 5.053955 and (b) 5.031738 GHz.

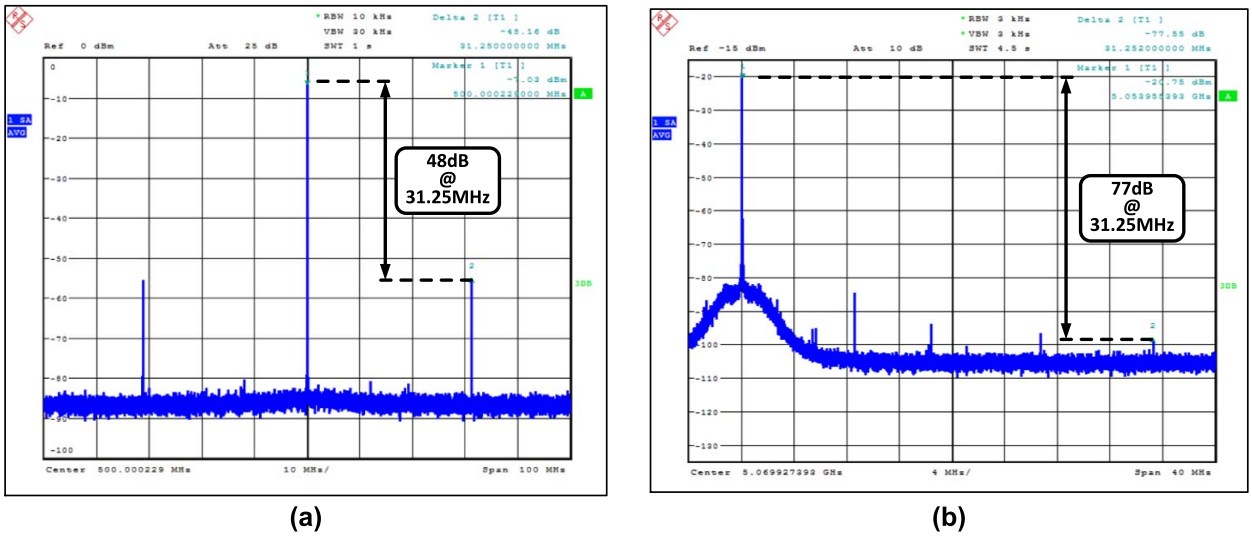


Fig. 23. Measured output voltage spectrum of (a) MDLL and (b) two-stage PLL.

bandwidth compared with gain-scaled ΔΣ FDC. The PLL with gain-scaled ΔΣ FDC also exhibits peaking due to low FDC STF bandwidth. The type I PLL shows an integrated jitter of 12.72 ps_{rms} in the frequency range of 1 kHz–30 MHz due to inferior suppression of DCO noise. Type II PLL jitter using gain-scaled FDC without PI is 1.67 ps_{rms}, while the PLL jitter using the proposed PI-based FDC is 375 fs_{rms} in the frequency range of 1 kHz–30 MHz. The PLL also achieves low in-band phase noise of −106.1 dBc/Hz using the proposed PI-based FDC. Fig. 21(a) shows the PLL output phase noise spectra with different configurations at an output frequency of 5.031738 GHz when the fractional spur is in-band. In this case, the type I PLL shows an integrated jitter of 10.1 ps_{rms} in the frequency range of 1 kHz–30 MHz while the type II PLL jitter using gain-scaled FDC without PI is 1.59 ps_{rms}, which reduces to 404 fs_{rms} when the proposed PI-based FDC is used. The PLL in-band phase noise remains almost the same, i.e., −106 dBc/Hz, using the proposed PI-based FDC. The in-band fractional spur at 488 kHz is −51.4 dBc in the case of the proposed PI-based FDC, which increases to −44.1 dBc when PI is not used.

To measure the integrated jitter and spur performance of the FDCPLL, fractional codes are swept starting from 5.03125 GHz over an offset frequency range of 7.6 kHz–15.6 MHz. As shown in Fig. 21(b), the maximum spur strength varies between −53 and −80 dBc, while the integrated jitter varies between 373 and 409 fs_{rms} over the same range of frequencies. We cannot add dither to the second-order digital ΔΣ modulator in the current prototype. This issue as well as PI nonlinearities degrade FDCPLL performance at output frequencies for which the output of the digital ΔΣ modulator is highly tonal.

The two-stage PLL achieves larger than 1 MHz bandwidth when generating 5.053955 GHz output frequency from a 31.25 MHz crystal reference. The overall output phase noise of the proposed two-stage PLL is shown in Fig. 22(a). The output phase noise of the first-stage MDLL is also plotted. When integrated from 1 kHz to 30 MHz, MDLL output jitter is 1.09 ps_{rms}, whereas the overall two-stage PLL jitter is 0.85 ps_{rms}. The increase in output jitter, compared with the case when an external high-frequency reference is used, can be attributed to the increased low-frequency phase noise from

TABLE I
PERFORMANCE COMPARISON OF PHASE DETECTION MECHANISMS IN DIGITAL FRACTIONAL-*N* PLLS

	This Work		JSSC '09 [26]	JSSC '11 [3]	JSSC '11 [27]	JSSC '12 [28]	JSSC '15 [5]	JSSC '16 [29]
	2-Stg PLL	FDC PLL						
Technology	65 nm		90 nm	65 nm	65 nm	55 nm	65 nm	65 nm
Architecture	MDLL + ΔΣ FDC	ΔΣ FDC	TA TDC	DTC	TDC + PI	Vernier TDC	DTC + TDC	SAR ADC
Calib. Free	Yes		No	No	No	No	No	No
Ref. Freq. [MHz]	31.25	500	25	40	40	26	50	50
O/P Freq. [GHz]	5		3.36	3.6	3.6	1.8	4.51	3.625
In-band PN [dBc/Hz][a]	-101.6	-106.1	-106.5	-98.4	-101.1	-99.1	-101	-104.6
Effective Resolution [ps]	5.13	12.22	2.61	8.38	6.14	6.24	6.95	4.59
Power [mW]	6.86[b]	3.84[b]	70	2.2[c]	69.6[c]	0.75	0.2	<3
Power Efficiency [dB][d]	-228.2	-223.2	-224	-228.9	-216.6	-236.1	-240.9	<-232.8

[a] In-band phase noise normalized to 5 GHz [b] Includes divider, excludes synthesized logic power [c] Includes divider
[d] Power Efficiency = $10 \cdot \log_{10}\left(\frac{(T_{LSB,eff}[s])^2}{12} \cdot P[mW]\right)$

TABLE II
PERFORMANCE COMPARISON OF DIGITAL FRACTIONAL-*N* PLLS

	This Work		JSSC '08 [15]	ASSCC '12 [30]	JSSC '13 [4]	JSSC '15 [9]	JSSC '15 [10]	JSSC '15 [5]	JSSC '16 [29]
	2-Stage PLL	FDC PLL							
Technology	65 nm		130 nm	65 nm	130 nm	65 nm	65 nm	65 nm	65 nm
Architecture	ΔΣ FDC		ΔΣ FDC	ΔΣ FDC	MO BBPD	ΔΣ FDC	ΔΣ FDC	DTC + TDC	TDC
Calib. Free	Yes		Yes	Yes	Yes	Yes	Yes	No	No
Supply [V]	1		1.4	1	1.3	1 / 1.2	1	1	1
Area [mm^2]	0.54	0.32	0.7	0.13	0.25	0.6	0.35	0.22	0.38
Ref. Freq. [MHz]	31.25	500	185.5	430	25	26	26	50	50
O/P Freq. [GHz]	5		2.2	5.8	1	3.5	3.5	4.51	3.625
RMS Jitter [ps]	1.22	0.4	–	1.03	1.9	–	0.7	0.49	0.39
In-band PN [dBc/Hz][a]	-101.6	-106.1	-77.8	-91.2	-91	-67	-90	-101	-104.6
Bandwidth [kHz]	1000		142	200	1000	40	140	750	1000
Power [mW]	10.1	7.1	14	8	7.4	21	15.6	3.7	9.7
FoM [dB][b]	-228	-239	–	-230.7	-225.7	–	-232	-239.5	-238.3

[a] In-band phase noise normalized to 5 GHz [b] FoM [dB] $= 10 \cdot \log_{10}\left((\sigma[s])^2 \times (P[mW])\right)$

crystal reference as well as MDLL. It is also seen that MDLL output has a spur at 91 kHz that appears at the FDCPLL output with a strength of −59.3 dBc. This spur is believed to be caused by the ΔΣ DAC in the MDLL implementation. As shown in Fig. 22(b), an in-band fractional spur of strength −35 dBc is measured when the two-stage PLL generates an output frequency of 5.031738 GHz while the integrated jitter is 1.22 ps_{rms}. These measurements indicate that the second-stage FDCPLL performance is sensitive to the jitter performance of its reference input. Fig. 23(a) and (b) show the output voltage spectrum of the MDLL and the second-stage output, respectively, when the final output frequency is 5.053955 GHz. A reference spur of −48 dBc is measured at the MDLL output. The second-stage FDCPLL further suppresses this reference spur to −77 dBc. Comparison of the proposed ΔΣ FDC architecture with other published TDC/DTC-based phase detection mechanisms is shown in Table I. Assuming that all the in-band phase noise is caused by the digital phase detection mechanism, the effective resolution is given by [26]

$$T_{\mathrm{LSB,eff}} = \frac{\sqrt{12 F_{\mathrm{REF}} \cdot 10^{\mathcal{L}(f)/10}}}{2\pi F_{\mathrm{OUT}}}$$

where $\mathcal{L}(f)$ is in-band phase noise expressed in dBc/Hz and F_{OUT} is the output frequency. It can be seen that the effective resolution of the proposed 1-bit $\Delta\Sigma$ FDC architecture is comparable with the state-of-the-art TDCs and DTCs despite using no calibration. On the other hand, by making use of complex digital calibration schemes, the state-of-the-art TDCs and DTCs can achieve better power efficiency compared to the proposed 1-bit $\Delta\Sigma$ FDC. The performance of the proposed two-stage PLL and its comparison with recent digital fractional-N PLLs is shown in Table II. The proposed PLL achieves more than 10 dB better normalized in-band noise floor as well as superior figure of merit compared with other calibration-free digital fractional-N PLLs. While the figure-of-merit of FDCPLL is comparable to calibrated digital fractional-N PLLs, the additional power consumption and jitter introduced by on chip high-frequency reference generator MDLL degrade the overall figure-of-merit.

V. Conclusion

In this paper, we have analyzed the "zero-input" first-order 1-bit $\Delta\Sigma$ FDC architecture and identified that reducing the input span of the 1-bit PQ significantly improves the performance of $\Delta\Sigma$ FDC. To this end, we have proposed the use of a PI-based fractional divider in $\Delta\Sigma$ FDC to achieve wide bandwidth and low in-band phase noise for an FDCPLL. To further reduce the $\Delta\Sigma$ quantization noise, we have also presented a two-stage PLL architecture that increases $\Delta\Sigma$ FDC input reference frequency by using an MDLL-based integer-N clock multiplier. Measurement results indicate that the proposed techniques enable a highly digital PLL implementation with 1-bit PQ that achieves -101.6 dBc/Hz in-band phase noise and 1.22 $\mathrm{ps_{rms}}$ jitter while generating 5.031 GHz output from 31.25 MHz reference clock input. For the same output frequency, the stand-alone FDCPLL achieves -106.1 dBc/Hz in-band phase noise and 403 $\mathrm{fs_{rms}}$ jitter with a 500 MHz reference clock input. The two-stage PLL consumes 10.1 mW power from a 1 V supply, out of which 7.1 mW is consumed by the second-stage FDCPLL.

Acknowledgment

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Mrunmay Talegaonkar (M'15) received the B.Tech. and M.Tech. degrees in electrical engineering from IIT Madras, Chennai, India, in 2007, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2016.

From 2007 to 2009, he was a Design Engineer with Analog Devices, Bengaluru, India, where he was involved in the design of digital-to-analog converters. From 2009 to 2010, he was a Project Associate with IIT Madras, where he was involved in high-speed clock and data recovery circuits. From 2010 to 2013, he was a Research Assistant with Oregon State University, Corvallis, OR, USA, where he was involved in high-speed links. He is currently a Staff Engineer with Inphi Corporation, Irvine, CA, USA. His current research interests include high-speed I/O interfaces and clocking circuits.

Dr. Talegaonkar was a recipient of the Analog Devices Outstanding Student Designer Award in 2012.

Tejasvi Anand (S'12–M'15) received the M.Tech. degree (Hons.) in electronics design and technology from the Indian Institute of Science, Bengaluru, India, in 2008, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2015.

From 2008 to 2010, he was an Analog Design Engineer with Cosmic Circuits (now a part of Cadence Design Systems). Bengaluru. He was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, in 2015. He is currently an Assistant Professor with the Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA. His current research interests include wire-line communication, frequency synthesizers, and sensors with an emphasis on energy efficiency.

Dr. Anand was a recipient of the 2014–2015 IEEE Solid-State Circuits Society Predoctoral Achievement Award, the 2015 Broadcom Foundation University Research Competition Award, the 2015 M. E. Van Valkenburg Graduate Research Award from the University of Illinois, the 2013 Analog Devices Outstanding Student Designer Award, and the 2009 CEDT Design (Gold) Medal from the Indian Institute of Science.

Ahmed Elkholy (S'08–M'17) received the B.Sc. (Hons.) and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2008 and 2012, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2016.

From 2008 to 2012, he was an Analog/Mixed-Signal Design Engineer with Si-Ware Systems, Cairo, where he was involved in designing high-performance clocking circuits and *LC*-based reference oscillators. He was with Xilinx, San Jose, CA, USA, in 2014, where he was involved in high-performance flexible clocking architectures. He is currently a Post-Doctoral Research Associate with the University of Illinois at Urbana–Champaign. His current research interests include frequency synthesizers, high-speed serial links, and low-power data converters.

Dr. Elkholy received the IEEE Solid-State Circuits Society (SSCS) Pre-Doctoral Achievement Award (2015–2016), the Analog Devices Outstanding Student Designer Award in 2016, and the M. E. Van Valkenburg Graduate Research Award from the University of Illinois (2016–2017). He also received the IEEE SSCS Student Travel Grant Award in 2015, the Intel/IBM/Catalyst Foundation CICC Student Award in 2015, the Edward N. Rickert Engineering Fellowship from Oregon State University (2012–2013), and the Best M.Sc. Thesis Award from Ain Shams University in 2012. He serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, and the IEEE International Symposium on Circuits and Systems.

Amr Elshazly (S'04–M'13) received the B.Sc. (Hons.) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2003 and 2007, respectively, and the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 2012, all in electrical engineering.

From 2004 to 2006, he was a VLSI Circuit Design Engineer with AIAT, Inc., Cairo, Egypt, where he was involved in the design of RF building blocks. From 2006 to 2007, he was with Mentor Graphics Inc., Cairo, where he was involved in designing multi-standard clock and data recovery circuits. He is currently a Design Engineer with Intel Corporation, Hillsboro, OR, USA, where he is involved in developing high-performance high-speed I/O circuits and architectures for next generation process technologies. His current research interests include high-speed serial links, frequency synthesizers, digital phase-locked loops, multiplying delay-locked loops, clock and data recovery circuits, data converter techniques, and low-power mixed-signal circuits.

Dr. Elshazly received the Analog Devices Outstanding Student Designer Award in 2011, the Center for Design of Analog–Digital Integrated Circuits Best Poster Award in 2012, and the Graduate Research Assistant of the Year Award in 2012 from the College of Engineering, Oregon State University. He serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, the IEEE International Symposium on Circuits and Systems, the IEEE International Conference of Electronic Circuits Systems, and the IEEE Asian Solid State Circuits Conference.

Romesh Kumar Nandwana (S'12) received the B.Tech. degree in electronics and communication engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 2009, the M.Eng. degree in electrical engineering from Oregon State University, Corvallis, OR, USA, in 2013, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2017.

From 2009 to 2010, he was a Scientist with Indian Space Research Organization, Ahmedabad, India, where he was involved in the design of RF power amplifiers and dc–dc converters for communication satellites. He was an Engineering Intern with Linear Technology Corporation, Grass Valley, CA, USA, in 2011, where he was involved in low-phase noise clock buffers. He was a Research Intern with Xilinx Inc., San Jose, CA, USA, in 2015, where he was involved in developing clocking circuits for high-speed links. He was a Graduate Intern with Intel Labs, Hillsboro, OR, USA, in 2016, where he was involved in high-speed optical circuits. He is currently a Hardware Engineer with Cisco Systems, Allentown, PA, USA, where he is involved in developing high-speed circuits for silicon photonic I/Os. His current research interests include frequency synthesizers, digital phase-locked loops, clock and data recovery circuits, high-speed serial links, and low-voltage mixed-signal circuits.

Dr. Nandwana received the 2016–2017 IEEE Solid-State Circuits Society Predoctoral Achievement Award. He serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the IEEE International NEWCAS Conference.

Saurabh Saxena (S'10–M'16) received the B.Tech. degree in electrical engineering and the M.Tech. degree in microelectronics and VLSI design from IIT Madras, Chennai, India, in 2009, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2015.

He is currently an Assistant Professor with the Department of Electrical Engineering, IIT Madras. His current research interests include delta–sigma modulators, high-speed I/O interfaces, and clocking circuits.

Dr. Saxena serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, and the IEEE International Symposium on Circuits and Systems.

Brian Young received the B.S. degree in electrical engineering from Pennsylvania State University, University Park, PA, USA in 2000 and the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 2013.

From 2000 to 2003, he was with Motorola Semiconductor, Chandler, AZ, USA. From 2003 to 2007, he was with AMI Semiconductor, Lower Gwynedd, PA, USA. From 2013 to 2017, he was with Marvell Semiconductor, Corvallis. Since 2017, he has been with ON Semiconductor, Corvallis. His current research interests include time-based data converters, digital PLLs, and high-performance mixed-signal circuits.

Dr. Young has received the 2010 and 2013 Analog Devices Outstanding Student Designer Award.

Woo-Seok Choi (S'12–M'16) received the B.S. and M.S. degrees in electrical engineering and computer science from Seoul National University, Seoul, South Korea, in 2008 and 2010, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2017.

He is currently a Post-Doctoral Researcher with the University of Illinois at Urbana–Champaign. His current research interests include designing energy-efficient high-speed serial links, low-power analog-to-digital converters, and interface circuits for capacitive sensors.

Dr. Choi was a recipient of the Provost's Distinguished Graduate Fellowship from Oregon State University (2011–2012), the Analog Devices Outstanding Student Designer Award in 2016, and the SSCS Predoctoral Achievement Award (2016–2017). He serves as a Reviewer of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED SYSTEMS, and the *Journal of Semiconductor Technology and Science*.

Pavan Kumar Hanumolu (S'99–M'07) received the Ph.D. degree from the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA, in 2006.

He is currently an Associate Professor with the Department of Electrical and Computer Engineering and a Research Associate Professor with the Coordinated Science Laboratory, University of Illinois at Urbana–Champaign, Champaign, IL, USA. His current research interests include energy-efficient integrated circuit implementation of analog and digital signal processing, sensor interfaces, wireline communication systems, and power conversion.

Dr. Hanumolu is an elected member of the IEEE Solid-State Circuits Society AdCom. He serves as a Technical Program Committee Member of the International Solid-State Circuits Conference. He also serves as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.