

A 4.4-5.4GHz Digital Fractional-N PLL Using $\Delta\Sigma$ Frequency-to-Digital Converter

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Abstract

A phase interpolator (PI) based fractional divider is used to improve the quantization noise shaping properties of a 1-bit $\Delta\Sigma$ frequency-to-digital converter (FDC). Fabricated in 65nm CMOS process, the prototype calibration-free fractional-N Type-II PLL employs the proposed FDC in place of a high resolution TDC and achieves -102dBc/Hz in-band phase noise and 852fs_{rms} integrated jitter (1k-40M) while generating 5.054GHz output from 31.25MHz input.

Introduction

Digital fractional-N PLLs have recently gained popularity due to their portability, configurability, and compatibility with manufacturing processes optimized for digital circuits. A major design bottleneck of digital fractional-N PLLs is the time-to-digital converter (TDC) quantization error, which increases in-band noise and degrades spurious performance. An all-digital $\Delta\Sigma$ FDC is an attractive alternative to a high resolution TDC in digital fractional-N PLLs [1-2].

As depicted in Fig. 1(a) a conventional 1-bit FDC consists of a dual-modulus divider (DMD) controlled by the output of a D flip-flop (DFF) [1]. With the DMD and DFF operating as a frequency integrator and a phase quantizer (PQ), respectively, the FDC acts as a $\Delta\Sigma$ modulator that digitizes the frequency difference between its inputs, CK_{REF} and CK_{VCO} . The PQ quantization error, E_Q , is 1st order noise shaped by the FDC loop. The resolution of the FDC is dictated by the oversampling ratio (OSR) decided by CK_{REF} frequency, F_{REF} , and PQ step size T_{PQ} . When used in a PLL, the FDC output is accumulated to estimate the phase error between its inputs with an effective quantization noise floor of $T_{PQ}^2/12F_{REF}$. In a conventional FDC, T_{PQ} equals the CK_{VCO} period, T_{VCO} . To achieve low in-band noise floor for the PLL, T_{PQ} can be further reduced to $T_{VCO}K_{PD}$, by scaling PQ output by K_{PD} and truncating the result using a digital $\Delta\Sigma$ modulator to 1-bit, as illustrated in Fig. 1(b) [2]. However, in practice, the benefits of the scaling approach are limited by highly nonlinear behavior of PQ resulting from its input spanning a large range ($\pm T_{VCO}/2$). The PQ nonlinearity increases the quantization noise floor, causes peaking due to limit cycles, and limits the effective bandwidth of the $\Delta\Sigma$ FDC loop. Additionally, the low bandwidth Type-I FDC-PLL implementation reported in [2] cannot adequately suppress low frequency VCO phase noise. In view of these drawbacks, this paper presents a Type-II PLL that utilizes a new FDC architecture to achieve low in-band noise and wide bandwidth.

Proposed Architecture and Implementation

The proposed PI-based FDC is shown in Fig. 2. We propose replacing the DMD used in conventional FDCs [1-2] with a PI-based fractional divider. A 20-bit fractional control word, N_{FRAC} , is combined with the scaled PQ output and fed to a 2nd order $\Delta\Sigma$ modulator. The digital $\Delta\Sigma$ modulator truncates its input to generate a 6-bit control word for the fractional divider. The $\Delta\Sigma$ modulator performs both PQ gain scaling as well as fractional dithering functions [2]. In the fractional divider, a

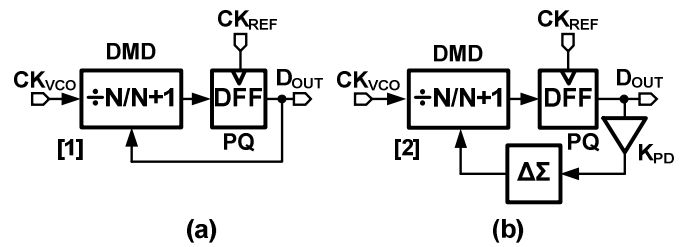


Fig. 1: Conventional 1-bit $\Delta\Sigma$ FDC architectures from [1], and [2].

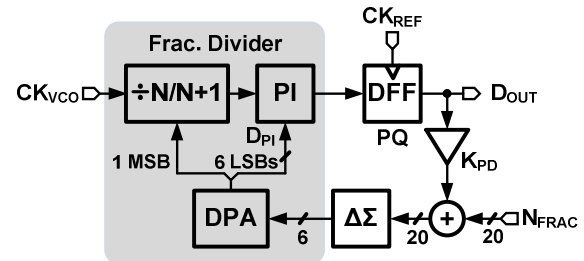


Fig. 2: Block diagram of the proposed PI-based $\Delta\Sigma$ FDC.

digital phase accumulator (DPA) implements the phase accumulation and modulo- 2π operation. The MSB and the 6 LSBs (denoted as D_{PI}) of the DPA output control the DMD and PI, respectively. The combination of DMD and PI acts as a 6-bit fractional divider and reduces the PQ input span from $\pm T_{VCO}/2$ to $\pm T_{VCO}/2^7$, thus alleviating the detrimental effects of PQ nonlinearity. The in-band quantization error is further suppressed by increasing the OSR using a reference frequency of 500MHz for the FDC.

Figure 3 shows the complete two-stage fractional-N PLL block diagram. The first stage digital multiplying delay-locked loop (MDLL) generates a 500MHz high frequency reference (REF_{HF}) from a 31.25MHz external crystal oscillator. The choice of MDLL is influenced by its excellent low frequency phase noise performance due to reference injection mechanism. REF_{HF} is used as reference input for the proposed PI-based $\Delta\Sigma$ FDC in the 2nd stage FDC-based PLL (FDC-PLL). The FDC output is decimated by a factor of 4 to obtain a 10-bit frequency error (F_{ERR}), which is accumulated to generate the phase error word (Φ_{ERR}). Φ_{ERR} is subsequently fed to a proportional-integral digital loop filter to achieve Type-II PLL response. A 2nd order digital $\Delta\Sigma$ modulator truncates the 14-bit loop filter output to 5-bits and drives a current-mode DAC. A second order passive RC low-pass filter suppresses the shaped DAC quantization error and generates control voltage, V_C , to tune the LC-VCO frequency.

The PI schematic is shown in Fig. 4. To avoid the need for quadrature phases, shift register based PI architecture is chosen. The VCO clock samples DMD output using a shift register arrangement and generates two coarse phases, Φ_0 and Φ_1 , that are T_{VCO} apart. A CML-based phase mixer performs phase interpolation between Φ_0 and Φ_1 according to the 6-bit control word D_{PI} . A 63-element thermometer-coded current steering DAC is used to control the interpolation weight in a monotonic fashion. PI linearity is improved by pre-distorting the DAC

unit elements and controlling the rise/fall times of Φ_0 and Φ_1 . Two fixed half LSB current sources are used to improve phase mixer bandwidth.

Measurement Results

The two-stage PLL is implemented in 65nm CMOS process. The first stage MDLL and second stage FDC-PLL occupy an active area of 0.22mm^2 and 0.32mm^2 , respectively. The total power consumption when generating a 5.054GHz output from a 31.25MHz reference input is 10.9mW, out of which the MDLL consumes 3.3mW. Figure 5 shows the measured output phase noise characteristics with 500MHz external reference in following configurations: Type-I FDC-PLL without PI, Type-II FDC-PLL without PI and Type-II FDC-PLL with PI. Compared to the Type-I FDC-PLL, Type-II FDC-PLLs exhibit superior phase noise performance at low offset frequencies (38dB improvement at 1kHz offset). Further, the proposed PI-based FDC improves the in-band phase noise floor of the type-II FDC-PLL by 13dB for the same loop parameters. The PI-based FDC-PLL also does not exhibit phase noise peaking due to reduced PQ input span. Figure 6 shows the measured output phase noise of the 2-stage fractional-N PLL at 5.054GHz output when using 31.25MHz reference input to the MDLL. The in-band noise floor is -102dBc/Hz . The TDC resolution needed to achieve similar noise floor in a conventional PLL is 4.84ps. The integrated jitter from 1kHz to 40MHz is $484.5\text{fs}_{\text{rms}}$ and $852\text{fs}_{\text{rms}}$, when the reference frequencies are 500MHz and 31.25MHz, respectively. The reference spur at the output is measured to be -84dBc when operating with 31.25MHz reference frequency. Performance summary of the PLL and its comparison with recently reported digital fractional-N PLLs that require no calibration are shown in Fig. 7. Compared to other implementations, this work achieves 10dB lower in-band phase noise when normalized to output frequency. Also notable are the wide bandwidth and superior FoM achieved for comparable reference frequencies.

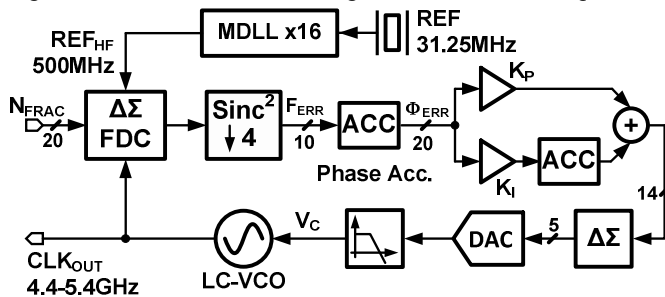


Fig. 3: Block diagram of the proposed fractional-N PLL.

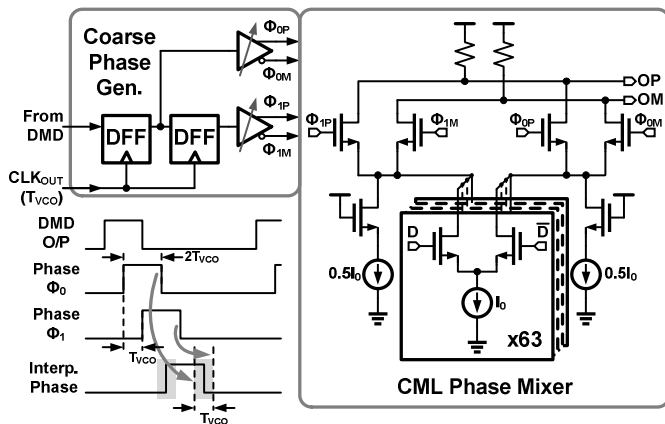


Fig. 4: Phase interpolator schematic.

The die micrograph, and the voltage spectrum of the 2-stage PLL output are also shown in Fig. 7.

Acknowledgements

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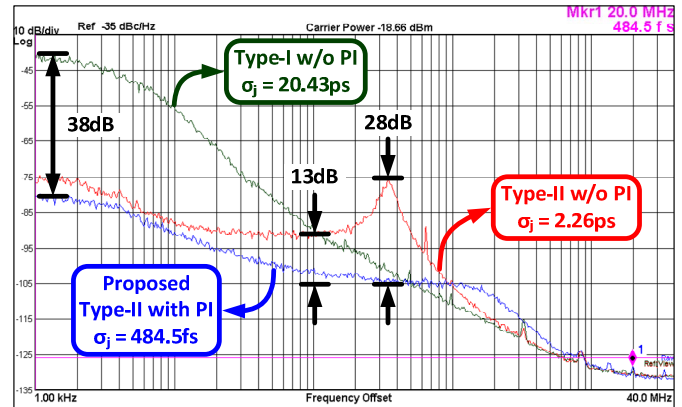


Fig. 5: Measured phase noise of three FDC-PLL configurations.

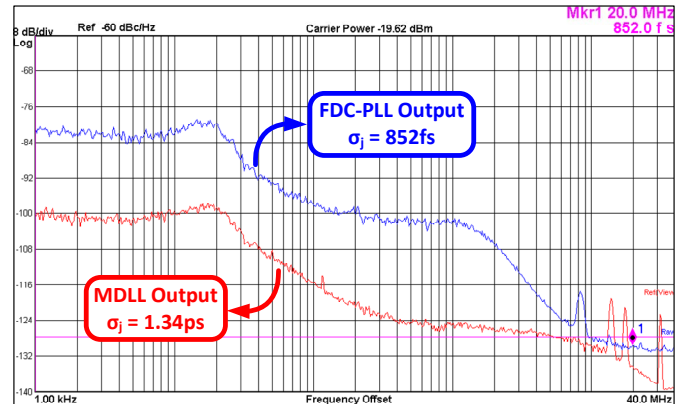


Fig. 6: Measured overall output phase noise performance of the 2-stage fractional-N PLL (MDLL + FDC-PLL).

	This Work		ISSCC'07 [2]	ASSCC'12 [3]	ISSCC'12 [4]	JSSC'13 [5]
	2-Stage PLL	FDC-PLL Only				
Technology	65nm CMOS		130nm CMOS	65nm CMOS	40nm CMOS	130nm CMOS
Architecture	1-b FDC		1-b FDC	1-b FDC	4-b TDC	5-b MOBBPD
Supply [V]	1		1.4	1	1.1	1.3
Area [mm ²]	0.54	0.32	0.7	0.133	0.06	0.25
Ref. Freq. [MHz]	31.25		185.5	430	25	25
Output [GHz]	4.4-5.4		2.2	5.8	0.23-4.5	0.84-1.032
RMS Jitter [ps]	0.85 (1k-40M)	0.48 (1k-40M)	N/A	1.03	1.65 (1k-10M)	1.9 (1k-20M)
In-band phase noise [dBc/Hz]	-102 @ 600k	-104.8 @ 600k	-85 @ 100k	-90 @ 100k	-95 @ 1.6k	-105 @ 100k
Normalized PhNoise @ 5.054GHz [dBc/Hz]	-102 @ 600k	-104.8 @ 600k	-77.8 @ 100k	-91.2 @ 100k	-86 @ 1.6k	-91 @ 100k
Bandwidth [kHz]	2000		142	200	100	1000
Power [mW]	10.9	7.6	14	8	13.2	7.4
FoM* [dB]	-231	-237.5	N/A	-230.7	-224.4	-225.7

*FoM [dB] = $10 \log_{10}(\sigma_j^2) \times (P[\text{mW}])$

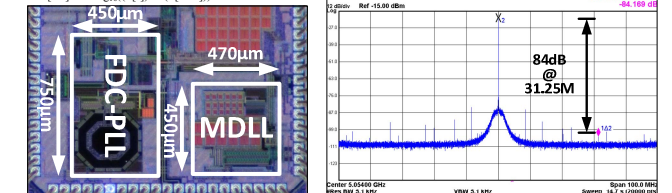


Fig. 7: Performance summary, die micrograph, and output voltage spectrum of the proposed 2-stage PLL.