A 75dB DR 50MHz BW 3rd Order CT-ΔΣ Modulator Using VCO-Based Integrators

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Abstract

A wide bandwidth, high sample rate 3rd order continuous-time ΔΣ modulator using VCO-based integrators is presented. Non-idealities caused by VCOs at the modulator frontend are addressed using both circuit- and architecture-level techniques. Fabricated in 65nm CMOS, the prototype modulator operates at 1.28GS/s and achieves a dynamic range of 75dB, SNR of 71dB in 50MHz bandwidth, while consuming 38mW of total power.

Introduction

Voltage-controlled-oscillator (VCO) based ADCs exhibit many desirable properties such as inherent quantization noise shaping, implicit anti-aliasing, and guaranteed monotonicity. Because they can be implemented using mostly digital circuits, their performance (resolution and energy efficiency) improves with technology scaling. A majority of the VCO-based ADCs are implemented using the feed-forward (FF) topology in which the VCO converts input voltage (V_{IN}) to frequency and a frequency-to-digital quantizer generates the noise-shaped digital output [1-5]. They suffer from two main drawbacks. First, because V_{IN} spans the entire tuning range of the VCO, such ADCs are susceptible to the non-linear voltage-to-frequency (V-to-F) transfer characteristic. Second, the order of noise shaping is limited to the first order, which makes it difficult to increase the signal bandwidth without compromising dynamic range. Calibration can help alleviate the impact of nonlinearity [1-2], but increasing the order mandates that VCO-based ADC be placed in the backend of a ΔΣ loop [5].

A VCO-based first-order ΔΣ modulator can also be implemented with a feedback (FB) topology using VCO as a voltage-to-phase integrator along with a phase quantizer and feedback DAC [6]. Due to high loop gain, VCO input spans only a small range, thus making FB topology largely insensitive to VCO's V-to-F nonlinearity. Furthermore, a VCO integrator transforms analog signals from the voltage-domain to time-domain, which makes signal dynamic range independent of supply voltage. Also, compared with traditional active-RC integrators, the highly digital nature of VCOs makes them technology-scaling friendly. However, increasing modulator order beyond first order requires a classical power hungry frontend integrator [6]. In this work, we demonstrate a VCO-based 3rd order CT ΔΣ modulator using VCO integrators in the frontend. The proposed design operates at 1.28Gs/s and achieves 75dB DR in 50MHz bandwidth.

Proposed Architecture

The proposed ΔΣ modulator schematic is shown in Fig. 1. The single-ended version is shown for simplicity. The modulator's notable feature is the introduction of VCO integrators in the modulator frontend. The first two integrators are implemented using voltage- and current-controlled ring

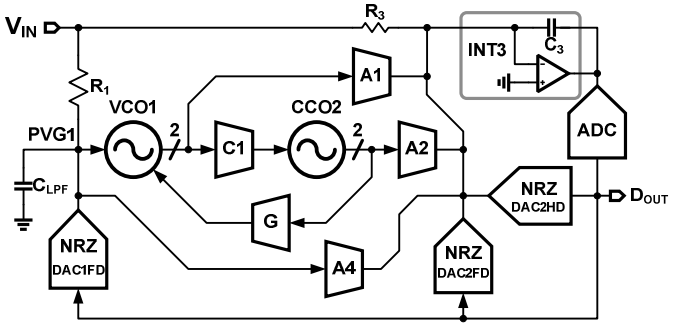

Fig. 1: Schematic of proposed third-order ΔΣ modulator.

oscillators, *VCO1* and *CCO2*, respectively. Both *VCO1* and *CCO2* nominally oscillate at 640MHz. The high impedance input of *VCO1* creates a pseudo virtual ground (PVG) and induces a passive integrator (PI). Capacitor C_{LPF} is added to lower the PI pole frequency to ~100MHz, reducing the impedance at PVG1 and sensitivity to *DAC1FD* current pulses. The low-Q nature of ring oscillator based VCOs introduces a parasitic second pole to the ideal integrator transfer function. This pole is proportional to the frequency of oscillation. The feed-forward path, consisting of transconductor, *A4*, provides an additional degree of freedom in compensating loop delay caused by PI and oscillator parasitic poles. Two phases from each oscillator control source-switched charge pumps (CP) to realize feed-forward gains, *A1* and *A2*, inter-stage gain, *C1*, and resonator gain *G*. Feed-forward resistor R_3 minimizes signal content processed by *VCO1* and *CCO2*, thereby improving modulator linearity. The third integrator, *INT3*, is implemented using active-RC architecture in order to provide a virtual ground for accurate current summation. Its op-amp is a two-stage amplifier with telescopic cascode first stage and common source second stage and is cascode compensated. A 4-bit flash ADC quantizes *INT3* output. All feedback DACs are of non-return-to-zero (NRZ) current steering type and have 17-levels. The primary feedback DAC, *DAC1FD*, has one full clock cycle delay. Current-mode fast feedback, using half/full-delay DACs, *DAC2HD* and *DAC2FD*, compensates excess loop delay. A thermometer encoder converts flash ADC output to Gray code to reduce supply sensitivity to major code transitions.

Figure 2 shows the block diagram of the pseudo-differential VCO integrator, *VCO1*. It is comprised of a digitally tunable source degenerated transconductor stage followed by current-controlled ring oscillators with quadrature phase outputs. A set of XOR phase detectors convert CCO output phase to pulse-width modulated signals. The transconductor stage converts input voltage (PVG1) into current, which controls the delay of the pseudo-differential delay cells within the oscillators. The use of more than one oscillator phase improves the temporal phase sampling approximation of VCO integrator phase. The *CCO2* architecture is similar to *VCO1* without transconductor stage.

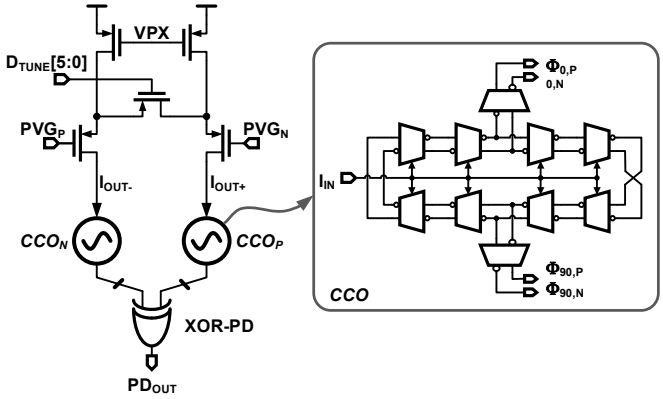

Fig. 2: Circuit diagram of *VCO1*.

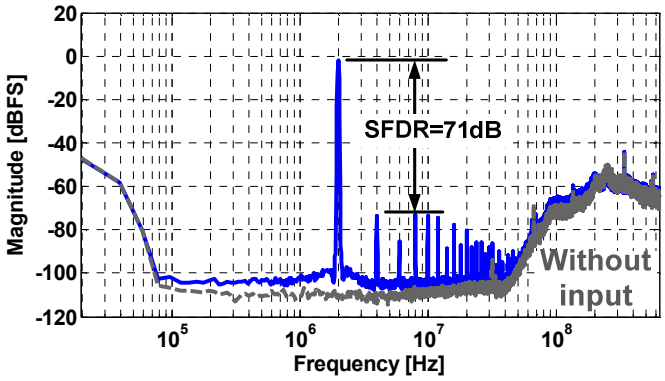

Fig. 3: FFT spectrum with and without 2MHz -1.8dBFS input.

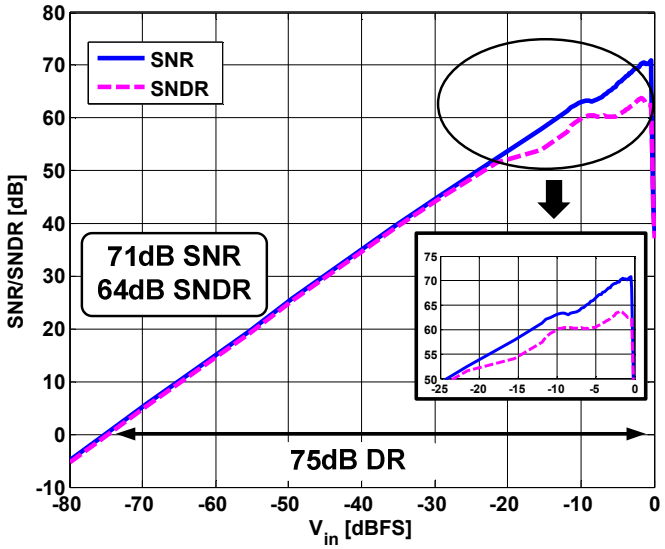

Fig. 4: Measured SNR and SNDR versus full-scale input.

Measurement Results

A prototype CT ΔΣ modulator was fabricated in a 65nm CMOS, and it occupies an active area of 0.49mm^2. Clocked at 1.28GHz, the modulator consumes 38mW power. The quadrature phase of the 1.28GHz sampling clock are generated from a 2.56GHz external reference. Figure 3 plots the windowed FFT spectrum of the digital output with and without a -1.8dBFS 2MHz input tone. The 4th harmonic limits SFDR to about 71dB. The measured SNR and SNDR, plotted as a function of input amplitude, is shown in Fig. 4. The modulator achieves a dynamic range, SNR, and SNDR in 50MHz BW of 75dB, 71dB, and 64dB, respectively. Typical DAC mismatch mitigation techniques proved to be too slow; therefore, the area of *DAC1FD* current sources was increased to reduce random mismatch. A small dip in SNR at -8dBFS is attributed to *DAC1FD* layout imperfections. A performance summary and comparison table of state-of-the-art wide BW VCO-based ADCs is shown in Table I. This work achieves a FOM_{SNDR} of 294fJ/conv. and FOM_{DR} of 83fJ/conv. and has the widest bandwidth among all published VCO-based ADCs to date. A die photograph is shown in Fig. 5.

Table I: Performance summary and comparison table.

	This Work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Architecture	VCO	VCO	VCO	VCO	VCO	VCO	VCO	op-amp
Fs [MHz]	1280	2400	640	640	600	950	900	4000
BW [MHz]	50	37.5	5	8	10	20	20	125
DR [dB]	75	73	77	65.6	83.5	71	77	70
SNR [dB]	71	71	75.4	61.1	79.1	60	81.2	65.5
SNDR [dB]	64	70	73.9	59.9	78	55	78.1	65
Power [mW]	38	39	4.1	4.3	16	38	87	256
V_{DD} [V]	1.5/1.2	1.2	1.2	1.2	1.4/1.0	1.2	1.5	1.8/1.1
Area [mm^2]	0.49	0.075	0.16	0.1	0.36	0.185	0.45	0.9
Technology [nm]	65	65	90	90	90	130	130	45
FOM [fJ/conv.][1]	294	201	101	333	123	2069	331	705
FOM [fJ/conv.][2]	83	143	71	173	65	328	376	397

FOM [fJ/conv.][1] = P/(2*BW*2^((SNDR-1.76)/6.02))
FOM [fJ/conv.][2] = P/(2*BW*2^((DR-1.76)/6.02))

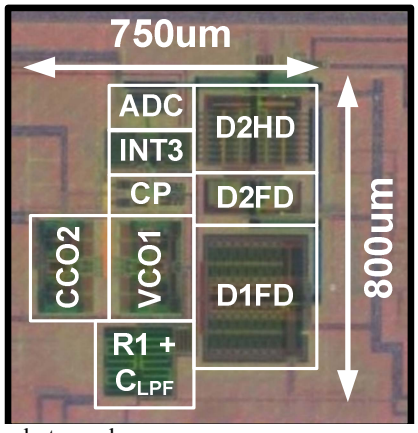

Fig. 5: Die photograph.

Acknowledgements

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References

[1] G. Taylor, and I. Galton, "A reconfigurable mostly-digital ΔΣ ADC with a worst-case FOM of 160dB," *VLSIC*, Jun. 2012.

[2] S. Rao, et al., "A 4.1mW, 12-bit ENOB, 5MHz BW, VCO-based ADC with on-chip deterministic digital background calibration in 90nm CMOS," *VLSIC*, Jun. 2013.

[3] S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, and P.K. Hanumolu, "A 71dB SFDR open loop VCO-based ADC using 2-level PWM modulation," *VLSIC*, Jun. 2011.

[4] K. Reddy, et al., "A 16mW 78dB-SNDR 10MHz-BW CT-ΔΣ ADC using residue-cancelling VCO-based quantizer," *ISSCC*, Feb. 2012.

[5] M.Z. Straayer, and M.H. Perrott, "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based quantizer and DEM circuit in 0.13μ CMOS," *VLSIC*, Jun. 2007.

[6] M. Park, and M. Perrott, "A 0.13μm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-based integrator and quantizer," *ISSCC*, Feb. 2009.

[7] M. Bolatkale, L.J. Breems, R. Rutten, and M.A.A. Makinwa, "A 4GHz continuous-time ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW," *ISSCC*, Feb. 2011.