# Thermal Management of SiC MOSFETs within Hydrokinetic Applications

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*Abstract*—**Hydrokinetic turbines are an emerging form of renewable energy generation. Although functionally similar to wind turbines, hydrokinetic systems incur extra costs and face constraints in available footprint. SiC power semiconductors within the required power electronics improve the performance. However, challenges within the design stem from an aquatic environment with corrosion and accumulation of organic matters, which eventually impact the thermal behavior of the power electronics. This paper provides a practical model of average device power losses and proposes a heat sink design to regulate device junction temperature. The design is validated in mathematical models and their simulations. A water-tank-based hardware experiment involving circulating water current and submerged power electronics is conducted to confirm the model, and the results are compared.**

*Index Terms*—**Hydrokinetic power, Turbine, Submerged power converter, SiC devices, Heatsink, Thermal modeling, Thermal design.**

## I. INTRODUCTION

The U.S. Energy Information Administration (EIA) predicts a constant growth in annual U.S. energy consumption of 1-2% until 2050 [1]. In that same time, it is predicted that the total power generated by coal and nuclear sources will drop by about 8%, while natural gas sources will drop by about 4% [1]. On the other hand, renewable generation is predicted to double, jumping from 21% when the study was done in 2020 to 42% in 2050 [1]. With these predicted numbers and the ever-growing threat of climate change, additional renewable energy generation sources must be considered.

Hydropower is one of the oldest forms of power generation, with the first grain mill driven by a water wheel dating back to Roman times [2]. Traditionally, large dams are used to generate hydroelectric power, constructions are limited due to their geographic restrictions, large costs, and environmental

and ecological impacts [3]. These issues are coming to light while riverine and tidal currents are still widely untapped [4]. Emerging hydrokinetic generation methods increase the percentage of energy harvested from water currents without the large structures and the ecological side-effects of traditional hydroelectric dams [4] [5]. Ducted hydrokinetic turbines are one such solution [4]. The use of hydrokinetic turbines, pictured in Figure 1, is traditionally limited due to high costs in constructing and maintaining their systems [4]. Advances must be made to improve initial cost, simplicity, and reliability, to increase the viability of hydrokinetic turbines for power generation.

A possible solution to create a simpler hydrokinetic system is using direct drive turbines. A direct-drive configuration offers a reduced mechanical part count, reducing its size and mechanical complexity. Direct-drive does come at the cost of more advanced power electronics and controls. Muljadi et al. [6] present a possible direct-drive architecture, requiring additional power electronics to maintain a more constant DC bus voltage. Ref [7] provides another design with similar characteristics featuring a more advanced control scheme. These added electrical components lessen the impact of the reduction in mechanical components afforded by the direct-drive architecture.



Fig. 1: Ducted turbine for hydrokinetic power generation. Adapted from [4].

Furthermore, cost savings from the absence of a gearbox may be diminished due to the inclusion of added electrical systems. Recent advances in power electronics may offer a solution to this. Silicon Carbide (SiC) power MOSFETs offer advantages over standard Silicon (Si) devices with a reduction in power losses and the ability to use higher switching speeds and voltages [8] [9] [10]. Higher switching frequency allows for the size reduction of filtering components within the circuit, mitigating some of the downsides to the direct-drive architecture [10]. Additionally, lower switching and conduction losses allow for an added ease in thermal management for SiC devices [8] [10]. Studies for SiC heatsink designs are presented in [11] and [12] but fail to address the complexities of a high-salinity aquatic environment. Further, [13] provides studies for IGBTs in undersea power electronics, but this cannot represent the forced convective cooling of SiC MOSFETs within the hydrokinetic application presented here. Additionally, [13] does not consider biofouling or corrosion. Research into SiC devices within submerged hydrokinetic applications is required.

This paper proposes a reliable small-footprint heat sink design that takes advantage of the forced convection due to riverine or ocean currents. First, MOSFET power losses are modeled for different devices from various manufacturers. Next, the initial thermal design is highlighted along with calculation and optimization for the application at hand while considering the harsh aquatic environment. Then simulations from a steady-state thermal model are provided. A water-tank-based hardware experiment involving controlled water current and submerged power electronics is conducted to confirm the model's findings. Finally, implications and future work are mentioned.

## II. POWER LOSS MODELING

Temperature generation within SiC MOSFETs facilitates accelerated aging. Aging effects include bond wire fatigue, solder fatigue, and gate-oxide degradation [14] [15]. Short-term operational characteristics such as device on-state resistance, capacitance, and switching losses also show considerable variation with temperature [15]. Therefore, accurate power loss modeling is critical when designing heat sinks to regulate junction temperature and to further schedule maintenance to prevent failures.

Before an initial design is conducted, operational parameters must be set. Project requirements dictate maximum power per hydrokinetic turbine to be 5 kW; then, several voltage and current pairs can be created to model the losses of the MOSFETs in question. Drain-source voltage ranges between 200 V and 1000 V, where drain current ranges from 5 A to 25 A. These are assumed in standard hard switching operation. With these parameters set, potential switches can be picked.

During device selection, a blocking voltage rating of 1200 V was chosen to provide ample safety margin and $R_{ds(on)}$ of 80 m$\Omega$ or lower, which in part is dictated by the drain current and switching frequencies. A high switching frequency could be used to tolerate the worst-case design scenario. Switches

were picked with a maximum operating temperature of 150 °C or greater. Finally, only MOSFETs coming in the TO-247-3 package would be used due to their abundance and ease of installation and replacement. Those devices with available SPICE models were given priority. Five discrete switches were simulated in a double pulse test within LTspice, which assessed the switching losses, across the voltage/current pairs. Table I shows each of the devices chosen to test. Figure 2 presents an example DPT circuit.

The switching loss is modeled in LTspice. The inductance in the circuit is changed through the various tests to maintain the required drain current. A second MOSFET is used but kept in the off state to use its intrinsic body diode for circulating current. This is done through a negative gate voltage. Next, the device under test is changed to the model of the current MOSFET being tested. Gate resistance for the MOSFET is kept at 4$\Omega$. Finally, a pulse signal provides the signal to turn the device on and off. It is specified as a pulse train with set times for T1, T2, and T3 used in the DPT. The overall model is run as a Transient simulation and given a stop time of 10 $\mu$s. The timestep is changed for each switching device to ensure that the model converges.

Once the simulation is complete, drain-to-source voltage and drain current are measured using the scope tool within LTspice. This data is exported to a text file and copied into

TABLE I: Table of Tested SiC MOSFETs.

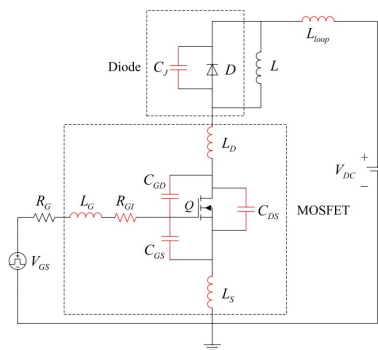| Device | $R_{ds(on)}$ (m$\Omega$) | Rated Voltage (V) | Rated Current (A) |
|---|---|---|---|
| ON Semi. NTHL040N120SC1 | 39 | 1200 | 42 |
| ON Semi. NTHL020N120SC1 | 20 | 1200 | 103 |
| Microchip MSC080SMA120B | 80 | 1200 | 37 |
| Microchip MSC040SMA120B | 40 | 1200 | 66 |
| Microchip MSC020SMA120B | 20 | 1200 | 103 |



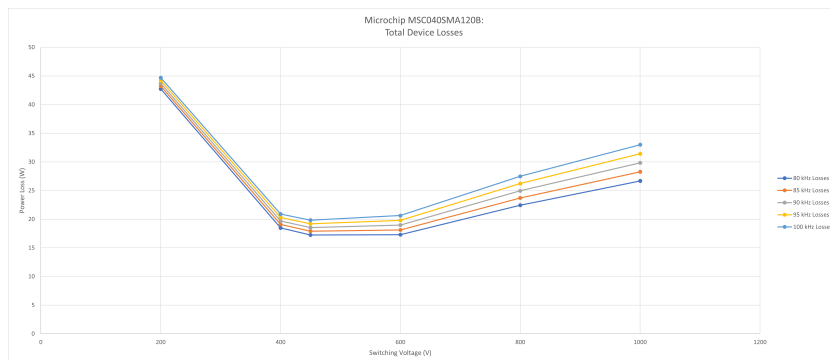Fig. 2: Double pulse test with circuit parasitics. Adapted from [16].

Fig. 3: Total power loss graph for the Microchip MSC040SMA120B.

an Excel spreadsheet. The voltage and current waveforms are again plotted within Excel, and the required multiplication and integration is performed. The energy graph is plotted; $E_{off}$ and $E_{on}$ are derived from this graph through inspection of points. This process is repeated for each switching device at all the different voltage/current pairs. Switching losses are approximated for every device/voltage/current combination at 5 kHz intervals between 80 kHz and 100 kHz. In the actual application these switching frequencies may be reduced to reduce switching losses. These losses are then added to the conduction losses at each voltage/current pair using the manufacturer-rated $R_{ds(on)}$ at 100 °C.

Figure 3 specifically shows the total device power losses for a specific DUT, in this case, the Microchip MSC040SMA120B. There is an evident "knee" in the loss graph at 450 V. This knee is due to balancing switching and conduction losses and when one begins to outweigh the other. The location of the knee depends on the rated $R_{ds(on)}$ of the switch, with a higher $R_{ds(on)}$ resulting in a higher knee voltage. In all simulated devices, the value at the knee corresponds to the voltage/current pair with the lowest overall losses.

Tables for each SiC MOSFET depicting the total losses can be obtained. Table II presents the losses at 100 kHz for all the MOSFETs. The ON Semiconductor NTHL040N120SC1 has the lowest losses, with 14.79 W at 80 kHz and 450 V/11.1 A. Meanwhile, the Microchip MSC080SMA120B has the highest losses of 73 W at 100 kHz and 200 V/25 A. Though the maximum power loss is much higher than the minumum, it is

vital to remember that these numbers cannot be viewed in a vacuum. Many other components in the circuit are influenced by the switching frequency, voltage, and current levels. The benefits for those components may outweigh the reduction in power loss, meaning that it may not be possible to compare the power losses dependent on switching frequency without weighing the other implications to the system. To keep the problem simple, 73 W is chosen to be the power loss of the MOSFETs to provide a worst-case scenario figure when calculating junction temperatures and the effects on the system thermals.

III. THERMAL DESIGN & MODELING

Multiple factors influence the heat sink design, such as heat transfer coefficients, footprint, reliability, and cost. Different geometries were considered. A control design came in the form of a simple flat plate geometry. A complex geometry where the power electronics were mounted inside of the nacelle of the hydroturbine and a boiler/condenser system was simulated. Finally, a fin array design was analyzed. Mathematical simulations in MATLAB and three-dimensional simulations within Fusion 360 were conducted for the various geometries. Each of these designs were analyzed both quantitatively and qualitatively. This analysis is was based off steady-state MOSFET junction temperature at maximum power loss, simplicity, reliability, footprint and cost and is performed in [17]. After analysis, the fin array approach was chosen to best fit the design requirements. Fins offer a simple design

TABLE II: Power Loss (W) at 100 kHz.

| Device | 200 V & 25 A | 400 V & 12.5 A | 450 V & 11.1 A | 600 V & 8.3 A | 800 V & 6.25 A | 1000 V & 5 A |
|---|---|---|---|---|---|---|
| ON Semi. NTHL040N120SC1 | 41.5 | 17.6 | 16.7 | 18.1 | 22.2 | 32.0 |
| ON Semi. NTHL020N120SC1 | 33.2 | 21.8 | 24.0 | 29.6 | 40.7 | 53.2 |
| Microchip MSC080SMA120B | 73.0 | 23.7 | 21.3 | 18.2 | 17.6 | 21.1 |
| Microchip MSC040SMA120B | 44.7 | 20.9 | 19.8 | 20.6 | 27.5 | 33.0 |
| Microchip MSC020SMA120B | 33.2 | 21.8 | 24.0 | 29.6 | 40.7 | 53.2 |

while maintaining high thermal effectiveness, partly due to the enhanced cooling of an aquatic environment.

An expanded mathematical model is created in MATLAB and uses equations adapted from [18]. The model begins with defining the thermal constants for seawater, the thermal interface material, and the heat sink made of Aluminum 6061. Physical constraints must be set to keep the footprint and cost down. The height, pitch, and width are constrained between 2 mm and 30 mm. The end goal is to find the junction temperature of the MOSFET for each combination of fin array dimensions, then find which one offers the lowest volume while maintaining a required temperature. To find the temperature, the thermal resistances in the circuit must be found. Junction to case, thermal interface, and heat sink conduction resistances are approximated using the standard conduction resistance equation. MOSFET power loss is approximated with a quadratic relation to water velocity, with a maximum of 73W of power loss. Further, it is assumed that a ducted turbine with a contraction ratio of 1.33:1 is used. The equivalent thermal resistance of the fin array is more difficult to calculate, as follows.

To start, the convective heat coefficient, h, is found using (1).

$$h = \frac{Nu_{forced}K}{x}.$$ (1)

where K is the conductivity of water, L is the length of the heat sink. $Nu_{forced}$ is calculated with (2) if the flow is laminar or (3) if it is turbulent.

$$Nu_{forced,laminar} = 0.664Re^{1/2}Pr^{1/3}$$ (2)

or

$$Nu_{forced,turbulent} = (0.037Re^{4/5} - 871)Pr^{1/3}$$ (3)

within these, the Reynolds number, Re, is calculated using (4).

$$Re = \frac{\rho v L_c}{\mu}$$ (4)

In the (4), v is an array of water velocities, and the other variables are fluid properties of water. The Reynolds number is checked to determine laminar or turbulent flow. Turbulent flow exists if Re is greater than $5*10^5$. In order to approximate the worst-case cooling scenario, the water velocity where rated power is first reached is used for the h calculation. This velocity represents the greatest power loss within the MOSFET with a relatively low convective cooling coefficient.

Using these equations, the convective heat transfer coefficient is calculated and the heat transfer rate of a single fin can be calculated with (5).

$$q_f = \bar{M}\frac{sinh(mL) + \frac{h}{mk}cosh(mL)}{cosh(mL) + \frac{h}{mk}sinh(mL)}$$ (5)

Where:
- $h$ = Convective heat transfer coefficient
- $k$ = Conductivity of the heatsink

- $L$ = Length of the heatsink
- $T_{sat}$ = Saturation temperature

$\bar{M}$ and m are defined using (6) and (7), respectively.

$$\bar{M} = \sqrt{hPkA_c\Theta_b}$$ (6)

and

$$m = \sqrt{\frac{hP}{kA_c}}$$ (7)

Where:
- $P$ = Perimeter of the fin
- $\Theta_b$ = Temperature difference between the base of the fin and ambient
- $A_c$ = Cross-sectional area of the fin

With the heat transfer rate of the fin calculated, and a known temperature difference between the fin's base and the ambient temperature, $\Theta_b$, the thermal resistance of a fin can be calculated from (8).

$$R_{fin} = \frac{\Theta_b}{q_f}$$ (8)

The thermal resistance of a single fin can then be used to calculate that of the array by the parallel resistances of individual fins and the unfinned area in between.

$$R_{array} = \frac{1}{\frac{N}{R_{fin}}} + \frac{1}{\frac{1}{A_bh}}$$ (9)

where N is the total number of fins and Ab is the total area between the fins in the array. The total volume of each width/pitch/height combination is also calculated. From this point, the other resistances within the circuit are calculated using the standard equation for thermal conduction resistance, (10).

$$R_{T,cond} = \frac{x}{LHK}$$ (10)

Where:
- $x$ = Material thickness
- $L$ = Width
- $H$ = Height
- $K$ = Thermal conductivity

This includes the thermal resistances of the heatsink body and the thermal interface material. These are added to MOSFET junction resistance and the others present within the circuit to get (11)

$$T_{junction} = P_{q,loss}(R_{jc} + R_{hs} + R_{TIM} + R_{array}) + T_{amb}$$ (11)

Where:
- $P_{q,loss}$ = MOSFET power loss
- $R_{jc}$ = MOSFET junction to case thermal resistance
- $R_{TIM}$ = Thermal interface resistance
- $R_{hs}$ = Heat sink body resistance
- $R_{array}$ = Fin array thermal resistance

- $T_{amb}$ = Ambient temperature (Assumed to be 20°C)

With (11), junction temperature can be calculated for each combination of heatsink width, pitch and height. Each combination's temperature calculation is done at an initial $\Theta_b$. Once the junction temperature is calculated, $\Theta_b$ is recalculated with the found thermal resistances; this repeats until $\Theta_b$ converges. Once $\Theta_b$ has converged, the final MOSFET junction temperature is calculated for each individual combination of fin array dimensions.Heat sink volume and junction temperature are normalized to their maximum values and inserted into a weighted sum. For example, junction temperature is given a weight of 0.8, while volume is given a weight of 0.2; however, other weight distributions are possible and can be included as additional design variables. Taking the minimum value from the array provided by the sum yields an optimal heat sink design with the optimal junction temperature and volume based on the given weights. Table III shows the designed heat sink dimensions for this particular case study.

Once the optimal design is found, MOSFET junction temperature is once again calculated but at different water velocities. Figure 4 shows the junction temperature and water velocity relationship for this fin array configuration. Junction temperature has an upward trend until 0.8 m/s water velocity. At this water velocity, maximum power generation and therefore, loss is achieved. From this point, water velocity increases, but power loss remains the same, leading to a decrease in junction temperature. For this conservative design, the maximum MOSFET temperature occurs at 0.82 m/s with a value of 86.84 °C, well within the allowable temperature range for SiC power MOSFETs.

Next, the influence of water-related corrosion and aging is considered within the model. Corrosion rates for aluminum are approximated using a similar approach to [19] and [20]. Due to the lack of literature on aquatic organic matter accumulation rates, it is assumed that the accumulation rate is about twenty times greater than the corrosion rate. Furthermore, a lack of information regarding the thermal properties of organic sea matter led to the assumption that its thermal properties could be approximated using other organic materials. In the case of this simulation, it was assumed that the thermal properties of organic matter, taken from [18], can perform as an analog for sea matter. The added conduction resistance due to aging is calculated using (12).

$$K_{avg} = \frac{A_{al}}{A_{tot}}K_{al} + \frac{A_{ox}}{A_{tot}}K_{ox} + \frac{A_{ac}}{A_{tot}}K_{ac} \qquad (12)$$

Where:

- $A_{tot}$ = Total fin cross-sectional area
- $A_{al}$ = Fin cross-sectional area composed of aluminum

TABLE III: Heat Sink Dimensions

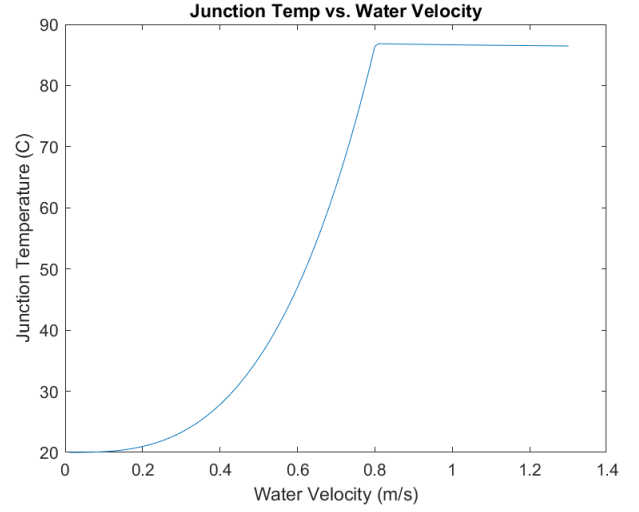| Fin Height | Fin Pitch | Fin Width | Fin Length | Total Width | Number of Fins |
|---|---|---|---|---|---|
| 9 mm | 2 mm | 2 mm | 60 mm | 90 mm | 22 |



Fig. 4: Junction temperature vs. water velocity for a ducted turbine with a contraction ratio of 1.33:1.

- $A_{ox}$ = Fin cross-sectional area composed of the oxidation layer
- $A_{ac}$ = Fin cross-sectional area composed of aluminum
- $K_{al}$ = Thermal conductivity of accumulated organic matter
- $K_{ox}$ = Thermal conductivity of the oxidation layer
- $K_{ac}$ = Thermal conductivity of accumulated organic matter

This equation (12) performs a superposition of the three thermal conductivities and provides an averaged conductivity to use in (5). Again, the thermal conductivity of the fin array is calculated using (8) and (9), then the aged junction temperature can be found. Figure 5 depicts the results of the aged simulation, comparing the new fin array with simulations
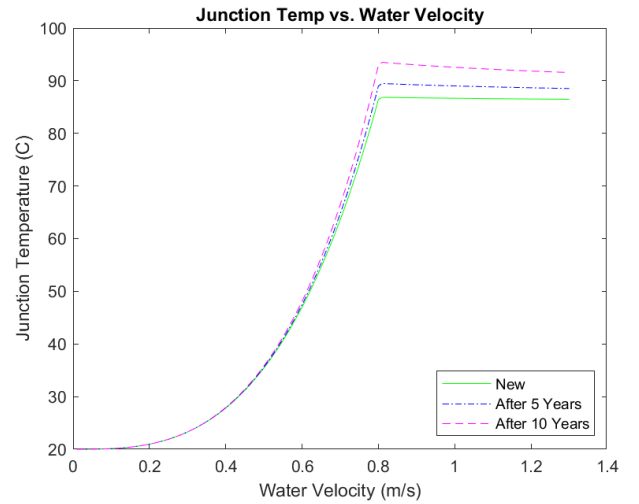


Fig. 5: Aging effects on junction temperature vs. water velocity for a ducted turbine with a contraction ratio of 1.33:1.
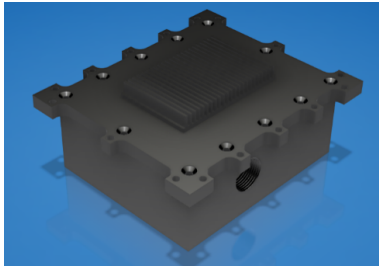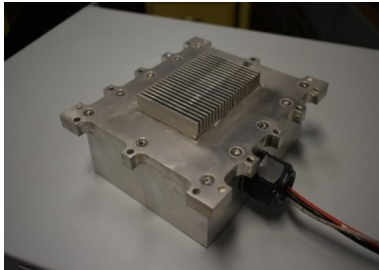
Fig. 6: The enclosure in Fusion 360.



Fig. 7: Enclosure manufactured from Aluminum 6061.

at 5 and 10 years of aging. It is evident by the relation that as the array ages that conduction resistance becomes more prominent within the heatsink, causing the final steady-state temperature to shift higher.

## IV. HARDWARE EXPERIMENT

Once initial modeling was complete, the design was recreated as a 3D model for machining. To minimize leaks, the enclosure consists of just two major physical parts. The first is the lower enclosure, which features 4 mm bolt holes tapped into the bottom of the enclosure to allow circuit boards to be mounted and a 3/4" NPT tapped hole on the side for a cord grip. Bolts that connect the lid to the lower enclosure are screwed into these 5 mm tapped holes, while the 1/16" O-ring groove along the top seals the gap between the lid and lower enclosure. All walls of the enclosure are 1/2" to allow for the 4mm tapped holes and clearance between the 5mm holes and O-ring groove. The top of the enclosure features the fin array, with 2mm spacing and 2mm width. This fin array is raised

compared to the rest of the lid to allow additional clearance for 4mm mounting holes below the fins. Additionally, this stand-off allows the fins to be lined up within the experimental setup easier. Countersunk 5mm bolt holes allow the lid to be attached to the lower enclosure without impeding fluid flow. The outer ears on the lid are given 5mm clearance holes to allow the enclosure to be mounted to the experimental test setup. A lip is milled near the lid's perimeter on the bottom side to allow for easier alignment with the lower enclosure. The fusion model is shown in Figure 6. The final actual enclosure is machined from Aluminum 6061 and presented in Figure 7.

A flow tank is created to test the design. Its primary purpose is to house the water and provide the flow needed to test the accuracy of the modeled heatsink. A constant speed sump pump creates the flow needed within the tank. This pump has a maximum flow rate of 46 GPM. From the pump, water flows upward to a tee valve. The valve allows for manual adjustment of the flow rate through the system. One outlet dumps water back into the tank while the other continues through the test system. After the valve, the water within the test system flows to a flowmeter. The flow meter allows for an accurate flow rate readout up to 60 GPM. From here, the water flows into a channel of known width. This channel has the heat sink enclosure mounted through its bottom, allowing water to flow through the fins. Once the water flows through the channel, it is dumped back into the tank to be recirculated. Figure 8a, 8b and 8c show the complete flow tank.

Attached to the heat sink, a 1 $\Omega$, TO-247 packaged power resistor is used to mimic the controllable varying power losses for a MOSFET. As the test proceeds, the water flow rate is controlled in 5 GPM increments. These numbers are converted to meters per second using the cross-section of the submerged area within the water channel. The equivalent power loss of the MOSFET is calculated at each velocity, and the voltage is adjusted on a DC power supply to replicate the power loss within the resistor. The case and ambient water temperatures are measured using thermocouples at each of these intervals. The equivalent junction temperature is then calculated using the averaged junction-to-case thermal resistance. The model parameters are adjusted to match the conditions within the testing environment.



(a) Experimental flow tank set up.
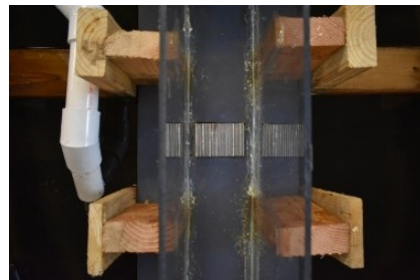


(b) Flow channel with heat sink mounted (Birdseye view).
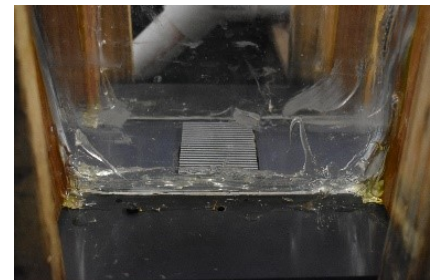


(c) Flow channel with heat sink mounted (Side view).
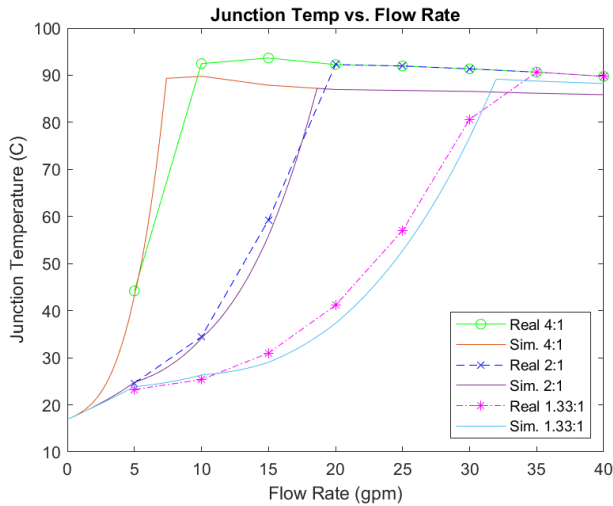
Fig. 8: Experimental flow tank setup.

Fig. 9: Comparison of experimental & simulation results.



Fig. 10: Experimental & simulation results comparison with contact resistance.

Comparing the modeled temperature with the actual temperature presented in Figure 9 yields some differences between the two. It is evident that they both follow the same general trends with flow rate, but there is a constant difference. This temperature difference is likely due to an omitted thermal resistance somewhere within the thermal circuit. This hypothesis is supported by the fact that the temperature error is depend on the flow rate, which is proportional to the MOSFET power loss. With that in mind, the model was revised.

Initially, the thermal contact resistance was not modeled, which can institute a large amount of additional thermal resistance. This is approximated by adding the thermal grease's thermal resistance used to coat the interface material. The model was rerun with the new resistance added, and a new comparison is provided in Figure 10. With the thermal grease accounted for, the model offers a significantly more accurate approximation of the junction temperature. With the added resistance, the maximum error is now 6.5%, with an average error of around 2.5%. This modeling change results in reasonable estimate of the thermal performance of the system.

Future works largely include improvement of the design. CFD could be used in order to provide a more accurate flow regime through the fin array. This would further improve the accuracy of the thermal model. A CFD model could also be used to improve the fin geometry itself. Further tests could be conducted with multiple MOSFETs to ensure that the devices stay within the allowable temperature range. Lastly, thermal contact resistance could be empirically measured in order to maximize the accuracy of the mathematical model.

## V. CONCLUSION

This paper demonstrated the design of a fin array heat sink for SiC MOSFET to be used in hydrokinetic applications. The work fills a literature gap of aquatic based convective cooling for wide-bandgap switching power electronics. Challenges due to the aquatic environment are considered, namely corrosion and biofouling. The combined SiC MOSFET and heat sink
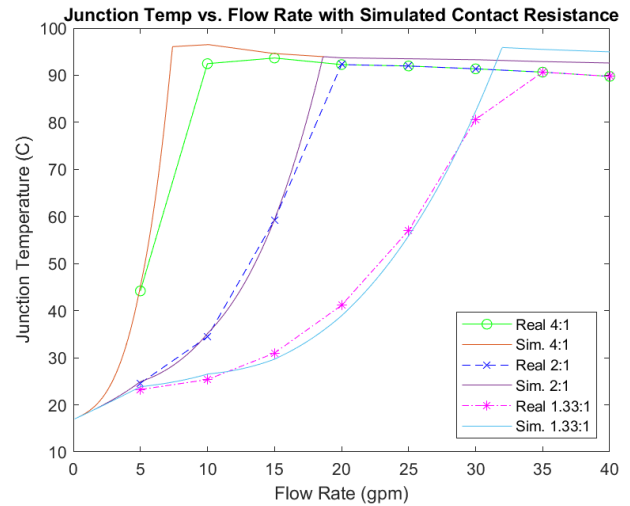
is intended to reduce footprint, costs, and constraints for the hydrokinetic turbines. The paper first walks through power loss and thermal calculations to model the electro-thermal system, and then a physical enclosure and heat sink are designed from the model. Experimental tests are conducted in a customized water tank that enables controlled water current over submerged power electronics and heat sink. Hardware measurements follow the same trend lines as the model simulation. Overall, both simulation and experimental results show effectiveness for maintaining device temperatures under various water flows. A constant error was shown between experimental results and measured temperatures. This was accounted for by adding an additional thermal resistance to mimic the effects of thermal contact resistance.

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