RAMIN JAVADI

Personal Website LinkedIn Google Scholar javadisr@oregonstate.edu
(+1) 541-250-7854 Corvallis, OR, USA

RESEARCH INTERESTS

Mixed-Signal Integrated Circuit Design
High-Speed Wireline/Optical Communication Systems

EDUCATION

Ph.D. in Electrical Electronics Engineering *2021 - Present*
Oregon State University *– OR, USA*

- Thesis: Energy-efficient high-speed wireline communication systems
- GPA: 4.0/4.0

M.Sc. in Electrical Electronics Engineering *2014 - 2017*
University of Tehran *– Tehran, Iran*

- Thesis: Design and implementation of dielectric dissipation factor measurement circuit and system
- GPA: 3.53/4.0

B.Sc. in Electrical Electronics Engineering *2010 - 2014*
Shamsipour Institute of Technology *– Tehran, Iran*

- The institute was founded in 1964 under the supervision of Massachusetts Institute of Technology (MIT) advisers, and by that time was named "American College"
- GPA: 3.8/4.0 *(Ranked 1st among all B.Sc. students, class of 2010)*

PUBLICATIONS

1. **R. Javadi** and T. Anand, "A machine learning-inspired PAM-4 transceiver for medium-reach wireline links," *IEEE Journal of Solid-State Circuits,* 2025. [Under Review]

2. **R. Javadi**, X. Lin and T. Anand, "A 3.2pJ/b 0.068pJ/b/dB 25Gb/s NRZ wireline transceiver with 3-tap FFE and random forest classification for compensating 47dB loss in 16nm FinFET," in *Proc. Symp. on VLSI Technology and Circuits,* 2025.

3. **R. Javadi** and T. Anand, "A 0.055pJ/bit/dB 42Gb/s PAM-4 wireline transceiver with consecutive symbol to center (CSC) encoding and classification for 26dB loss in 16nm FinFET," in *Proc. IEEE Custom Integ. Circuits Conf. (CICC),* 2025.

☆ *This design helps to reduce the energy consumption of data centers for artificial intelligence (AI) by 50% and is selected as the Best Student Paper Award winner at the prestigious IEEE CICC 2025. Owing to the impact of this research, it has been featured by national and international Media outlets such as: ScienceDaily, Forbes, Dailyexe, ScienceReader, Oregon State University, Columbia University, KGW-TV (NBC affiliated), KATU-TV (ABC affiliated), Knowridge, GlobalEnergyPrize, SemiEngineering, Securities, Theoutpost, Flickr, TechXplore, EurekAlert, etc.*

4. **R. Javadi** and T. Anand, "An enhanced eye-opening PAM-4 with encoding for short-reach wireline communication systems," in *Proc. IEEE 67th Int. Midwest Symp. on Circuits and Systems (MWSCAS),* 2024.

5. A. Ensinger, **R. Javadi**, X. Lin, B. Bose and T. Anand, "Minimum power point design of inverter based continuous time linear equalizer (CTLE)," in *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS),* 2024.

SKILLS

IC Design Technology Node: Intel 16nm FinFET, TSMC 65nm CMOS

CAD and Simulation: Cadence Virtuoso, H-SPICE, PSPICE, Keil

PCB Design Tools: Altium Designer

Programming: C, MATLAB, Verilog, Python

FPGA: AMD-Xilinx Artix UltraScale+, XEM8320 (XCAU25P)

Microcontrollers: ARM, AVR

WORK EXPERIENCE

Research Scholar *2022 - Present*

Semiconductor Research Corporation (SRC) *– Center for Ubiquitous Connectivity (CUbiC), NY, USA*

- Machine learning-inspired high-speed links architectures

Graduate Research / Teaching Assistant *2021 - Present*

Oregon State University *– Corvallis, OR, USA*

- Energy efficient high-speed wireline communication systems, Mixed-signal IC design

Research and Development (R&D) Design Engineer *2018 - 2021*

TOSAN (Manufacturer of Neonatal Systems, Medical) *– Tehran, Iran*

- Analog and digital circuit design, Microcontroller programming

University Instructor *2017 - 2018*

Shamsipour Institute of Technology *– Tehran, Iran*

- Electrical fundamental, Electronics, Digital circuits

SELECTED PROJECTS

- Low power wide tuning range phase-locked loop (PLL) in 22nm FinFET
- Design and simulation of 6th-order elliptic switch capacitor filter
- Design and simulation of a 10-bit 40MHz pipelined ADC in 180nm CMOS
- Design and simulation of various operational transconductance amplifiers (OTAs) with diverse specifications in 180nm, 130nm, and 65nm CMOS technologies
- Design and implementation of main control circuit for infant phototherapy & radiant warmer based on general and particular standards requirement and EMC compliances

ACCOMPLISHMENTS

- Recipient of the prestigious 2025 IEEE Custom Integrated Circuits Conference (CICC) Best Student Paper Award
- Peer Reviewer, IEEE International Midwest Symposium on Circuits and Systems
- Ranked 1st among all B.Sc. students in Electrical Electronics Engineering, class of 2010
- Ranked 10th in the National University Entrance Exam (B.Sc. 2010)
- Achieved top 1% rank in the National University Entrance Exam (M.Sc. 2014)

REFERENCES

- Prof. Tejasvi Anand, Associate Professor, Department of EECS, Oregon State University – anandt@oregonstate.edu
- Prof. Gabor Temes, Professor, Department of EECS, Oregon State University – gabor.temes@oregonstate.edu
- Prof. Un-Ku Moon, Professor, Department of EECS, Oregon State University – moon@eecs.oregonstate.edu