CMOS Integrated Circuits II
Project

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Contents

1 Project Overview

The objective is to design and layout a fully-differential operational amplifier in the 0.18um process with the following specifications:

- Power supply: V_{DD} = 1.8V, 1.7V, 1.9V (TT, SS, FF)
- Load at each output: C_{load} = 2pF (to be affected by TT, SS, FF)
- Loop gain: > 70 dB
- Loop UGBW: > 90 MHz
- Loop phase margin: > 60deg
- CMFB phase margin: > 60deg
- CM accuracy (with no differential signal): < ±0.05V
- Output swing (70% linear of either +/- node): > 1.2V peak-to-peak differential
- Power consumption (including bias): < 8mW

LVS: Passed
DRC: Passed

Name	Spec	Slow	Typical	Fast
Power supply [V]	VDD	1.7	1.8	1.9
Reference CM [V]	VCM	0.9	0.9	0.9
Reference current [uA]	IREF	40	40	40
Temperature [C]	-	85	27	-40
Loop gain [dB]	> 70	78.2	75.8	75.2
Loop UGBW [MHz]	> 90	101.9	136.4	199.1
Loop PM [deg]	> 60	66.9	65.1	61.8
CMFB PM [Deg]	> 60	62.1	63.2	62.4
CM accuracy [mV]	< ±50	-23	13	42
Output swing [$V_{pk\text{-}pk}$]	> 1.2	2.24	2.38	2.55
Power [mW]	< 8	4.47	4.85	5.30

Table 1: Specifications and Results

2 Schematics

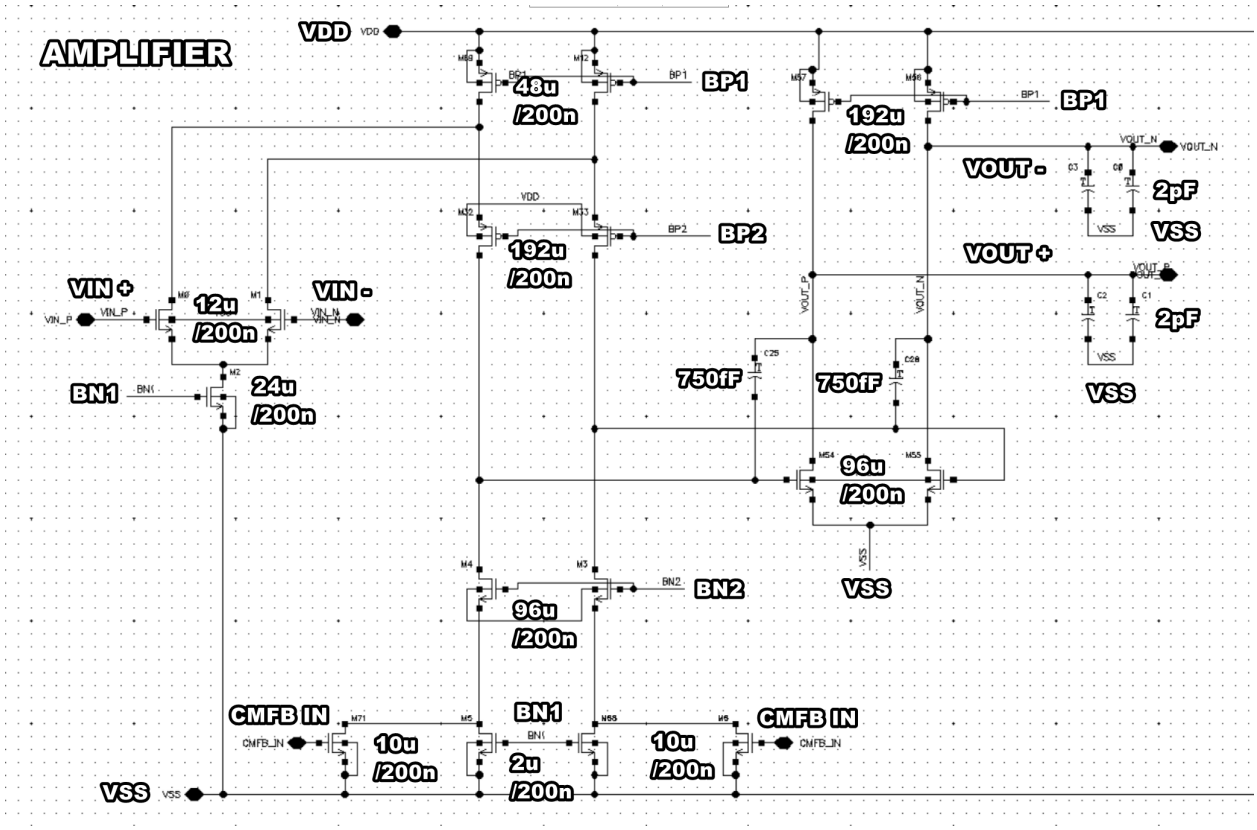

Figure 1: Amplifier Schematic

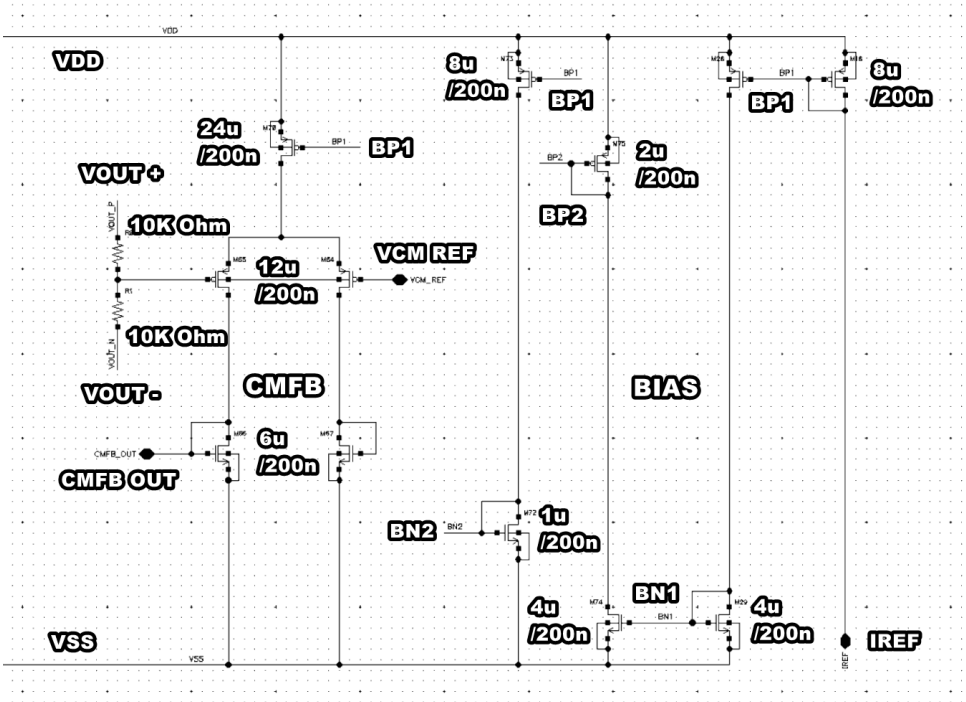

Figure 2: CMFB and Bias Schematic

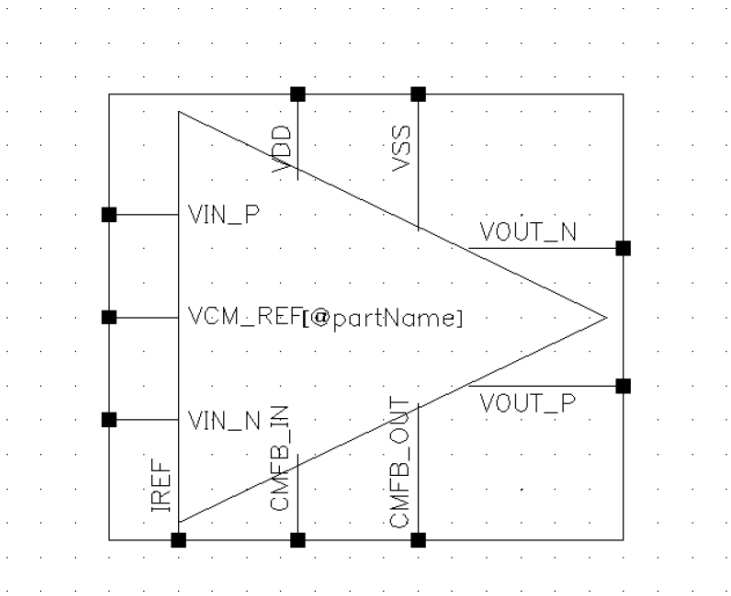

Figure 3: Op-Amp Symbol

3 Simulation Results

3.1 Differential Loop

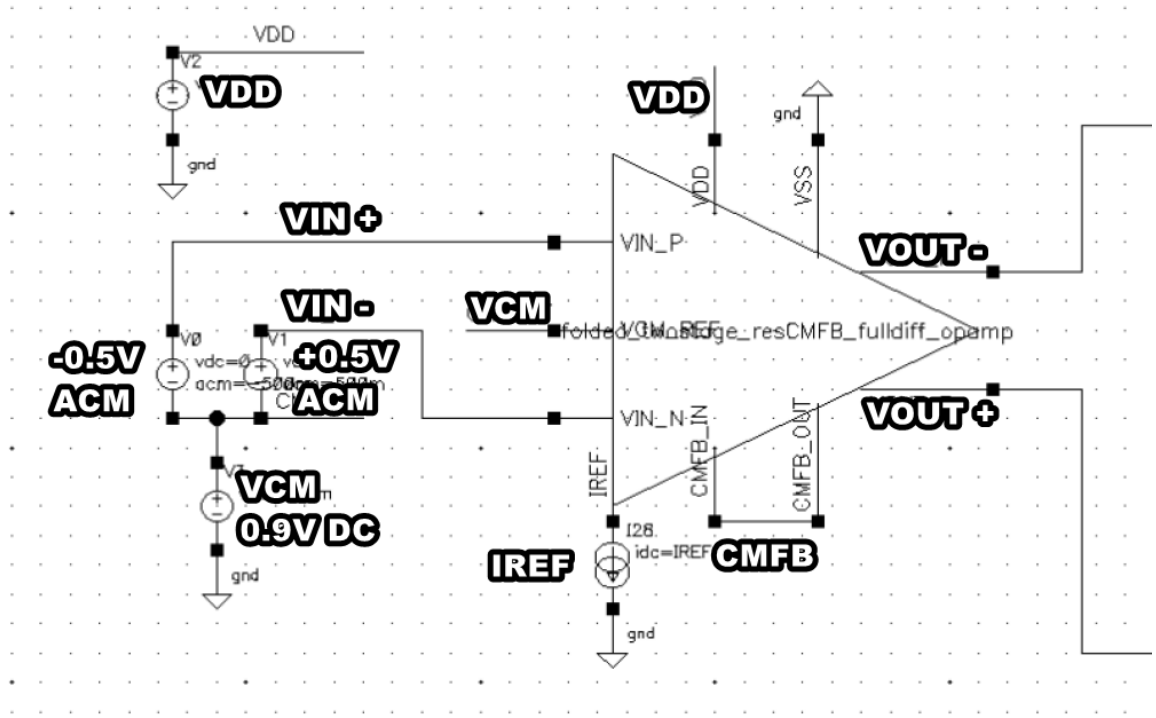

Figure 4: Differential Loop Testbench (1 of 2)

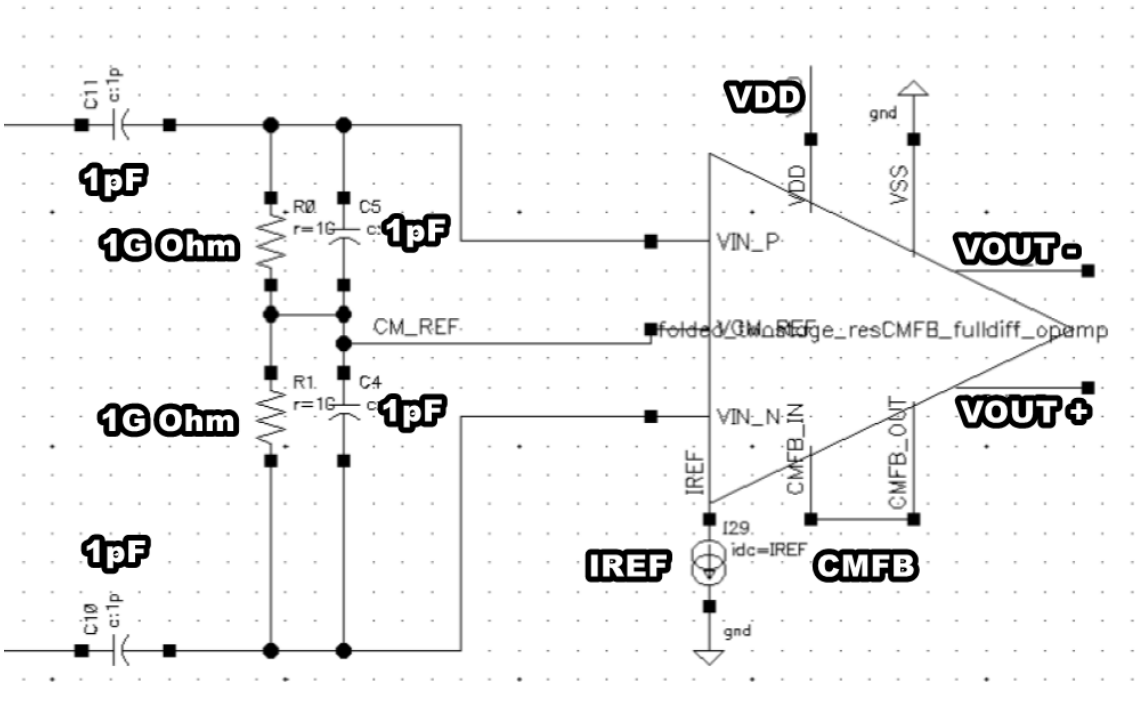

Figure 5: Differential Loop Testbench (2 of 2)

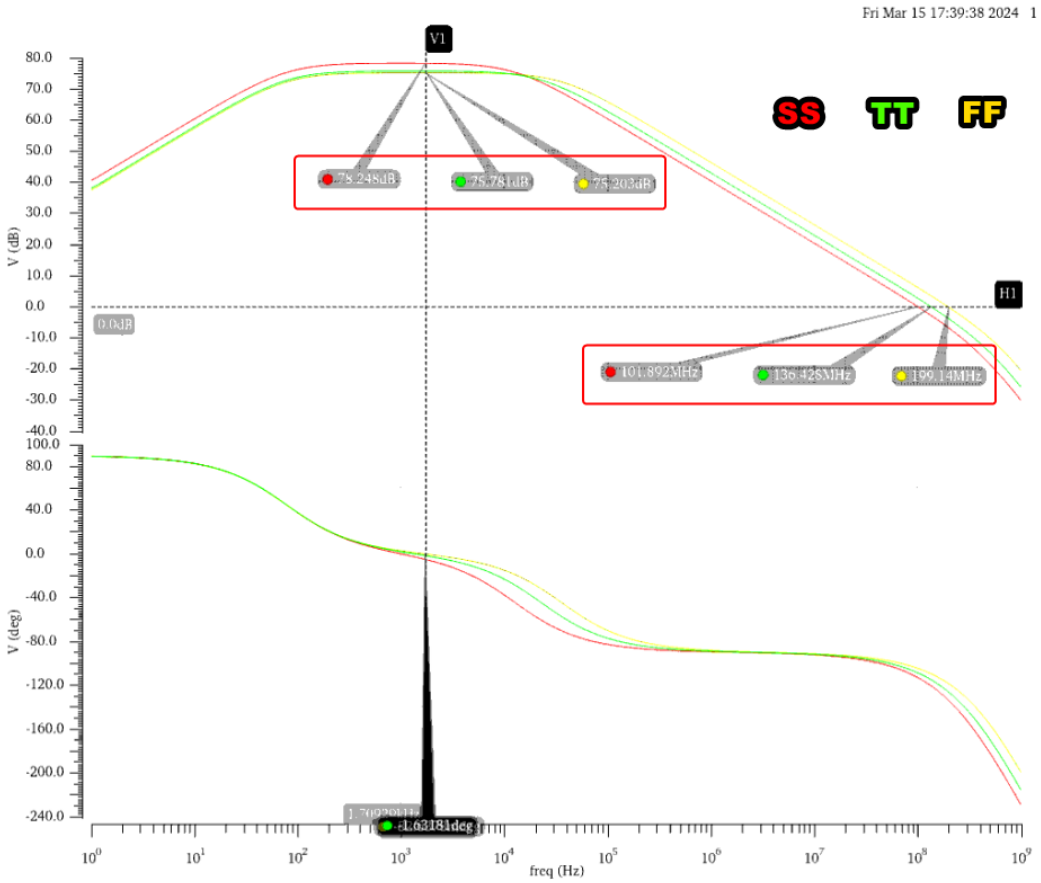

Figure 6: Differential Loop Gain and Phase

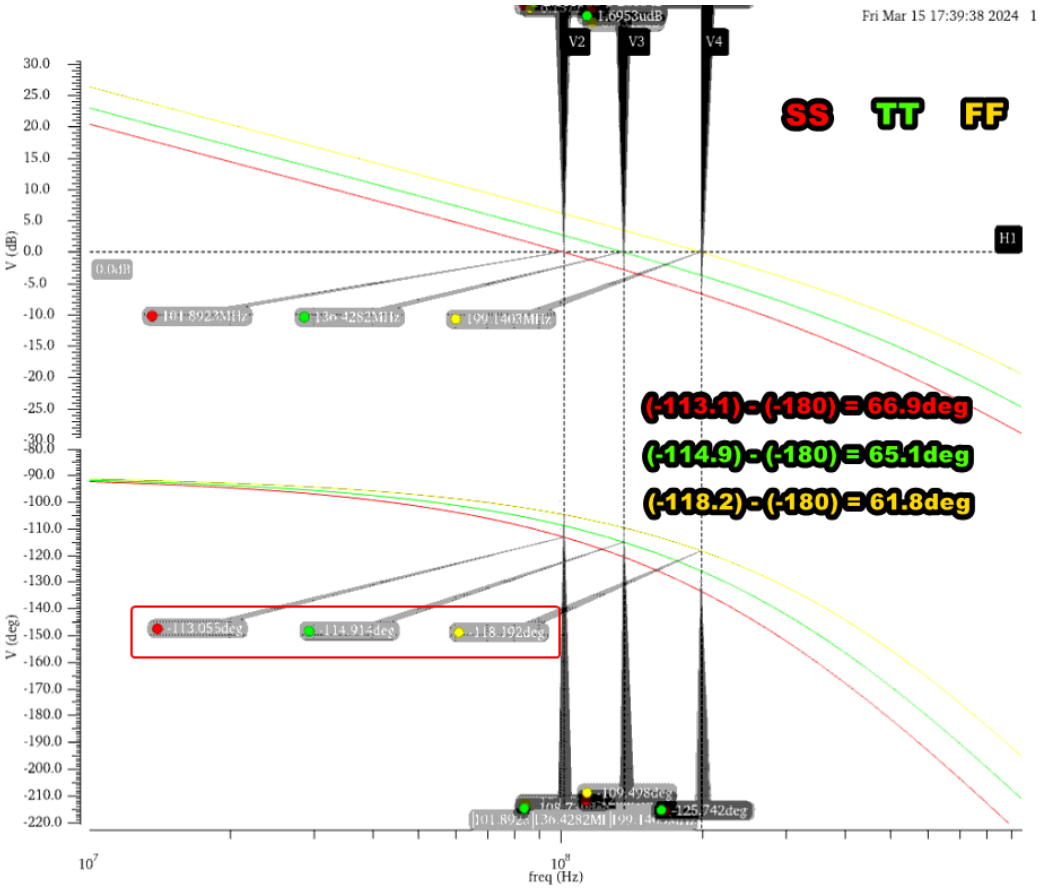

Figure 7: Differential Loop Phase Margin

3.2 CMFB Loop

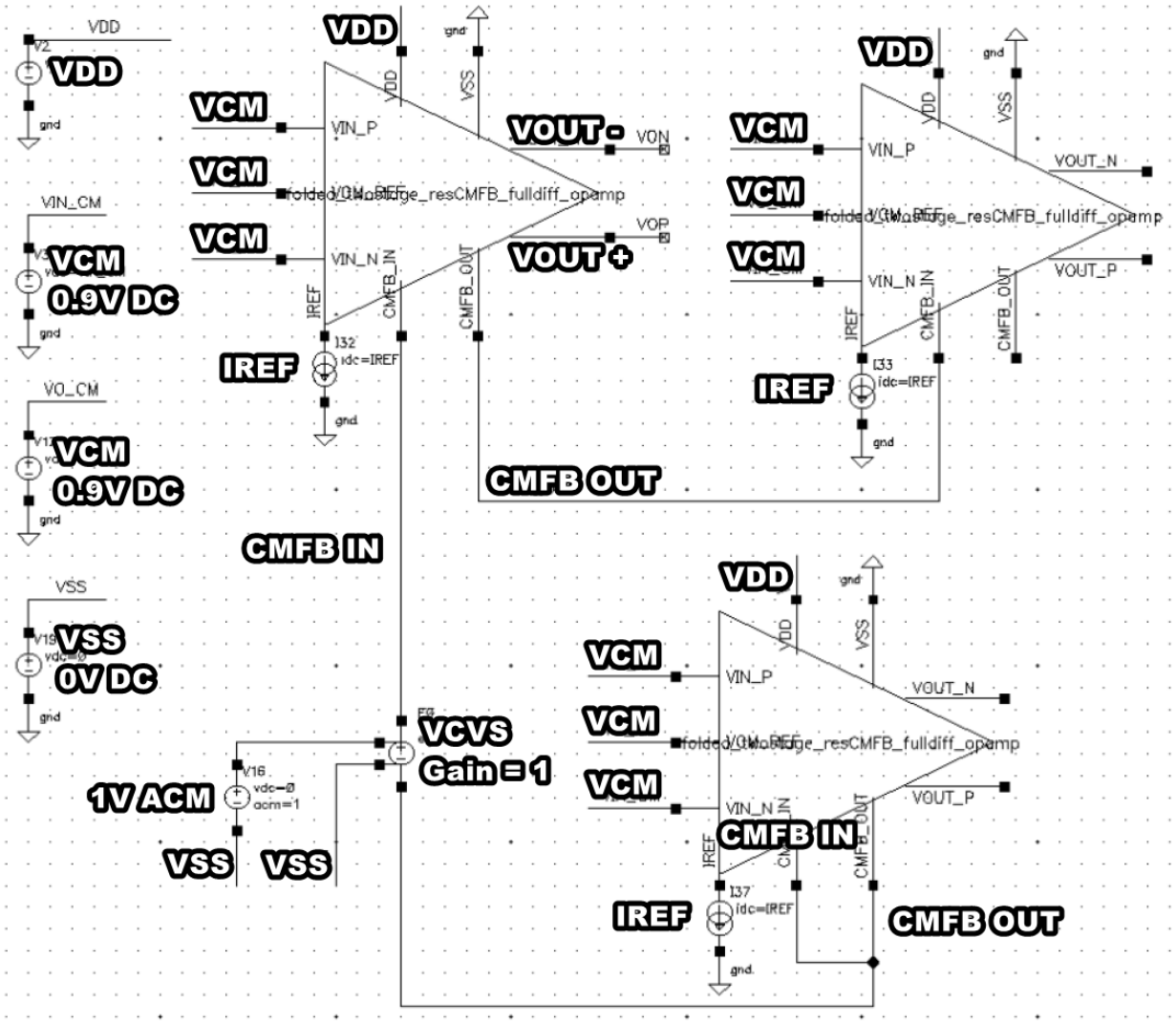

Figure 8: CMFB Loop Testbench

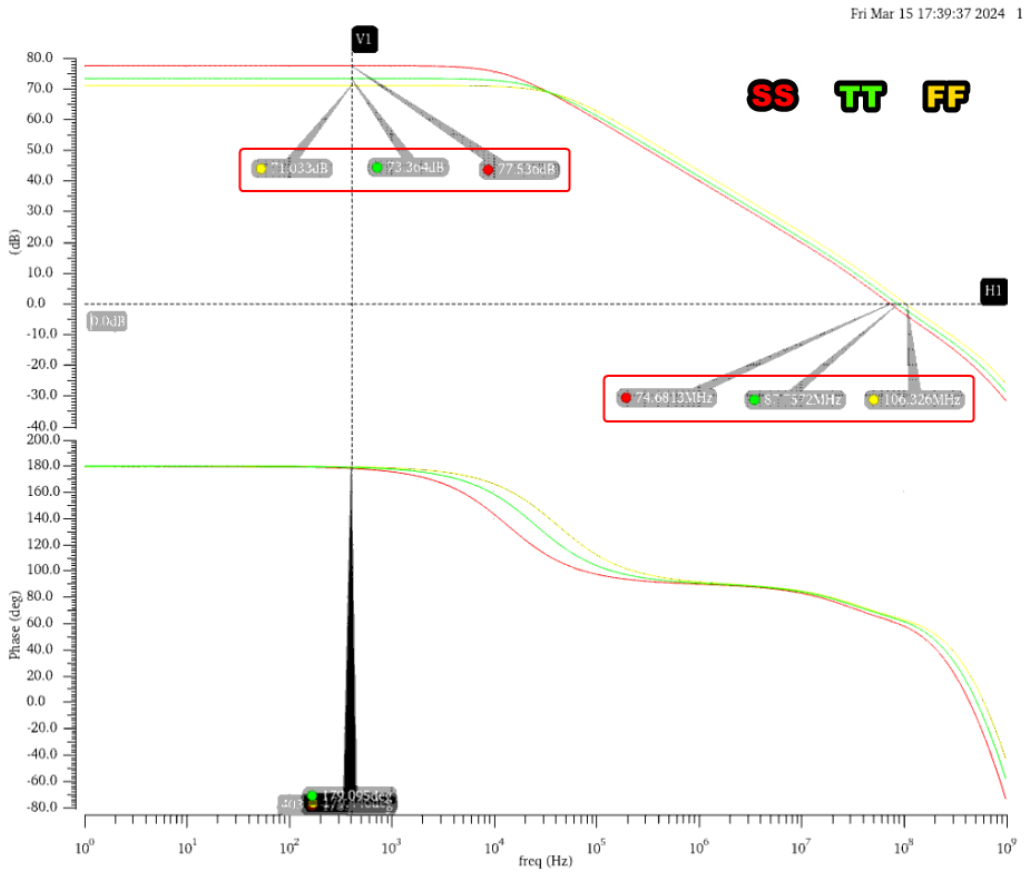

Figure 9: CMFB Gain and Phase

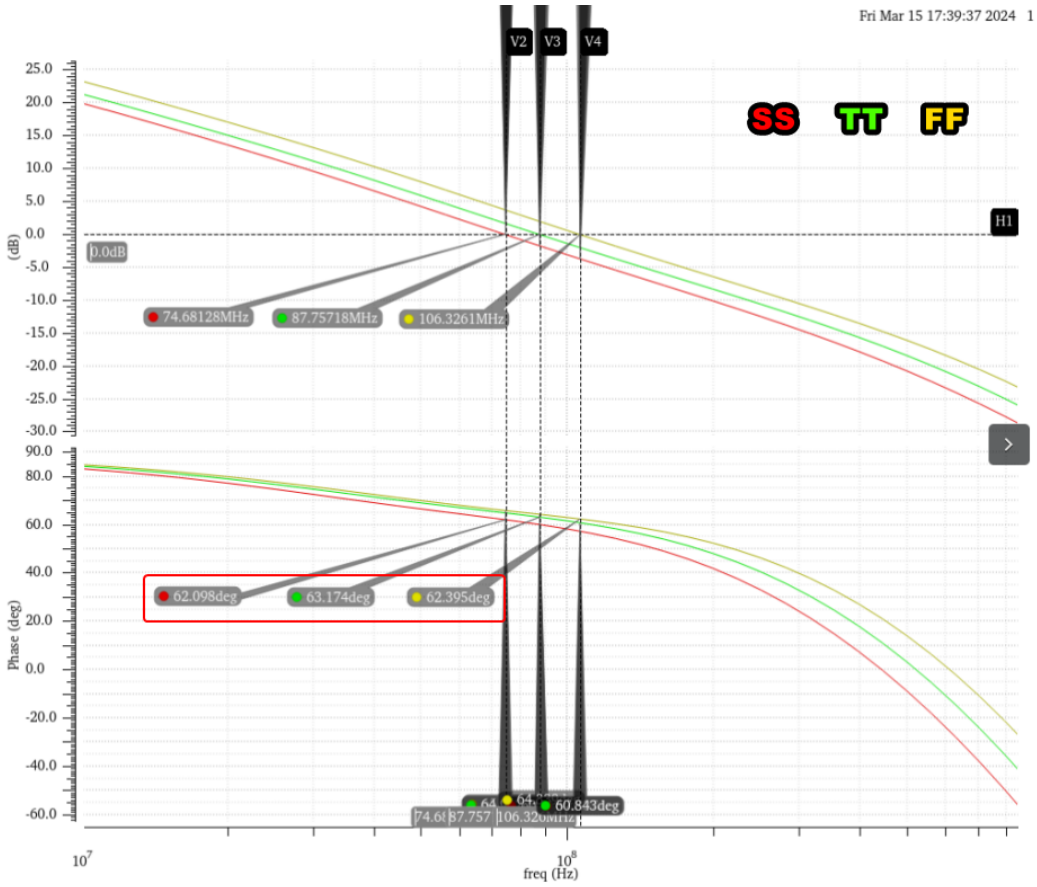

Figure 10: CMFB Phase Margin

3.3 DC & Output Swing

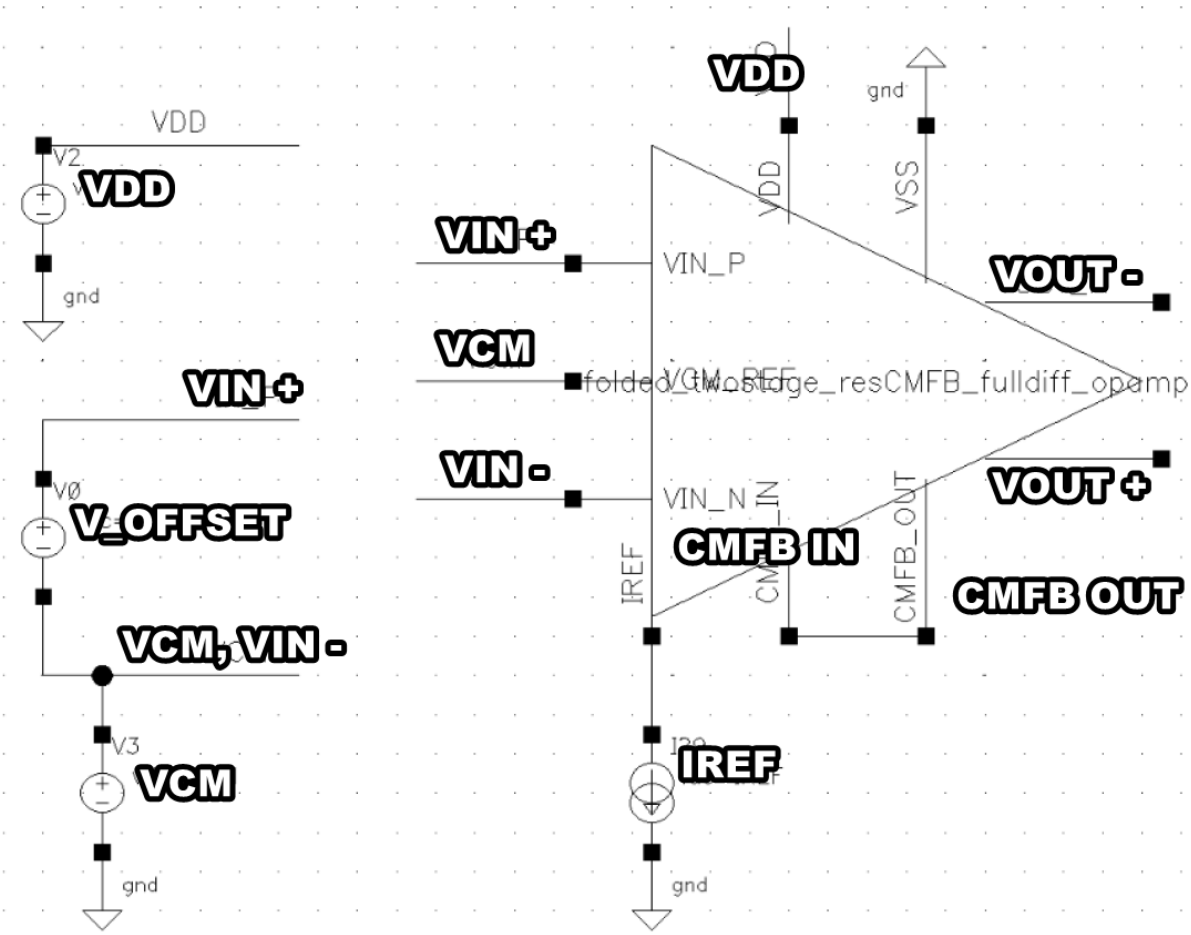

Figure 11: DC & Output Swing Testbench

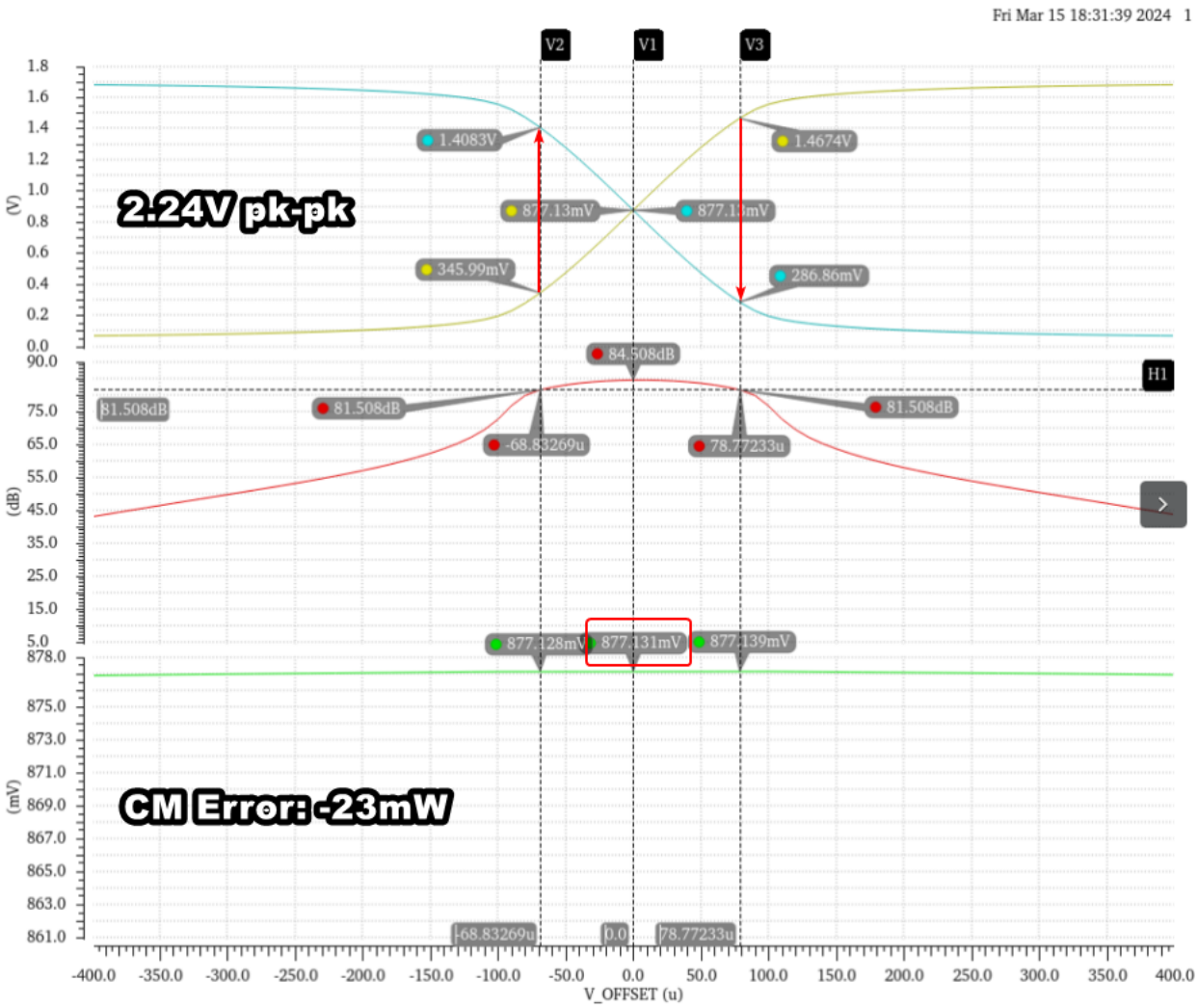

Figure 12: SS Output Swing & CM Accuracy

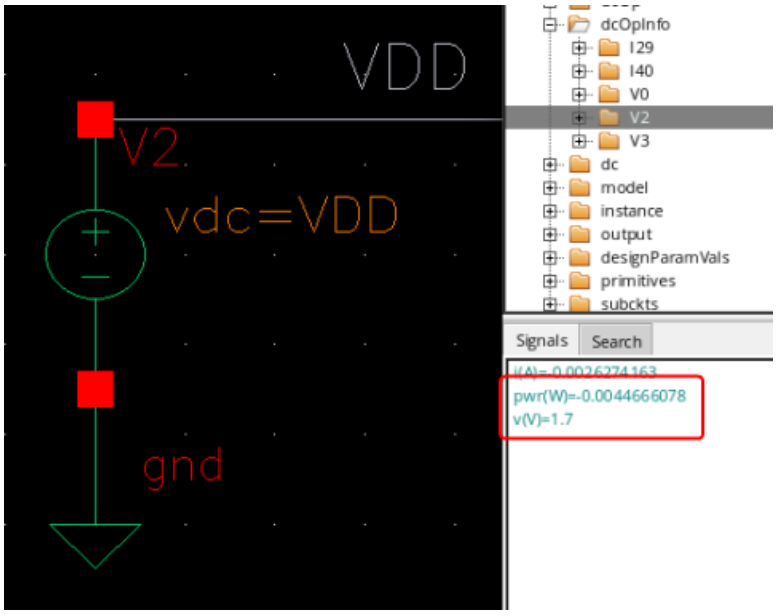

Figure 13: SS Power Consumption

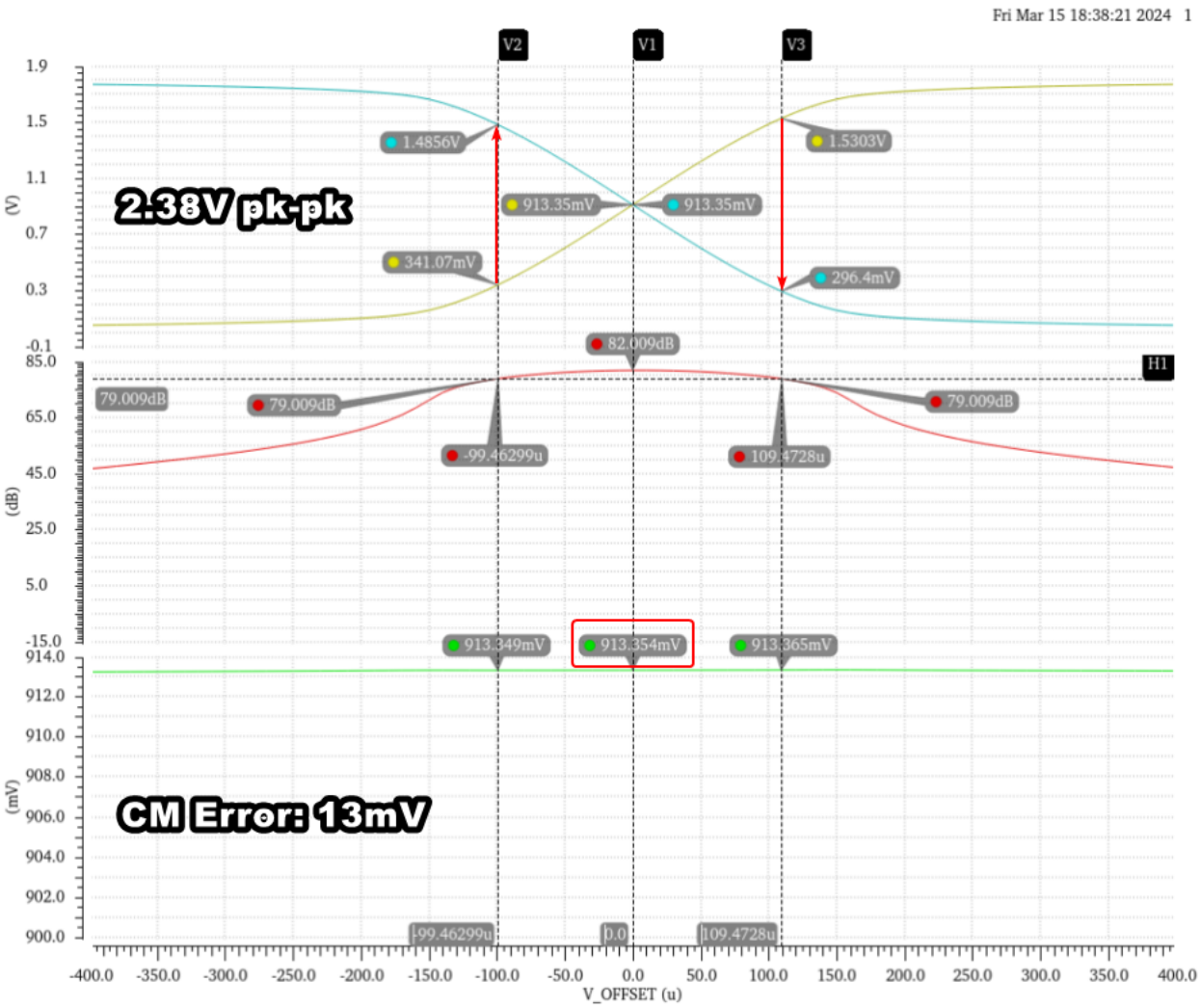

Figure 14: TT Output Swing & CM Accuracy

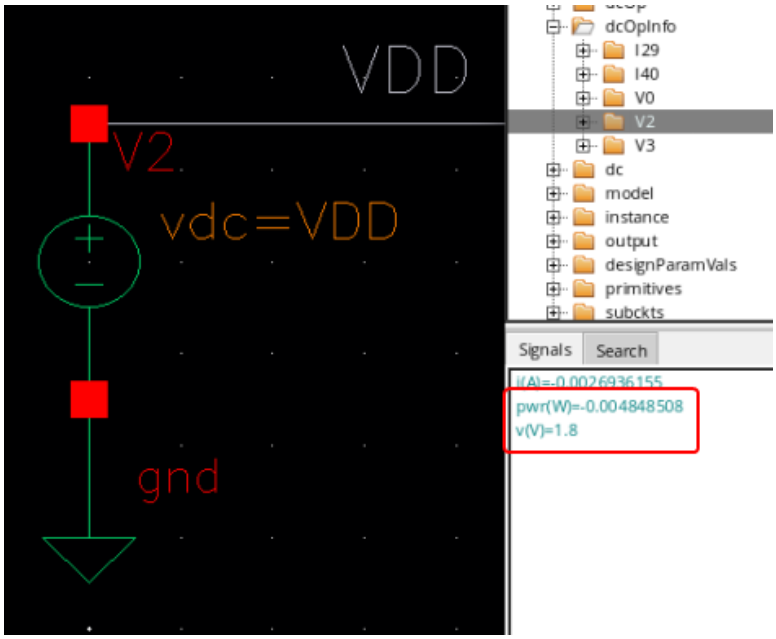

Figure 15: TT Power Consumption

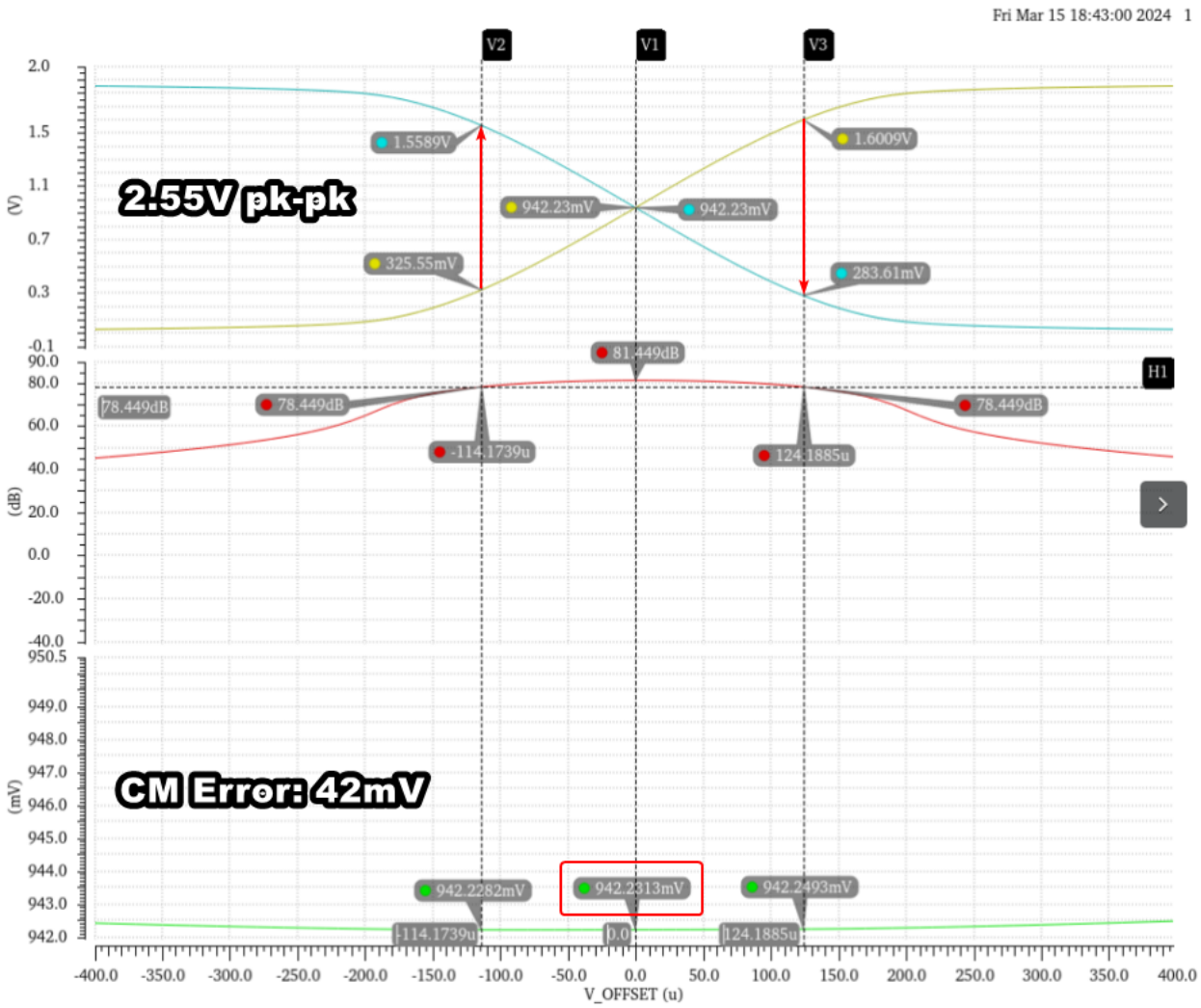

Figure 16: FF Output Swing & CM Accuracy

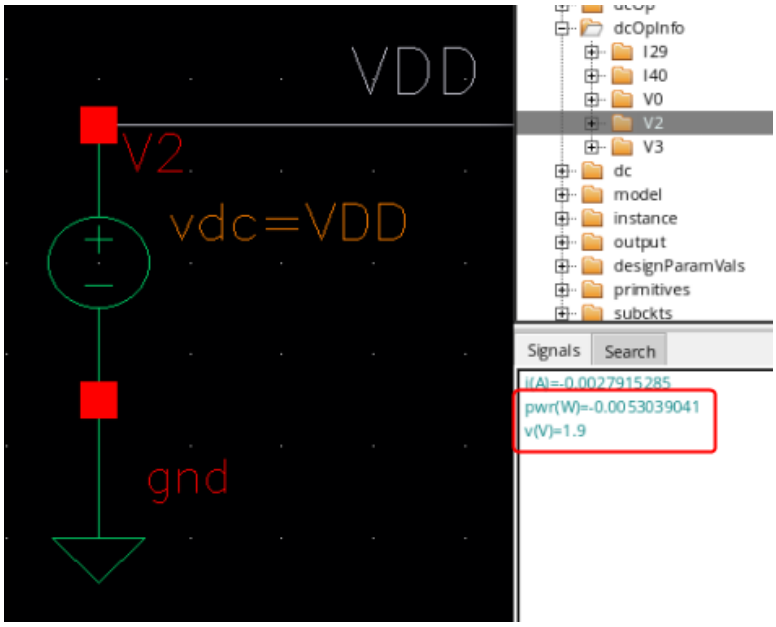

Figure 17: FF Power Consumption

4 Layout

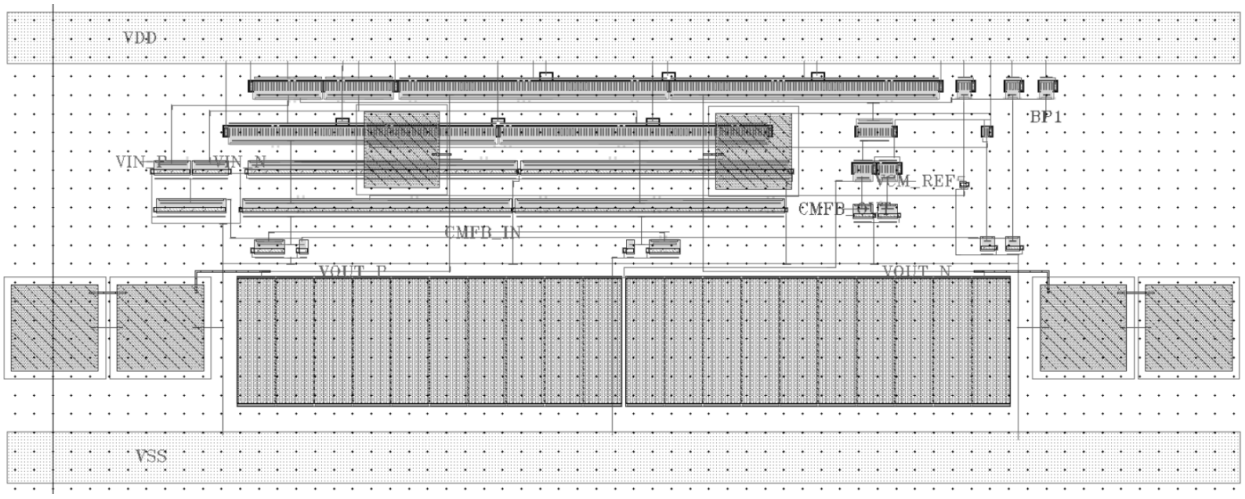

Figure 18: Layout

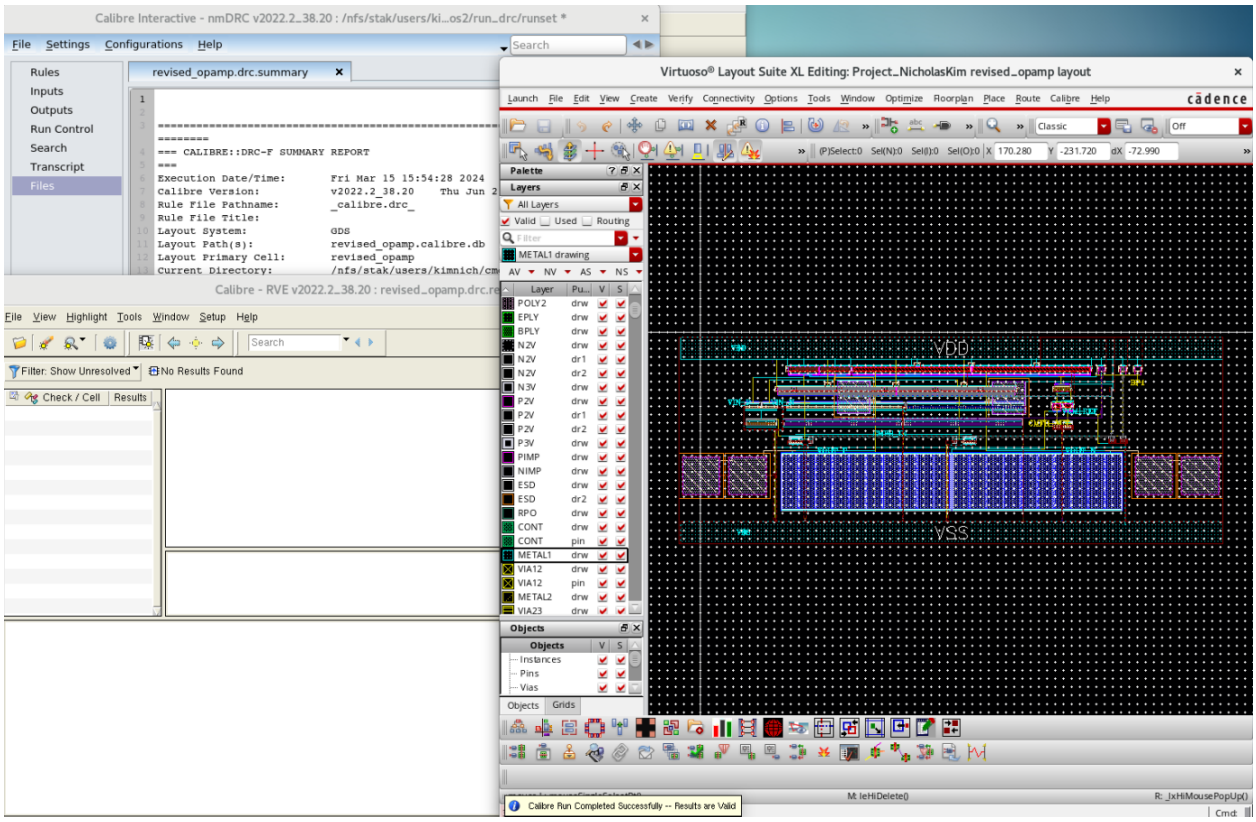

Figure 19: DRC Result

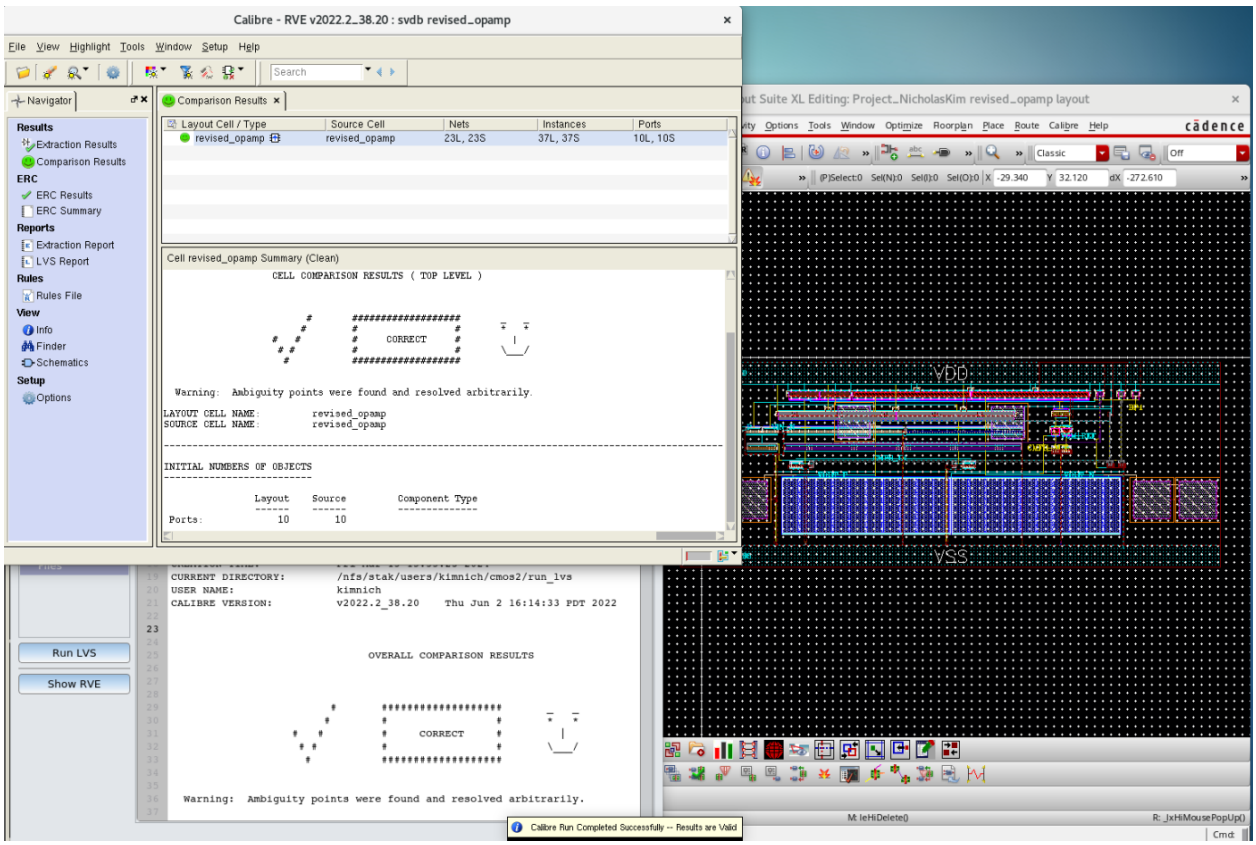

Figure 20: LVS Result