CMOS Integrated Circuits I
Operational Amplifier Design Project

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Contents

1 Design Objective

The objective of the project is to design a two-stage single-ended CMOS operational amplifier in the 0.18um process with the following specifications:

- Load capacitance: 4pF
- Power supply: $V_{dd} = 0.9\text{V}$, $V_{ss} = -0.9\text{V}$
- Open-loop gain: $\geq 60\text{dB}$
- Phase margin: $\geq 60^\circ$
- Unity gain frequency: $\geq 12\text{MHz}$

2 Design Process

The first step in the design process was to determine a CMOS configuration that would meet the requirements. This op-amp was implemented with a single-ended differential amplifier followed by a telescopic cascode gain stage.

After calculating the differential gain of the op-amp in terms of gm and r_{ds}, the gm and r_{ds} values were assumed to be equal across all gain stage devices in order to approximate a gm-r_{ds} relationship that would achieve a DC gain well above the requirement.

By setting a gm of 1mS, a transconductance efficiency of 10 for moderate inversion was targeted on all gain stage devices in order to determine an I_d of 0.1mA. In Cadence simulations on isolated NMOS and PMOS devices, an I_d of 0.1mA was set to determine device sizes such that $gm = 1\text{mS}$. The drain-source resistances, channel length modulation parameters, transconductance parameters, and threshold voltages were determined for NMOS and PMOS devices during this step.

The differential amplifier and telescopic cascode are supplied by a current mirror, approximating a current draw of 0.5mA and power consumption of 0.9mW.

Initial calculations and fine-tuning in Cadence simulation determined the bias voltages on the telescopic cascode achieving saturation on all devices with a DC output of $\approx$0V.

The final design choice was to shift the pole frequencies by adding a capacitor across the output and V_{ss} to achieve an appropriate phase margin at $\approx 80^\circ$.

3 Cadence Simulation Results

3.1 Result Tables and Schematics

Requirement	Specification	Simulated Result
Load capacitance	4pF	4pF
Power supply	$V_{dd} = 0.9$V, $V_{ss} = -0.9$V	$V_{dd} = 0.9$V, $V_{ss} = -0.9$V
Open-loop gain	$\geq$ 60dB	73.6dB
Phase margin	$\geq 60°$	80.3°
Unity gain frequency	$\geq$ 12MHz	48.8MHz
Power	N/A	0.878mW

Table 1: Specifications and Simulated Results

Device label	Width	Length	Drain-source current
NM0	3.5µm	180nm	94.4572µA
NM1	3.5µm	180nm	94.4572µA
NM2	3.5µm	180nm	96.581µA
NM3	3.5µm	180nm	96.581µA
PM0	24µm	180nm	193.162µA
PM1	12µm	180nm	94.4572µA
PM2	12µm	180nm	94.4572µA
PM3	12µm	180nm	96.581µA
PM4	12µm	180nm	96.581µA
PM5	12µm	180nm	200µA

Table 2: Device sizes and drain-source currents (see Figure 3)

Node label	DC voltage
V_{dd}	0.9V
V_{ss}	-0.9V
V_1	242.893mV
V_2	356.267mV
V_3	-227.625mV
V_4	-227.625mV
V_5	-300.267mV
V_6	410.267mV
V_{b1}	385mV
V_{b2}	$-250mV$mV
V_{out}	-0.936mV

Table 3: DC voltages at all nodes (refer to Figure 2 node labels)

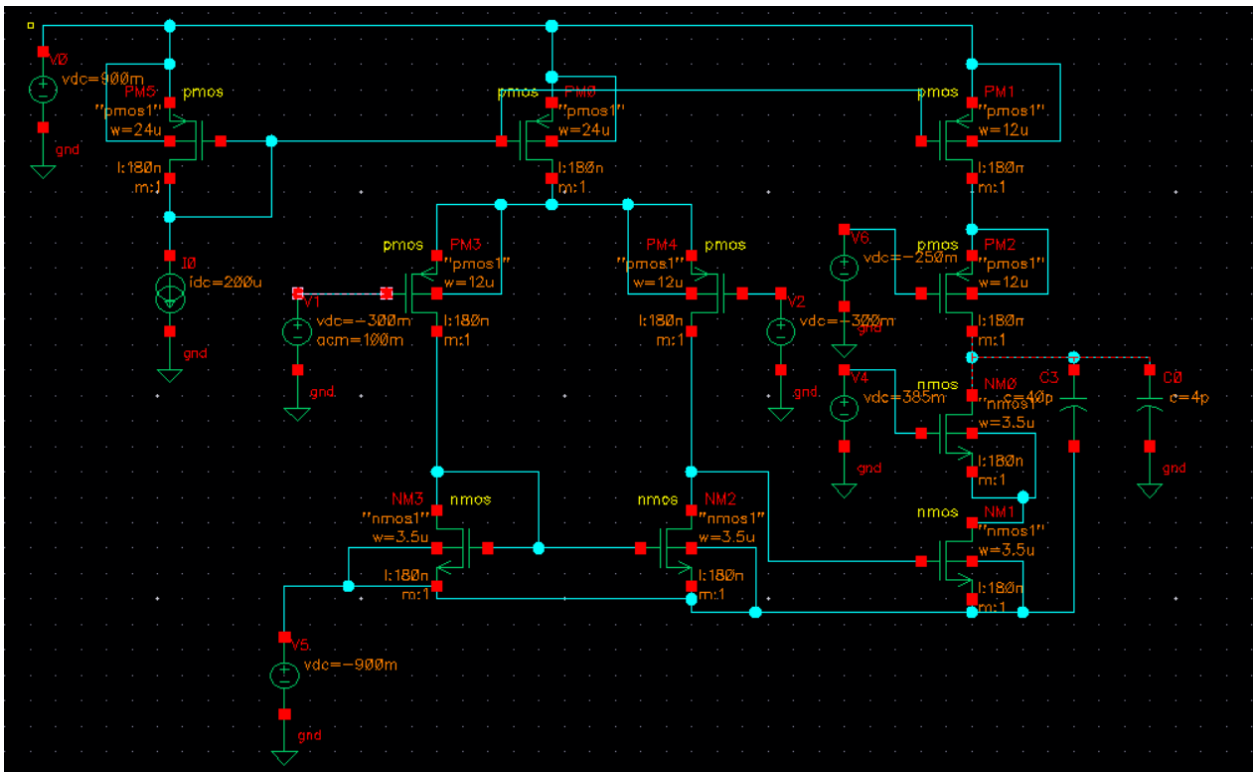

Figure 1: Op-Amp Schematic

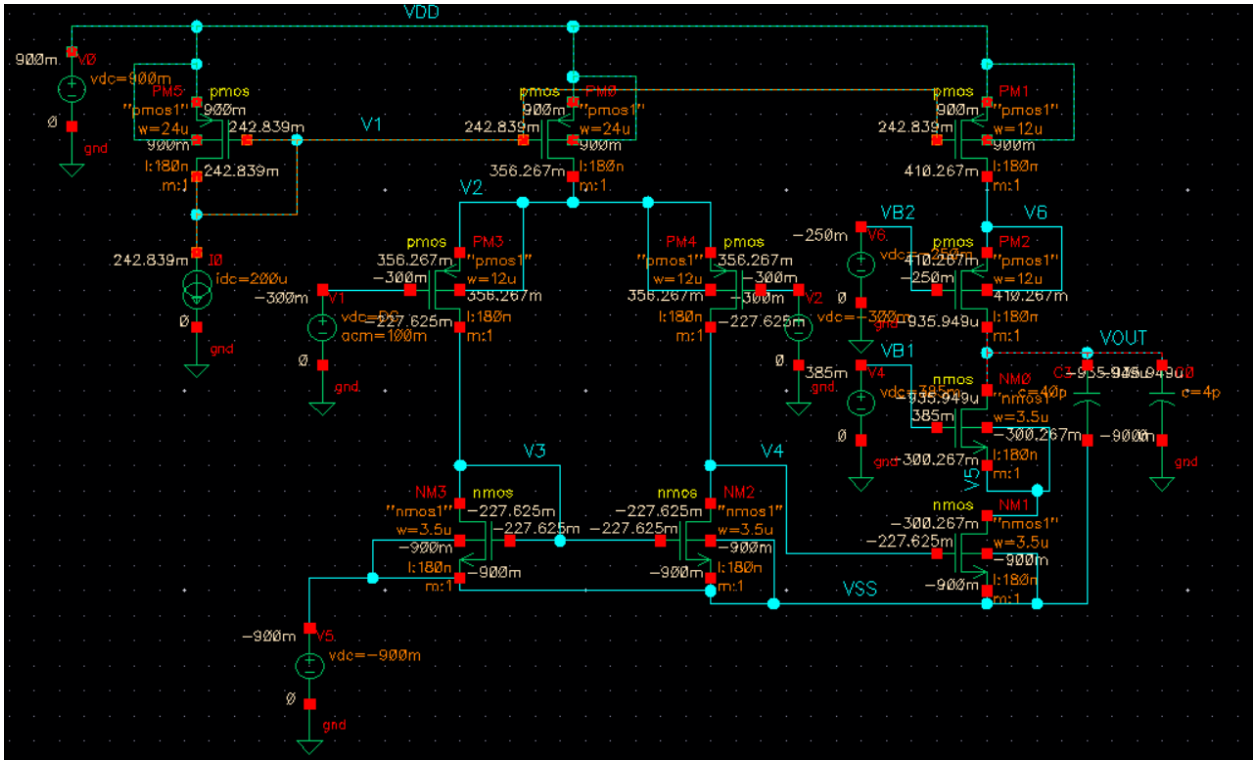

Figure 2: Schematic with Node Voltages

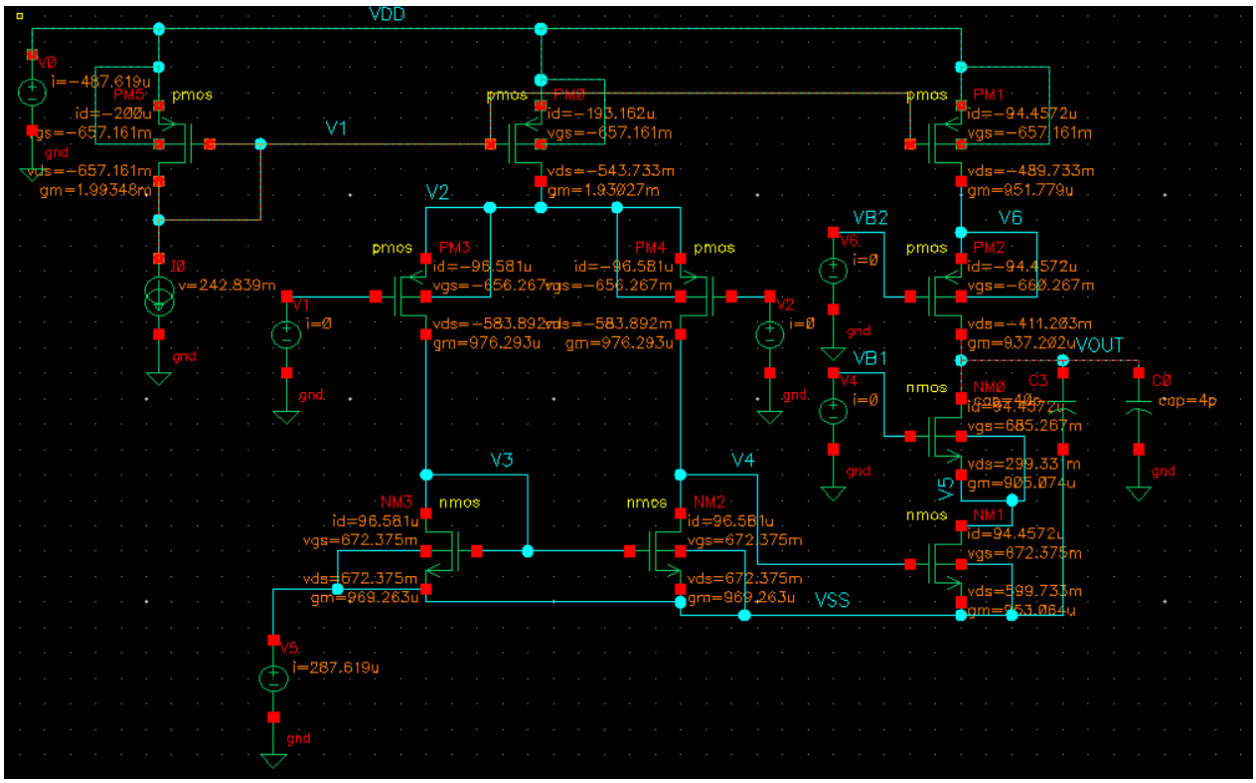

Figure 3: Schematic with Device Currents

3.2 Simulation Plots

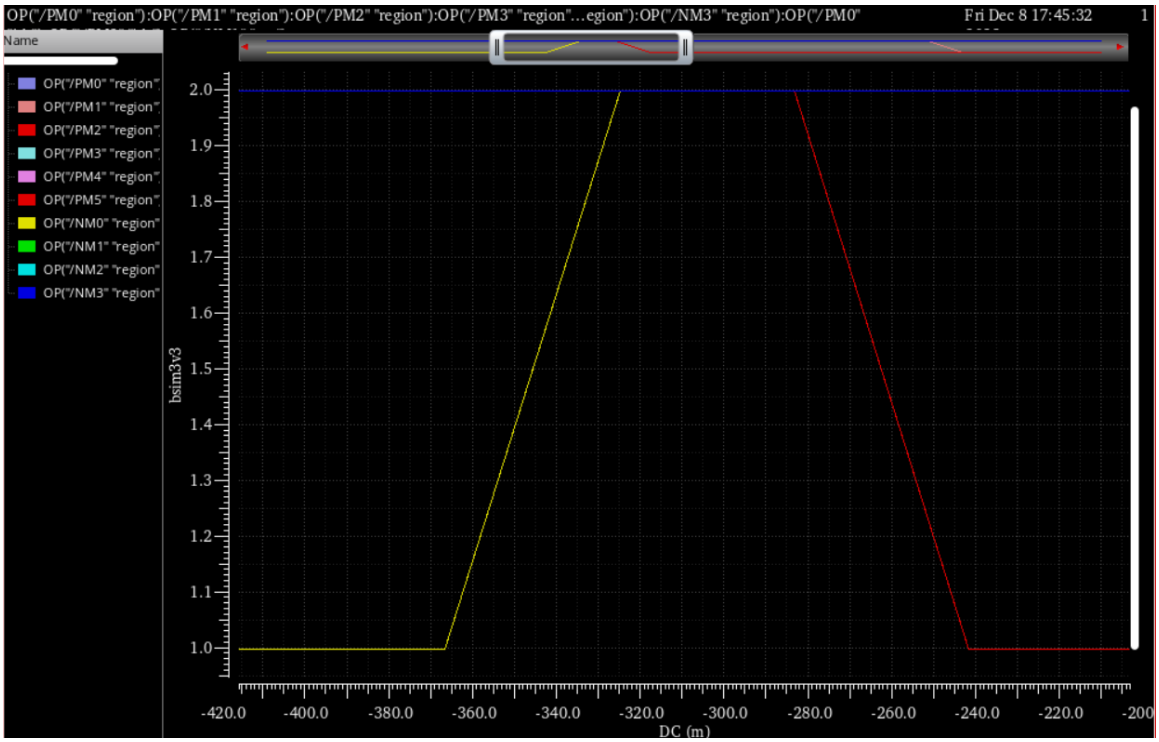

Figure 4: Common-Mode Input Range

Figure 4 is a plot of all transistor regions of operation as a function of the common-mode input voltage. Region 2 indicates saturation. The op-amp has a common-mode input range of approximately −325mV to −285mV.

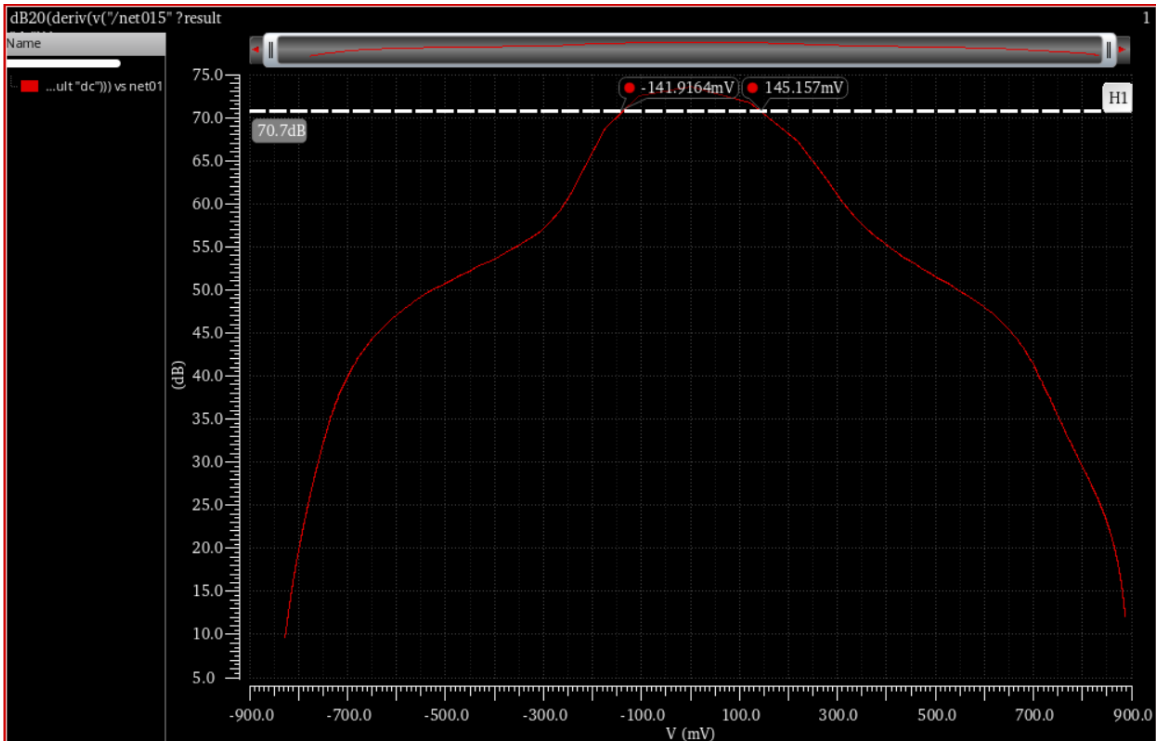

Figure 5: Output Swing

Figure 5 is a plot of the gain as a function of the output voltage. The DC gain of the op-amp is 73.627dB. The output swing is defined as the output voltage range within which the gain remains within 3dB of the DC gain. The op-amp has an output swing of approximately −142mV to 145mV.

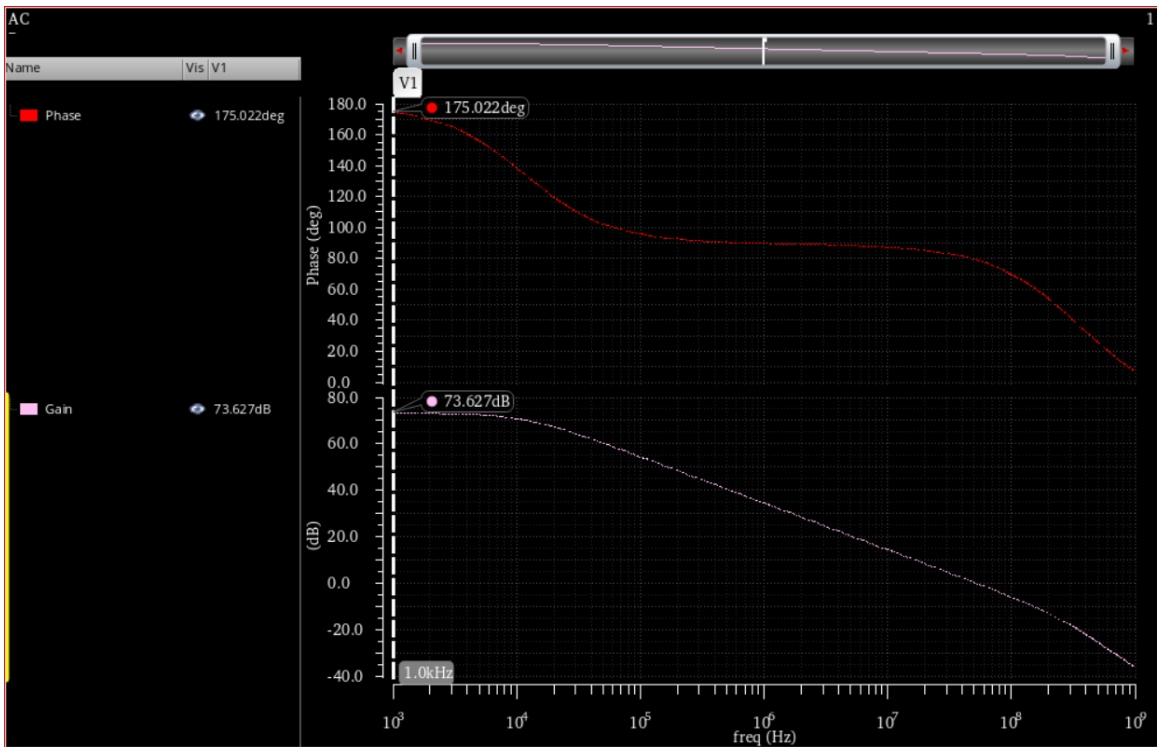

Figure 6: Open-Loop Gain

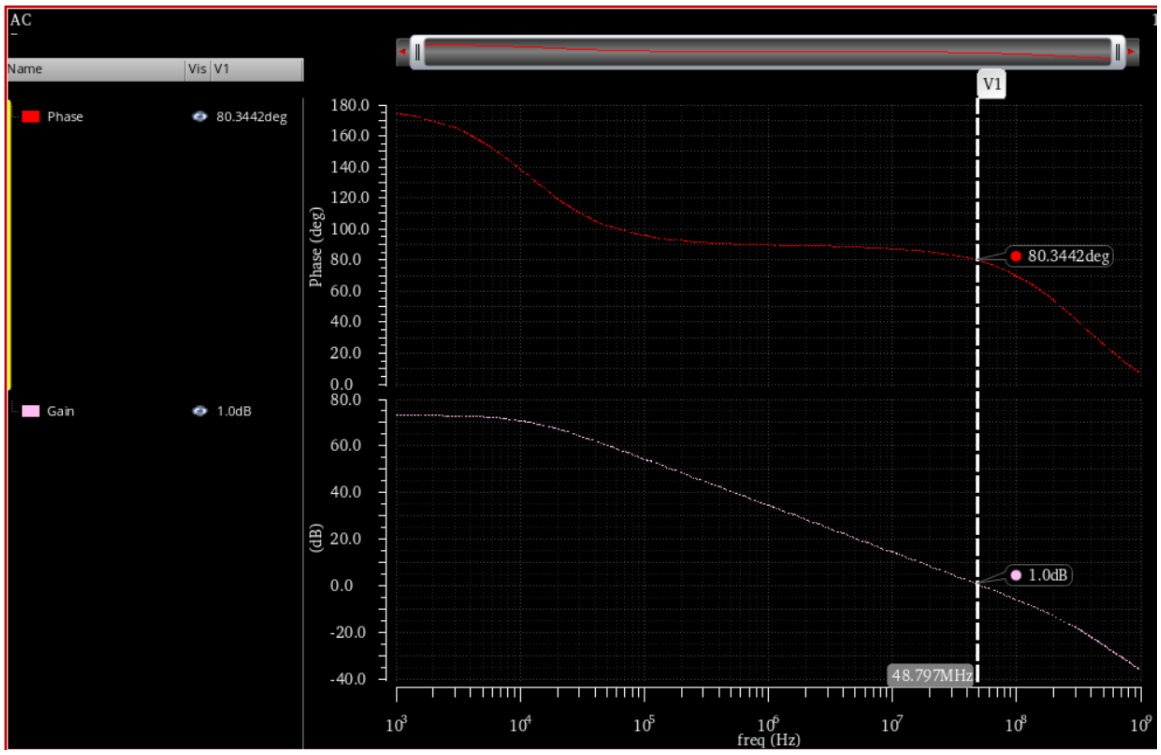

Figure 7: Gain and Phase Plots

Figures 6 and 7 are gain and phase plots. The DC gain is 73.627dB. The unity gain frequency is 48.797MHz. The phase margin is 80.3442°.