Live Lecture Chat Window
April 17, 2024

14:09:05 So something that just impacts temperature won't do for Project #2?

That would be fine since temperature affects grain growth.

14:21:01 Could you reiterate why the volatile keyword is necessary?

It's a message to the compiler that tells it that a certain variable might be changed unexpectedly by another thread. It lets the compiler know not to try to make assumptions about a variable's value.

14:25:58 Is parallelism concerned with performance called something different from parallelism concerned with code structure?

Projects #0 and #1 are concerned with performance. Project #2 is concerned with code structure.

14:26:49 Also, are there any rules about the overall title (Deer-Grain-Environment Simulation in this example)?

Just do something descriptive.

14:26:53 Any specific reason the units in the project writeup are Imperial but your graph uses Metric?

Converting temperatures to Celsius and converting length to centimeters makes the numbers fit better on the graph. Overall, though, I am in favor of metric. "Should the US go to metric?" was an issue when I was a kid. I find it embarrassing that we *still* haven't found the political willpower to do it.

14:27:50 Any tips on how to write the Ranf() function? The one from Project1 doesn't seem to be working for me.

It works. Check how you are using it in your code.

14:29:15 Does Ranf() need to be seeded?

No, not absolutely necessary.

15:25:13 Would forcing the CPU to use only L3 cache for a variable be too slow?

That variable would still need to get to L2 cache (and then to L1 cache) to get into the CPU's ALU.

15:34:46 Restating the cache line performance benefit from "padding" - the idea here is to give each thread its "own" cache line, right?

Correct. The idea is to prevent a core from needing to share the same cache line with other cores..

15:41:01 And, to be clear, a cache line can sit as Invalid for a very long time, or indefinitely, so long as it isn't accessed in any way, right?

That's correct. The path to memory and back doesn't get triggered until the thread holding the Invalid state tries to read from its version of the cache line in its L2 cache.

15:47:59 From Bailey, Mike to Everyone: [Here's how to get to rabbit from flip]

      ssh rabbit.engr.oregonstate.edu