Live Lecture Chat Window

June 5. 2024

14:19:06 Because you used the terms "cluster" vs "DGX" - we would ssh into the DGX cluster to run our Project 7 (MPI) code, correct?

"The DGX" is the 6 gold boxes that hold a total of 96 Nvidia V100 cards: "The cluster" is a collection of PCs. Both the DGX and the cluster are front-ended by the submit-* machines from which you can submit sbatch jobs into either one. You can't reach the DGX or the cluster directly. You have to do it through one of the submit-* machines.



14:27:04 From Brendan Heinz to Everyone:

On the audible wish list for those that like to listen to books! [ChipWar]

https://www.audible.com/pd/Chip-War-

Audiobook/B09TX11LQB?ref_pageloadid=tl2gKjGc7dMGKFKl&ref=a_library_w_c5_lProduct_1&pf_rd_p=95b555b2-2931-4812-98e1-

6535e764d43f&pf_rd_r=143Z70XT8AY3R97F39TJ&pageLoadId=xCDSG2j4mHA38d94&creativeId=b5fa8 602-fb94-432a-aacc-e3734bed4f97

14:32:52 Do you have any suggestions/tips for keeping up with the field efficiently?

Subscribe to newsletters, blogs, magazines, journals, etc. Join ACM and one or more SIGs. Go to conferences. It's a never-ending struggle.

14:39:48 Question about OpenMP and MPI compatibility - MPI_Recv is thread-safe but not interruptsafe. Can I safely put it inside an OpenMP #pragma or will the lack of interrupt safety (one thread switching away from the MPI_Recv) get me in trouble?

I believe that this is telling you that you can put MPI_Send and MPI_Recv calls within OpenMP pragmas. I would guess that "interrupt" means a Linux signal. (https://faculty.cs.niu.edu/~hutchins/csci480/signals.htm)

14:40:37 Are there any office hours next week?

Yes. My Office Hours during Finals Week are:

Monday, June 10	1:00 - 3:00 PDT
Tuesday, June 11	3:00 - 5:00 PDT

15:17:19 Has Nvidia CEO Jensen ever spoken at OSU?

He seems to be here for some reason every couple of years. He was here a month ago for the groundbreaking of the new building:

