Avant!

Chapter 15

Introducing MOSFET

A MOSFET is defined by the MOSFET model and element parameters, and two submodels selected by the CAPOP and ACM model parameters. The CAPOP model parameter specifies the model for the MOSFET gate capacitances. The ACM (Area Calculation Method) parameter selects the type of diode model to be used for the MOSFET bulk diodes. Each of these submodels has associated parameters that define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level, such as Level 1 or Level 50.

This chapter covers the design model and simulation aspects of MOSFET models, parameters of each model level, and associated equations. MOSFET diode and MOSFET capacitor model parameters and equations are also described. For information about individual models and their parameters, refer to Chapter 16, "Selecting a MOSFET Model".

The following topics are covered in this chapter:

- Understanding MOSFET Models
- Selecting Models
- Using Nonplanar and Planar Technologies
- Using a MOSFET Diode Model
- Using MOS Diode Equations
- Using Common Threshold Voltage Equations
- Performing MOSFET Impact Ionization
- Using Noise Models
- Using Temperature Parameters and Equations

Understanding MOSFET Models

The selection of the MOSFET model type for use in analysis usually depends on the electrical parameters critical to the application. Level 1 models are most often used for simulation of large digital circuits where detailed analog models are not needed. Level 1 models offer low simulation time and a relatively high level of accuracy with regard to timing calculations. When precision is required, as for analog data acquisition circuitry, more detailed models, such as the Level 6 IDS model or one of the BSIM models (Level 13, 39, or 49) can be used.

For precision modeling of integrated circuits, the BSIM models take into account the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

Use the SOSFET model (Level 27) to model silicon-on-sapphire MOS devices. You can include photocurrent effects at this level.

Use Levels 5 and Level 38 for depletion MOS devices.

Level 2 models take into account bulk charge effects on current. Level 3 models require less simulation time and provides as much accuracy as Level 2 and have a greater tendency to converge. Level 6 models are compatible with models originally developed with ASPEC. Level 6 can be used to model ion-implanted devices.

Selecting Models

A MOS transistor is described by use of an element statement and a .MODEL statement. The element statement defines the connectivity of the transistor and references the .MODEL statement. The .MODEL statement specifies either an n- or p-channel device, the level of the model, and a number of user-selectable model parameters.

Example

```
M3 3 2 1 0 PCH <parameters>
.MODEL PCH PMOS LEVEL=13 <parameters>
```

The above example specifies a PMOS MOSFET with a model reference name, PCH. The transistor is modeled using the Level 13 BSIM model. The parameters are selected from the model parameter lists in this chapter.

MOSFET Model Levels

MOSFET models consist of client private and public models selected by the parameter .MODEL statement LEVEL parameter. New models are constantly being added to HSPICE.

Not all MOSFET models are available in the PC version of HSPICE, Table 15-1 shows what is available for PC users. Models listed are either on all platforms, including PC, as indicated in the third column, or they are available on all platforms *except* the PC, as indicated in the last column.

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
1	Schichman-Hodges model	X	
2	MOS2 Grove-Frohman model (SPICE 2G)	X	
3	MOS3 empirical model (SPICE 2G)	X	
4	Grove-Frohman: Level 2 model derived from SPICE 2E.3	X	

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
5	AMI-ASPEC depletion and enhancement (Taylor-Huang)	X	
6	Lattin-Jenkins-Grove (ASPEC style parasitics)	X	
7	Lattin-Jenkins-Grove (SPICE style parasitics)	X	
8	advanced Level 2 model	X	
9 **	AMD		X
10 **	AMD		X
11	Fluke-Mosaid model		X
12 **	CASMOS model (GTE style)		X
13	BSIM model	X	
14 **	Siemens Level=4		X
15	user-defined model based on Level 3		X
16	not used	–	–
17	Cypress model		X
18 **	Sierra 1		X
19 ***	Dallas Semiconductor model		X
20 **	GE-CRD FRANZ		X
21 **	STC-ITT		X
22 **	CASMOS (GEC style)		X
23	Siliconix		X
24 **	GE-Intersil advanced		X
25 **	CASMOS (Rutherford)		X
26 **	Sierra 2		X

Level	MOSFET Model Description	All Platforms including PC	All Platforms except PC
27	SOSFET		X
28	BSIM derivative; Meta-software proprietary model	X	
29 ***	not used	–	–
30 ***	VTI		X
31***	Motorola		X
32 ***	AMD		X
33 ***	National Semiconductor		X
34	(EPFL) not used		X*
35 **	Siemens		X
36 ***	Sharp		X
37 ***	TI		X
38	IDS: Cypress depletion model		X
39	BSIM2		X
46 ***	SGS-Thomson MOS Level 3		X
47	BSIM3 Version 2.0		X
49	BSIM3 Version 3		
50	Philips MOS9		

* not officially released
** equations are proprietary – no documentation will be provided
*** requires a license and equations are proprietary – no documentation will be provided

MOSFET Capacitor Selection

The MOSFET capacitance model parameter, CAPOP, is associated with the MOS model. Depending on the value of CAPOP, different capacitor models are used to model the MOS gate capacitance, that is, the gate-to-drain capacitance,

the gate-to-source capacitance, and the gate-to-bulk capacitance. CAPOP allows for the selection of several versions of the Meyer and charge conservation model.

Some of the capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

CAPOP=0   SPICE original Meyer model (general)

CAPOP=1   modified Meyer model (general)

CAPOP=2   parameterized modified Meyer model (general default)

CAPOP=3   parameterized Modified Meyer model with Simpson integration (general)

CAPOP=4   charge conservation model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only

CAPOP=5   no capacitor model

CAPOP=6   AMI capacitor model (Level 5)

CAPOP=9   charge conservation model (Level 3)

CAPOP=13   generic BSIM model (Default for 13, 28, 39)

CAPOP=11   Ward-Dutton model specialized (Level 2)

CAPOP=12   Ward-Dutton model specialized (Level 3)

CAPOP=39   BSIM 2 Capacitance Model (Level 39)

CAPOP=4 selects the recommended charge-conserving model (from among CAPOP=11, 12, or 13) for the given DC model.

Table 15-1: CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12

Table 15-1: CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
13, 28, 39	13	13
others	2	11

The proprietary models, as well as Level 5, 17, 21, 22, 25, 31, 33, and the SOS model Level 27, have their own built-in capacitance routines.

MOS Diode Selection

The model parameter ACM (Area Calculation Method), which controls the geometry of the source and drain diffusions, selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

ACM=0   SPICE model, parameters determined by element areas

ACM=1   ASPEC model, parameters function of element width

ACM=2   META model, combination of ACM=0,1 and provisions for lightly doped drain technology

ACM=3   Extension of ACM=2 model that deals with stacked devices (shared source/drains) and source/drain periphery capacitance along gate edge.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs having width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length, and HSPICE uses the MOSFET model parameters to select the appropriate model for the given width and length.

The HSPICE automatic model selection program searches a data file for a MOSFET model with the width and length range specified in the MOSFET element statement. This model statement is then used in the simulation.

To search a data file for MOSFET models within a given range of width and length, provide a root extension for the model reference name (in the .MODEL statement). Also, you must use the model geometric range parameters LMIN, LMAX, WMIN, and WMAX. These model parameters give the range of the physical length and width dimensions to which the MOSFET model applies. For example, if the model reference name in the element statement is NCH, the model selection program examines the models with the same root model reference name NCH, for example, NCH.1, NCH.2 or NCH.A. The model selection program selects the first MOSFET model statement whose geometric range parameters include the width and length specified in the associated MOSFET element statement.

The following example illustrates calling the MOSFET model selection program from a data file. The model selector program examines the .MODEL statements that have the model reference names with root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50 .

Example

```
*FILE: SELECTOR.SP  TEST OF MOS MODEL SELECTOR
.OPTION LIST WL SCALE=1U SCALM=1U NOMOD
.OP
V1 1 0 5
V2 2 0 4
V3 3 0 1
V4 4 0 -1
M1 1 2 3 4 NCHAN 10 2
M2 1 2 3 4 NCHAN 10 3
M3 1 2 3 4 NCH 10 4
M4 1 2 3 4 NCHX 10 5
M5 1 2 3 4 NCHY 20 5
M6 1 2 3 4 NCHY 50 5
$$$$$$  FOR CHANNEL LENGTH SELECTION
.MODEL NCHAN.2 NMOS LEVEL=2 VTO=2.0 UO=800 TOX=500
NSUB=1E15
+    RD=10  RS=10  CAPOP=5
```

```
+     LMIN=1  LMAX=2.5  WMIN=2 WMAX=15
.MODEL NCHAN.3 NMOS LEVEL=2 VTO=2.2 UO=800 TOX=500
NSUB=1E15
+     RD=10  RS=10  CAPOP=5
+     LMIN=2.5  LMAX=3.5  WMIN=2 WMAX=15
$$$$$$$   NO SELECTION FOR CHANNEL LENGTH AND WIDTH
.MODEL NCH  NMOS LEVEL=2 VTO=2.3 UO=800 TOX=500
NSUB=1E15
+     RD=10  RS=10  CAPOP=5
$+    LMIN=3.5  LMAX=4.5  WMIN=2 WMAX=15
.MODEL NCHX NMOS LEVEL=2 VTO=2.4 UO=800 TOX=500
NSUB=1E15
+     RD=10  RS=10  CAPOP=5
$+    LMIN=4.5  LMAX=100  WMIN=2 WMAX=15
$$$$$$$  FOR CHANNEL WIDTH SELECTION
.MODEL NCHY.20  NMOS LEVEL=2 VTO=2.5 UO=800 TOX=500
NSUB=1E15
+     RD=10  RS=10  CAPOP=5
+     LMIN=4.5  LMAX=100  WMIN=15 WMAX=30
.MODEL NCHY.50 NMOS LEVEL=2 VTO=2.5 UO=800 TOX=500
NSUB=1E15
+     RD=10  RS=10  CAPOP=5
+     LMIN=4.5  LMAX=100  WMIN=30 WMAX=500
.END
```

MOSFET Control Options

Specific control options (set in the .OPTIONS statement) used for MOSFET models include the following. For flag-type options, 0 is unset (off) and 1 is set (on).

ASPEC	This option uses ASPEC MOSFET model defaults and set units. Default=0.
BYPASS	This option avoids recomputation of nonlinear functions that do not change with iterations. Default=0.

MBYPAS	BYPASS tolerance multiplier. Default=1.
DEFAD	default drain diode area. Default=0.
DEFAS	default source diode area. Default=0.
DEFL	default channel length. Default=$1e^{-4}$m.
DEFW	default channel width. Default=$1e^{-4}$m.
DEFNRD	default number of squares for drain resistor. Default=0.
DEFNRS	default number of squares for source resistor. Default=0.
DEFPD	default drain diode periphery. Default=0.
DEFPS	default source diode periphery. Default=0.
GMIN	Pn junction parallel transient conductance. Default=$1e^{-12}$mho.
GMINDC	Pn junction parallel DC conductance. Default=$1e^{-12}$mho.
SCALE	element scaling factor. Default=1.
SCALM	model scaling factor. Default=1.
WL	This option changes the order of specifying MOS element VSIZE from the default order, length-width, to width-length. Default=0.

Override the defaults DEFAD, DEFAS, DEFL, DEFNRD, DEFNRS, DEFPD, DEFPS, and DEFW in the MOSFET element statement by specifying AD, AS, L, NRD, NRS, PD, PS, and W, respectively.

Unit Scaling

Units are controlled by the options SCALE and SCALM. SCALE scales element statement parameters, and SCALM scales model statement parameters. SCALM also affects the MOSFET gate capacitance and diode model parameters. In this chapter, scaling only applies to those parameters specified as scaled. If SCALM is specified as a parameter in a .MODEL statement, it overrides the option SCALM; in this way, models using different values of SCALM can be used in

the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

Table 15-2: Model Parameter Scaling

Parameter Units	Parameter Value
meter	multiplied by SCALM
meter^2	multiplied by SCALM^2
meter^{-1}	divided by SCALM
meter^{-2}	divided by SCALM^2

Override global model size scaling for individual MOSFET, diode, and BJT models that uses the .OPTION SCALM=<*val*> statement by including SCALM=<*val*> in the .MODEL statement. .OPTION SCALM=<*val*> applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models, and cannot be overridden in the model.

Scaling for Level 25 and 33

When using the proprietary Level 25 (Rutherford CASMOS) or Level 33 (National) models, the SCALE and SCALM options are automatically set to 1e-6. If you use these models together with other scalable models, however, set the options, SCALE=1e-6 and SCALM=1e-6, explicitly.

Bypassing Latent Devices

Use the BYPASS (latency) option to decrease simulation time in large designs. It speeds simulation time by not recalculating currents, capacitances, and conductances if the voltages at the terminal device nodes have not changed. The BYPASS option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use .OPTION BYPASS to set BYPASS.

BYPASS can result in a reduction in accuracy of the simulation for tightly coupled circuits such as op-amps, high gain ring oscillators, and so on. Use .OPTION MBYPAS to set MBYPAS to a smaller value to improve the accuracy of the results.

MOSFET Element Syntax

This section describes the MOSFET element syntax.

General form

    Mxxx nd ng ns <nb> mname <L=val> <W=val> <AD=val> <AS=val> <PD=val>
    <PS=val>
    +   <NRD=val> <NRS=val> <RDC=val> <RSC=val> <OFF> <IC=vds, vgs, vbs>
    <M=val>
    +   <DTEMP=val> <GEO=val> <DELVTO=val>

or

    Mxxx nd ng ns <nb> mname lval wval …

or

    .OPTION WL
    Mxxx nd ng ns <nb> mname wval lval …

Mxxx	MOSFET element name. The name must begin with an "M" followed by up to 15 alphanumeric characters.
ng	gate terminal node name
ns	source terminal node name
nb	bulk terminal node name Can be set by BULK parameter in model statement.
nd	drain terminal node name
mname	model name reference
	Note: If the model name includes a period (.), the HSPICE automatic model selector does not work properly for that model. Do not use periods in model names if you intend to use the automatic model selector.
L	channel length. This option overrides DEFL in OPTIONS statement. Default=DEFL. Lscaled = L · SCALE. The maximum value of Lscaled is 0.1 m.

W	channel width. This option overrides DEFW in OPTIONS statement. Default= DEFW. Wscaled = W · SCALE
AD	drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD only when ACM=0. (See "Using a MOSFET Diode Model" for effective ADeff).
AS	source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS only when ACM=0. (See "Using a MOSFET Diode Model" for effective ASeff).
PD	perimeter of the drain junction, including the channel edge. Overrides DEFPD in OPTIONS statement. ACM=0 and ACM=1 Default=DEFPD. ACM=2, 3 Default=0.0 (See "Using a MOSFET Diode Model").
PS	perimeter of the source junction, including the channel edge. Overrides DEFPS in OPTIONS statement. ACM=0 and ACM=1 Default=DEFPD. ACM=2, 3 Default=0.0 (See "Using a MOSFET Diode Model").
NRD	number of squares of drain diffusion for resistance calculations. Overrides DEFNRD in .OPTIONS statement. ACM=0 and ACM=1: default=DEFNRD. ACM=2: default=0.0 (see "Using a MOSFET Diode Model").
NRS	number of squares of source diffusion for resistance calculations. Overrides DEFNRS in .OPTIONS statement. ACM=0 and ACM=1: default=DEFNRS. ACM=2, 3: default=0.0 (see "Using a MOSFET Diode Model").
RDC	additional drain resistance due to contact resistance. (Units are ohm; Default = 0.0) **Note:** A value assigned for RDC in the element statement overrides any value for RDC as a model parameter.
RSC	additional source resistance due to contact resistance. (Units are ohm; Default=0.0)

Note: A value assigned for RSC in the element statement overrides any value for RSC as a model parameter.

OFF sets the initial condition to OFF for this element in the DC analysis, or for the first timepoint in the transient analysis. Default=ON.
Note: This command does not work for depletion devices.

M multiple device option. MOSFET channel width, diode leakage, capacitors, and resistors are altered by this parameter. Simulates multiple parallel devices. Default=1.0.

vbs initial condition for the voltage across the external bulk and source terminals. Overridden by the IC statement.

vds initial condition for the voltage across the external drain and source terminals. Overridden by the IC statement.

vgs initial condition for the voltage across the external gate and source terminals. Overridden by the IC statement.

DTEMP device temperature difference from circuit temperature. Default=0.0.

GEO source/drain sharing selector for ACM=3. Default=0.0 (see ACM=3 section).

DELVTO zero-bias threshold voltage shift. Default=0.0.

Note: SCALE defaults to 1.0 meter. To enter parameter PD=val with units in microns, for example, set SCALE to 1e-6. Then if PD=5 is entered, HSPICE sets PD=5e-6 meters, or 5 microns.

Examples

```
M1 24 2 0 20 TYPE1

M31 2 17 6 10 MODM L=5U W=2U
M31 2 16 6 10 MODM 5U 2U
Or
```

```
.OPTION WL
M31 2 16 6 10 MODM 2U 5U

M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U
PS=40U
M1 2 9 3 0 MOD1 10U 5U 2P 2P
```

The first example specifies a MOSFET element connected between nodes 24, 2, 0, and 20. It calls a MOSFET model statement which has a model reference name called TYPE1. The .OPTION WL reverses the order of the width and length parameters in the MOSFET element statement.

The element statement parameters previously listed are summarized below. You can specify the geometric parameters, except for M, in the options statements. Element parameter values always override .OPTION or .MODEL parameter settings.

Table 15-3: MOSFET Element Parameters

Function	Parameters
geometric	AD, AS, L, M, PD, PS, W
initialization	IC=Vds, Vgs, Vbs, OFF
netlist	Mxxx, nd, ng, ns, nb, mname
resistance	NRD, NRS, RDC, RSC
temperature	DTEMP

Table 15-4: Variables and Constants.

Variable	Definition
cbd	bulk to drain capacitance
cbs	bulk to source capacitance
cbg	gate to bulk capacitance

Table 15-4: Variables and Constants.

Variable	Definition
cgd	gate to drain capacitance
cgs	gate to source capacitance
f	frequency
gbd	bulk to drain dynamic conductance

Equation Variables

This section lists the equation variables and constants.

Table 15-5: Equation Variables and Constants

Variable/Quantity	Definition
gbs	bulk to source dynamic conductance
gds	drain to source dynamic conductance controlled by vds
gdb	drain to bulk impact ionization conductance
gm	drain to source dynamic transconductance controlled by vgs
gmbs	drain to source dynamic bulk transconductance controlled by vsb
ibd	bulk to drain DC current
ibs	bulk to source DC current
ids	drain to source DC current
idb	drain to bulk impact ionization current
ind	drain to source equivalent noise circuit
inrd	drain resistor equivalent noise circuit
inrs	source resistor equivalent noise circuit
rd	drain resistance
rs	source resistance

Table 15-5: Equation Variables and Constants

Variable/Quantity	Definition
vsb	source to bulk voltage
vds	drain to source voltage
vgs	gate to source voltage
Δt	t-tnom
εsi	1.0359e-10F/m dielectric constant of silicon
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	new temperature of model or element in °K
tnom	tnom = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C).
vt	$k \cdot t/q$
vt(tnom)	$k \cdot tnom/q$

MOSFET Current Convention

Figure 15-1: shows the assumed direction of current flow through a MOS transistor. When printing the drain current, use either I(M1) or I1(M1) syntax. I2 produces the gate current, I3 produces the source current, and I4 produces the substrate current. References to bulk are the same as references to the substrate.
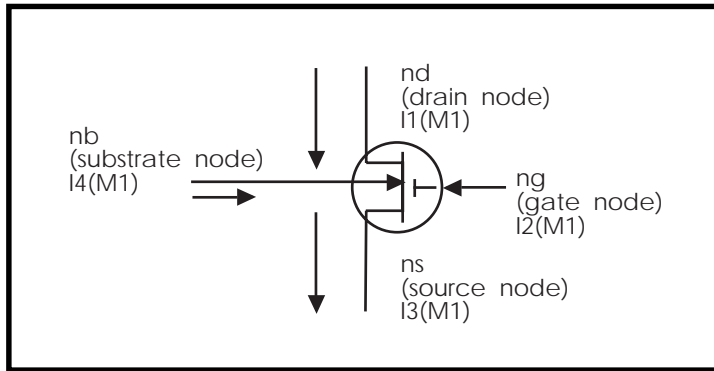
Figure 15-1: MOSFET Current Convention, N-channel

MOSFET Equivalent Circuits

HSPICE uses three equivalent circuits in the analysis of MOSFETs: DC, transient, and AC and noise equivalent circuits. The components of these circuits form the basis for all element and model equation discussion. The equivalent circuit for DC sweep is the same as the one used for transient analysis, except capacitances are not included. Figures 15-2 through Figure 15-4 display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (ids). For the noise and AC analyses, the actual ids current is not used. Instead, the model uses the partial derivatives of ids with respect to the terminal voltages vgs, vds, and vbs. The names for these partial derivatives are:

Transconductance

$$gm = \frac{\partial(ids)}{\partial(vgs)}$$

Conductance

$$gds = \frac{\partial(ids)}{\partial(vds)}$$

Bulk Transconductance

$$gmbs = \frac{\partial(ids)}{\partial(vbs)}$$

The ids equation describes the basic DC effects of the MOSFET. The effects of gate capacitance and of source and drain diodes are considered separately from the DC ids equations. In addition, the impact ionization equations are treated separately from the DC ids equation, even though its effects are added to ids.
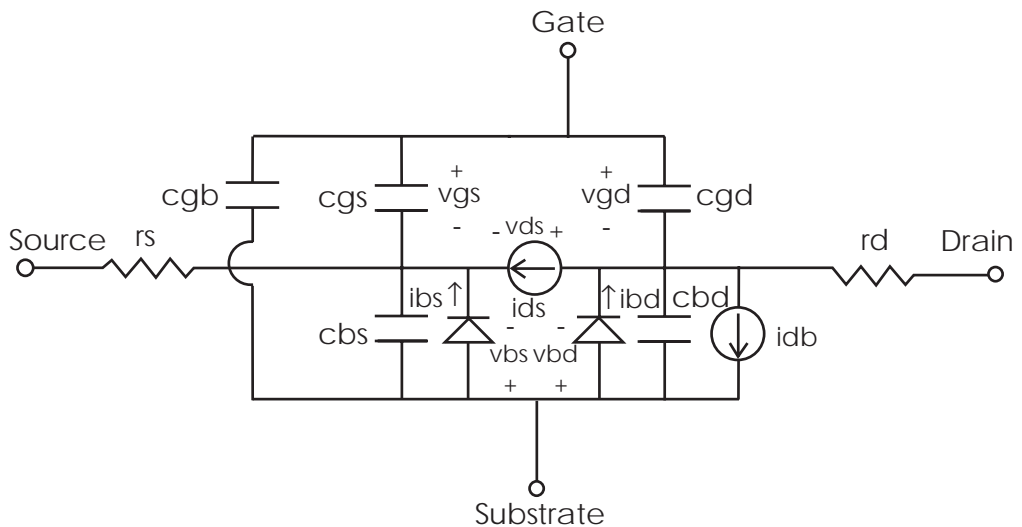

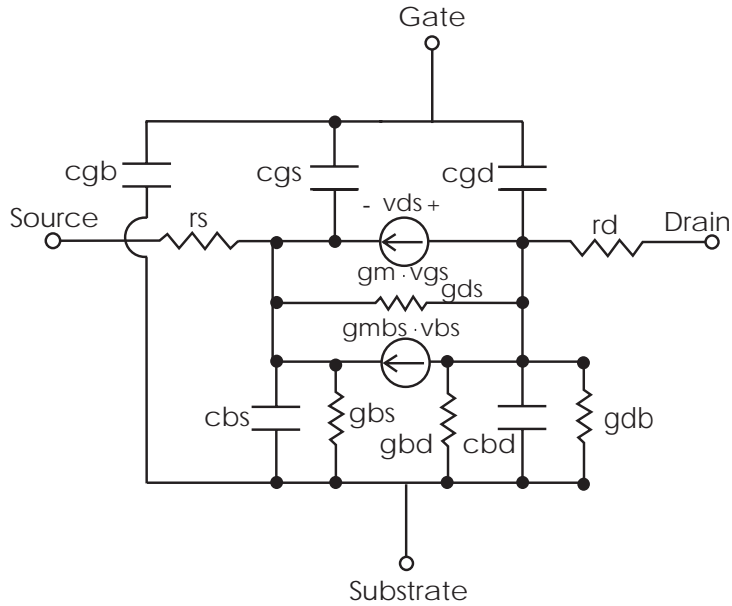**Figure 15-2: Equivalent Circuit, MOSFET Transient Analysis**

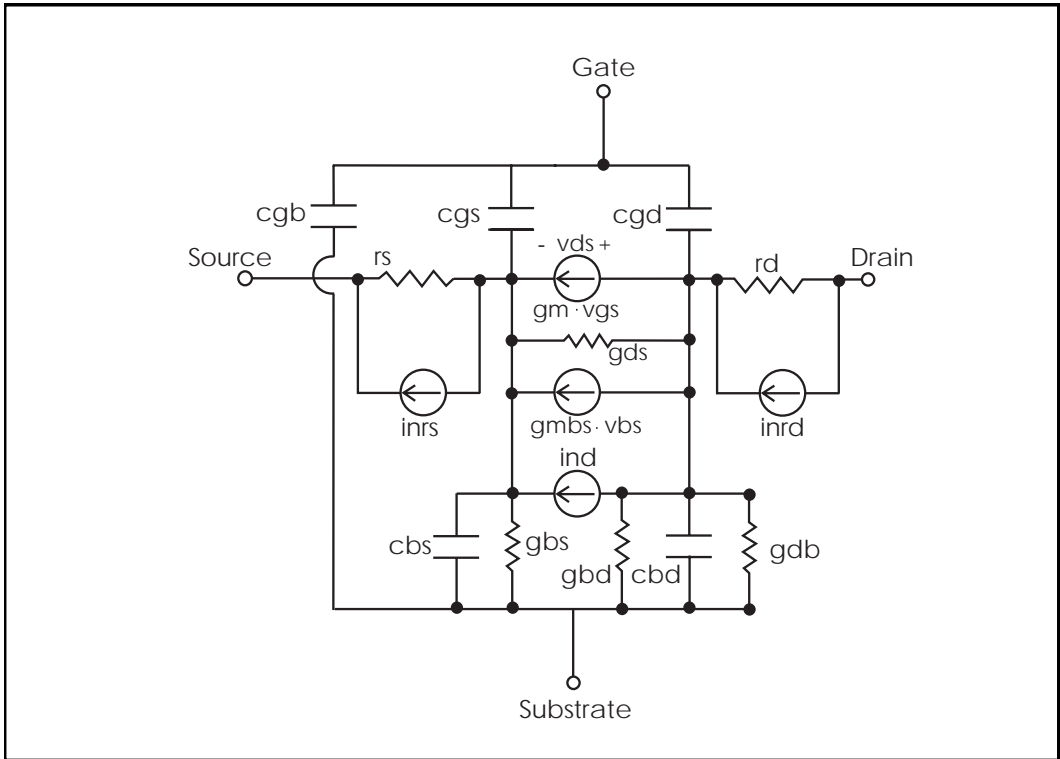**Figure 15-3: Equivalent Circuit, MOSFET AC Analysis**

Figure 15-4: Equivalent Circuit, MOSFET AC Noise Analysis

Using Nonplanar and Planar Technologies

Two MOSFET fabrication technologies have dominated integrated circuit design: nonplanar and planar technologies. Nonplanar technology uses metal gates. The simplicity of the process generally provides acceptable yields. The primary problem with metal gates is metal breakage across the field oxide steps. Field oxide is grown by oxidizing the silicon surface. When the surface is cut, it forms a sharp edge. Since metal must be affixed to these edges in order to contact the diffusion or make a gate, it is necessary to apply thicker metal to compensate for the sharp edges. This metal tends to gather in the cuts, making etching difficult. The inability to accurately control the metal width necessitates very conservative design rules and results in low transistor gains.

In planar technology, the oxide edges are smooth, with a minimal variance in metal thickness. Shifting to nitride was accomplished by using polysilicon gates. Adding a chemical reactor to the MOS fabrication process enables not only the deposition of silicon nitride, but also that of silicon oxide and polysilicon. The ion implanter is the key element in this processing, using implanters with beam currents greater than 10 milliamperes.

Since implanters define threshold voltages and "diffusions" as well as field thresholds, processes require a minimum number of high temperature oven steps. This enables low temperature processing and maskless pattern generation. The new wave processes are more similar to the older nonplanar metal gate technologies.

Field Effect Transistor

The metal gate MOSFET is a nonisoplanar metal-oxide-semiconductor field effect transistor as illustrated in Figure 15-5 and Figure 15-6.
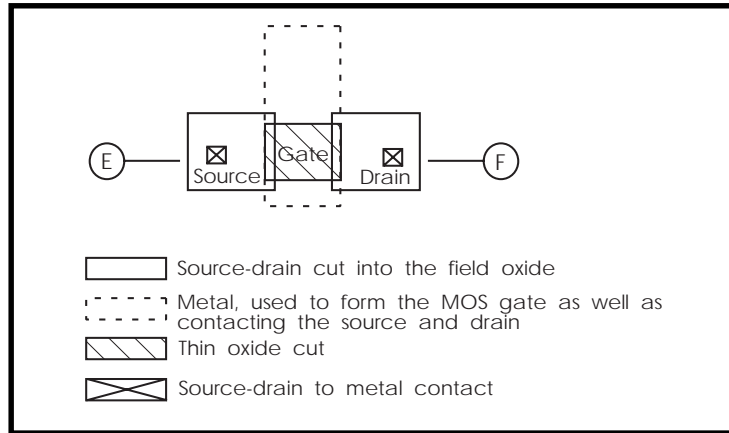
Figure 15-5: Field Effect Transistor

Looking at the actual geometry, from source-to-drain, Figure 15-6 shows a perspective of the nonisoplanar metal-oxide semiconductor field effect transistor.
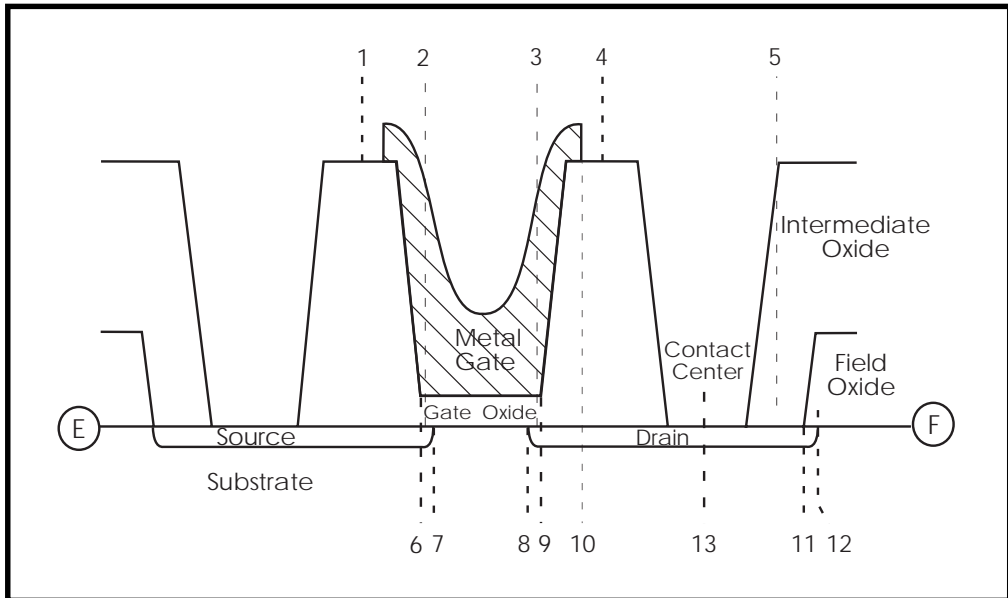

Figure 15-6: Field Effect Transistor Geometry

1 - 4	drawn metal gate channel length
2 - 3	drawn oxide cut
7 - 8	effective channel length
6 - 9	etched channel length
8 - 9	lateral diffusion
5	drawn diffusion edge
11	actual diffusion edge

To visualize the construction of the silicon gate MOSFET, observe how a source or drain to field cuts (Figure 15-7.) The cut A-B shows a drain contact (Figure 15-8).
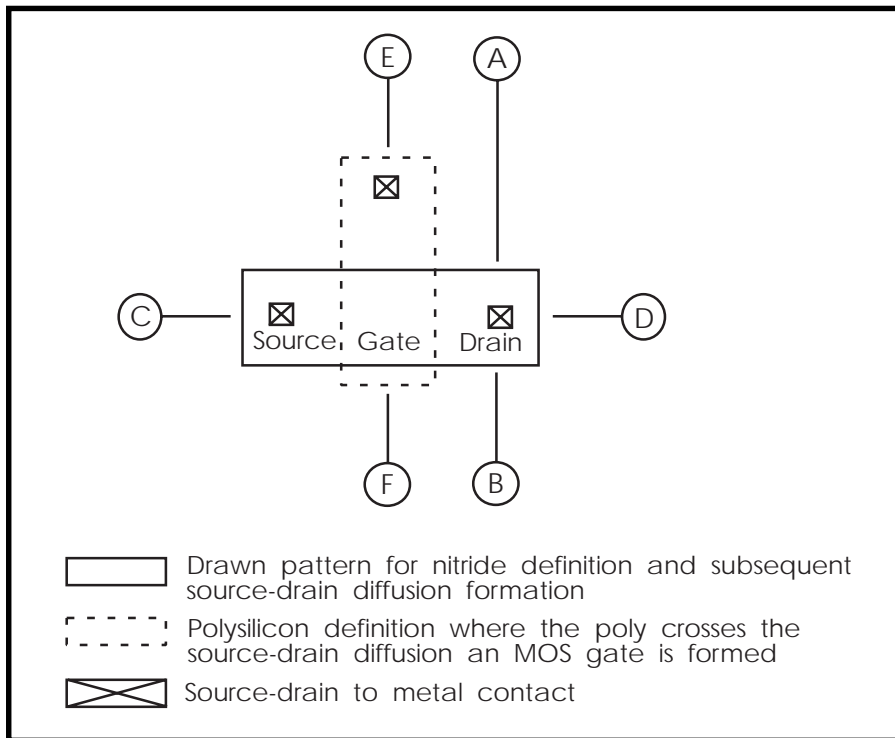

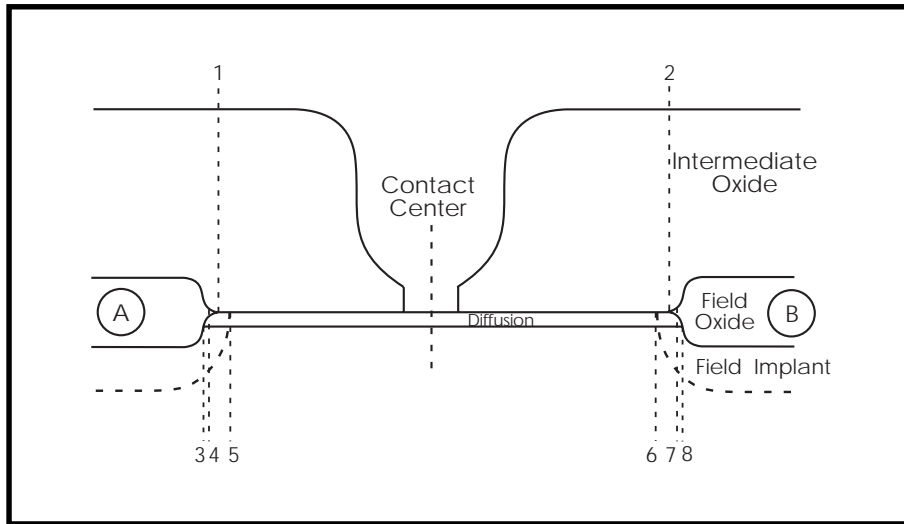**Figure 15-7: Isoplanar Silicon Gate Transistor**

Figure 15-8: Isoplanar MOSFET Construction, Part A

1 - 2   diffusion drawn dimension for nitride

4 - 7   nitride layer width after etch

3 - 1   periphery of the diode

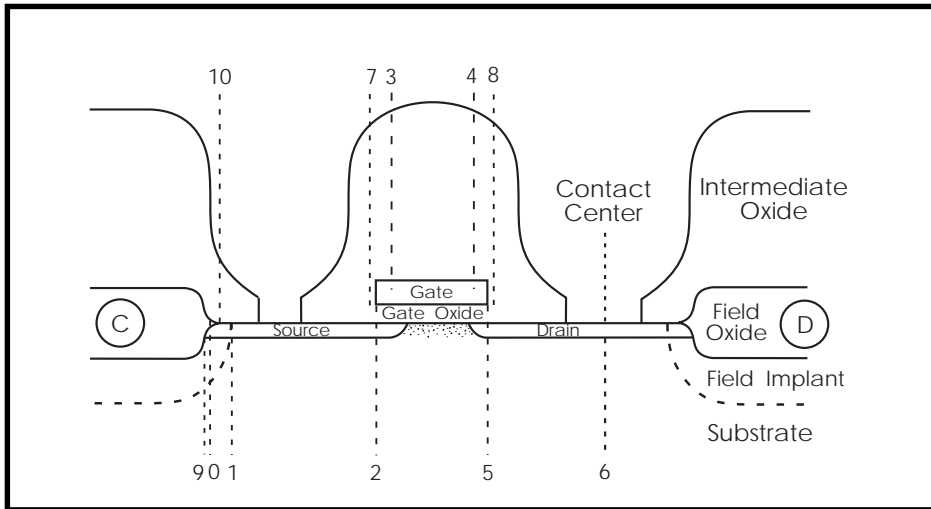The cut from the source to the drain is represented by C - D (Figure 15-9), which includes the contacts.

Figure 15-9: Isoplanar MOSFET Construction, Part B

7 - 8	drawn channel length L
2 - 5	actual poly width after etching $L + XL$ where $XL<0$
3 - 4	effective channel length after diffusion $L + XL - LD$
4 - 5	lateral diffusion LD
9 - 10	diffusion periphery for diode calculations
5 - 6	gate edge to center contact for ACM=1 and ACM=2 calculations

The planar process produces parasitic capacitances at the poly to field edges of the device. The cut along the width of the device demonstrates the importance of these parasitics (Figure 15-10).

The encroachment of the field implant into the channel not only narrows the channel width, but also increases the gate to bulk parasitic capacitance.

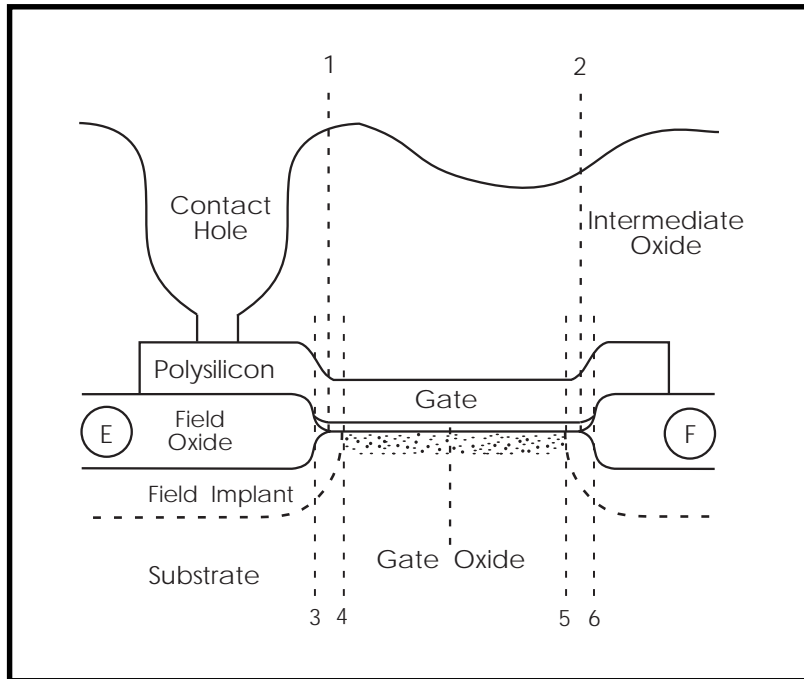**Figure 15-10: Isoplanar MOSFET, Width Cut**

1 - 2	drawn width of the gate W
3 - 4	depleted or accumulated channel (parameter WD)
4 - 5	effective channel width W+ XW -2 WD
3 - 6	physical channel width W + XW

General MOSFET Model Statement

This is the general form for all model specifications. All related parameter levels are covered in their respective sections.

General form

```
.MODEL mname [PMOS | NMOS] (<LEVEL=val>
<keyname1=val1> <keyname2=val2>…)
+      <VERSION=version_number>
```

or

```
.MODEL mname NMOS(<LEVEL = val> <keyname1 = val1>
<keyname2=val2>…)
+      <VERSION=version_number> …)
```

mname	model name. Elements refer to the model by this name.
PMOS	identifies a p-channel MOSFET model
NMOS	identifies an n-channel MOSFET model
LEVEL	The MOSFET model includes several device model types. Use the LEVEL parameter for selection. Default=1.0.
VERSION	This parameter specifies the version number of the model, for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the .MODEL statement description for information about the effects of the VERSION parameter.

Examples

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
.MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
VERSION=95.1
```

Using a MOSFET Diode Model

The Area Calculation Method (ACM) parameter allows for the precise control of modeling bulk-to-source and bulk-to-drain diodes within MOSFET models. The ACM model parameter is used to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

MOSFET Diode Model Selection

To select a MOSFET diode model, set the ACM parameter within the MOSFET model statements. If ACM=0, the pn bulk junctions of the MOSFET are modeled in the SPICE-style. The ACM=1 diode model is the original ASPEC model. The ACM=2 model parameter specifies the HSPICE improved diode model, which is based on a model similar to the ASPEC MOSFET diode model. The ACM=3 diode model is a further HSPICE improvement that deals with capacitances of shared sources and drains and gate edge source/drain-to-bulk periphery capacitance. If the ACM model parameter is not set, the diode model defaults to the ACM=0 SPICE model. ACM=0 and ACM=1 models do not permit the specification of HDIF. ACM=0 does not permit specification of LDIF. Furthermore, the geometric element parameters AD, AS, PD, and PS are not used for the ACM=1 model.

Convergence

The GMIN and GMINDC options parallel a conductance across the bulk diodes and drain-source for transient and DC analysis, respectively. Use these options to enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the parameters RSH, RS, and RD to keep the diode from being overdriven in either a DC or transient forward bias condition. Use of these parameters also enhances the convergence properties of the diode model.

MOSFET Diode Model Parameters

This section describes the diode model parameters for MOSFET.

DC Model Parameters

Name(Alias)	Units	Default	Description
ACM		0	area calculation method
JS	amp/ m^2	0	bulk junction saturation current JSscaled = JS/SCALM^2 – for ACM=1, unit is amp/m and JSscaled = JS/SCALM.
JSW	amp/m	0	sidewall bulk junction saturation current JSWscaled = JSW/SCALM.
IS	amp	1e-14	bulk junction saturation current. For the option ASPEC=1, default=0.
N		1	emission coefficient
NDS		1	reverse bias slope coefficient
VNDS	V	-1	reverse diode current transition point

Capacitance Model Parameters

Name(Alias)	Units	Default	Description
CBD	F	0	zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0.
CBS	F	0	zero bias bulk-source junction capacitance. Used only when CJ and CJSW are 0.

Name(Alias)	Units	Default	Description
CJ (CDB, CSB, CJA)	F/m^2	579.11 μF/m^2	zero-bias bulk junction capacitance: CJscaled = CJ/SCALM^2 – for ACM=1 the unit is F/m and CJscaled = CJ/SCALM – default for option ASPEC=0 is $$CJ = \left(\frac{\varepsilon si \cdot q \cdot NSUB}{2 \cdot PB}\right)^{1/2}$$
CJSW (CJP)	F/m	0	zero-bias sidewall bulk junction capacitance CJSWscaled = CJSW/SCALM – default = 0
CJGATE	F/m	CSJW	zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only) CJGATEscaled=CJGATE/SCALM Default = CJSW for HSPICE releases later than H9007D. Default = 0 for HSPICE releases H9007D and earlier, or if CJSW is not specified.
FC		0.5	forward-bias depletion capacitance coefficient (not used)
MJ (EXA, EXJ, EXS, EXD		0.5	bulk junction grading coefficient
MJSW (EXP)		0.33	bulk sidewall junction grading coefficient
NSUB (DNB, NB)	1/cm^3	1.0e15	substrate doping
PB (PHA, PHS, PHD)	V	0.8	bulk junction contact potential
PHP	V	PB	bulk sidewall junction contact potential
TT	s	0	transit time

Drain and Source Resistance Model Parameters

Name(Alias)	Units	Default	Description
RD	ohm/sq	0.0	drain ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.
RDC	ohm	0.0	additional drain resistance due to contact resistance
LRD	ohm/m	0	drain resistance length sensitivity. Use this parameter with automatic model selection in conjunction with WRD and PRD to factor model for device size.
WRD	ohm/m	0	drain resistance length sensitivity (used with LRD)
PRD	ohm/m^2	0	drain resistance product (area) sensitivity (used with LRD)
RS	ohm/sq	0.0	source ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.
LRS	ohm/m	0	source resistance length sensitivity. Use this parameter with automatic model selection in conjunction with WRS and PRS to factor model for device size.
WRS	ohm/m	0	source resistance width sensitivity (used with LRS)
PRS	ohm/m^2	0	source resistance product (area) sensitivity (used with LRS)
RSC	ohm	0.0	additional source resistance due to contact resistance
RSH (RL)	ohm/sq	0.0	drain and source diffusion sheet resistance

MOS Geometry Model Parameters

Name(Alias)	Units	Default	Description
HDIF	m	0	length of heavily doped diffusion, from contact to lightly doped region (ACM=2, 3 only)
			HDIFwscaled = HDIF · SCALM
LD (DLAT,LATD)	m		lateral diffusion into channel from source and drain diffusion. If LD and XJ are unspecified, LD default=0.0. When LD is unspecified, but XJ is specified, LD is calculated from XJ. LD default=0.75 · XJ. For Level 4 only, lateral diffusion is derived from LD·XJ. LDscaled = LD · SCALM
LDIF	m	0	length of lightly doped diffusion adjacent to gate (ACM=1, 2) LDIFscaled = LDIF · SCALM
WMLT		1	width diffusion layer shrink reduction factor
XJ	m	0	metallurgical junction depth XJscaled = XJ · SCALM
XW (WDEL, DW)	m	0	accounts for masking and etching effects XWscaled = XW · SCALM

ACM=0 MOS Diode

The following listing illustrates typical parameter value settings for a MOSFET diode that is designed with a MOSFET that has a channel length of 3 μm and a channel width of 10 μm.

Figure 15-11: – ACM=0 MOS Diode

Example

Transistor with LD=.5μm   W=10μm   L=3μm

AD	area of drain (about 80 pm^2)
AS	area of source (about 80 pm^2)
CJ	4e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-8 A/m^2
JSW	1e-13 A/m
NRD	number of squares for drain resistance
NRS	number of squares for source resistance
PD	sidewall of drain (about 36 μm)
PS	sidewall of source (about 36 μm)

Effective Areas and Peripheries Calculations

For ACM=0, the effective areas and peripheries are calculated as follows:

$$ADeff = M \cdot AD \cdot WMLT^2 \cdot SCALE$$

$$ASeff = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

$$PDeff = M \cdot PD \cdot WMLT \cdot SCALE$$

$$PSeff = M \cdot PS \cdot WMLT \cdot SCALE$$

Effective Saturation Current Calculations

For ACM=0, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define:

$$val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0 then,

$$isbs = val$$

Otherwise,

$$isbd = M \cdot IS$$

Drain Diode Saturation Current

Define:

$$val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd = val$$

Otherwise,

$$isbd = M \cdot IS$$

Effective Drain and Source Resistances

For ACM=0, the effective drain and source resistances are calculated as follows:

Source Resistance

Define:

$$val = NRS \cdot RSH$$

If val > 0 then,

$$RSeff = \frac{val + RSC}{M}$$

Otherwise,

$$RSeff = \frac{RS + RSC}{M}$$

Drain Resistance

Define:

$$val = NRD \cdot RSH$$

If val > then,

$$RDeff = \frac{val + RDC}{M}$$

Otherwise,

$$RDeff = \frac{RD + RDC}{M}$$

ACM=1 MOS Diode

HSPICE uses ASPEC-style diodes when the model parameter ACM=1 is
specified. Parameters AD, PD, AS, and PS are not used, and the units JS and CJ
differ from the SPICE style diodes (ACM=0).

Figure 15-12: ACM=1 MOS Diode

Example

The listings below are typical parameter value settings for a transistor with

LD=0.5 μmW=10 μmL=3 μmLDIF=0.5 μm

CJ	1e-10 F/m of gate width Note the change from F/m^2 (in ACM=0) to F/m.
CJSW	2e-10 F/m of gate width
JS	1e-14 A/m of gate width Note the change from A/m^2 (in ACM=0) to A/m
JSW	1e-13 A/m of gate width
NRD	number of squares for drain resistance
NRS	number of squares for source resistance

Effective Areas and Peripheries Calculations

For ACM=1, the effective areas and peripheries are calculated as follows:

$ADeff \; = \; Weff \cdot WMLT$

$ASeff \; = \; Weff \cdot WMLT$

$PDff \; = \; Weff$

$PSeff \; = \; Weff$

where

$Weff \; = \; M \cdot (Wscaled \cdot WMLT + XWscaled)$

Note: The Weff is not quite the same as the weff given in the models Level 1,
2, 3, 6, and 13 sections. The term $2 \cdot WDscaled$ is not subtracted.

Effective Saturation Current Calculations

For ACM=1, the MOS diode effective saturation currents are calculated as
follows:

Source Diode Saturation Current

Define:

$val \; = \; JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If val > 0 then,

$isbs \; = \; val$

Otherwise:

$isbs \; = \; M \cdot IS$

Drain Diode Saturation Current

Define:

$$val \ = \ JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd \ = \ val$$

Otherwise,

$$isbd \ = \ M \cdot IS$$

Effective Drain and Source Resistances

For ACM=1, the effective drain and source resistances are calculated as follows:

Source Resistance

For UPDATE=0,

$$RSeff \ = \ \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1 and LDIF=0 and the ASPEC option is also specified then:

$$RSeff \ = \ \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0,

$$RDeff \ = \ \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE $\geq$ 1 and LDIF=0 and the ASPEC option is also specified then:

$$RDeff \ = \ \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

Note: See Levels 6 and 7 for more possibilities.

ACM=2 MOS Diode

HSPICE uses HSPICE style MOS diodes when the model parameter ACM=2 is specified. This allows a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly and heavily doped diffusions (by setting the LD, LDIF, and HDIF parameters). The units of JS, JSW, CJ, and CJSW used in SPICE are preserved, permitting full compatibility.

ACM=2 automatically generates more reasonable diode parameter values than those for ACM=1. The ACM=2 geometry can be generated one of two ways:

- Element parameters: AD, AS, PD, and PS can be used for parasitic generation when specified in the element statement. Default options values for these parameters are not applicable.
- If the diode is to be suppressed, set IS=0, AD=0, and AS=0.

The source diode is suppressed if AS=0 is set in the element and IS=0 is set in the model. This setting is useful for shared contacts.

Figure 15-13: ACM=2 MOS Diode

Example

Transistor with LD=0.07μm W=10 μm L=2 μm LDIF=1 μm HDIF= 4 μm, typical MOSFET diode parameter values are:

AD	area of drain. Default option value for AD is not applicable.
AS	area of source. Default option value for AS is not applicable.
CJ	1e-4 F/m^2
CJSW	1e-10 F/m
JS	1e-4 A/m^2
JSW	1e-10 A/m
HDIF	length of heavy doped diffusion contact to gate (about 2 μm)
	HDIFeff=HDIF · WMLT · SCALM
LDIF+LD	length of lightly doped diffusion (about 0.4μm)
NRD	number of squares drain resistance. Default option value for NRD is not applicable.
NRS	number of squares source resistance. Default option value for NRS is not applicable.
PD	periphery of drain, including the gate width for ACM=2. No default.

PS	periphery of source, including the gate width for ACM=2. No default.
RD	resistance (ohm/square) of lightly doped drain diffusion (about 2000)
RS	resistance (ohm/square) of lightly doped source diffusion (about 2000)
RSH	diffusion sheet resistance (about 35)

Effective Areas and Peripheries Calculations

For ACM=2, the effective areas and peripheries are calculated as follows:

If AD is not specified then,

$$ADeff \; = \; 2 \cdot HDIFeff \cdot Weff$$

Otherwise,

$$ADeff \; = \; M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

If AS is not specified then,

$$ASeff \; = \; 2 \cdot HDIFscaled \cdot Weff$$

Otherwise,

$$ASeff \; = \; M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

If PD is not specified then,

$$PDeff \; = \; 4 \cdot HDIFeff + 2 \cdot Weff$$

Otherwise,

$$PDeff \; = \; M \cdot PD \cdot WMLT \cdot SCALE$$

If PS is not specified then,

$$PSeff \; = \; 4 \cdot HDIFeff + 2 \cdot Weff$$

Otherwise,

$$PSeff \; = \; M \cdot PS \cdot WMLT \cdot SCALE$$

where

$$Weff \; = \; M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff \; = \; HDIFscaled$$

$$HDIFscaled \; = \; HDIF \cdot SCALM \cdot WMLT$$

Note: The Weff is not quite the same as the Weff given in the model Level 1, 2, 3, and 6 sections. The term $2 \cdot WDscaled$ is not subtracted.

Effective Saturation Current Calculations

For ACM=2, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define:

$$val \; = \; JSscaled \cdot ASeff + JSWscaled \cdot PSeff$$

If val > 0 then,

$$isbs \; = \; val$$

Otherwise,

$$isbs \; = \; M \cdot IS$$

Drain Diode Saturation Current

Define:

$$val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$$

If val > 0 then,

$$isbd = val$$

Otherwise,

$$isbd = M \cdot IS$$

Effective Drain and Source Resistances

For ACM=2, the effective drain and source resistances are calculated as follows.

Source Resistance

If NRS is specified then,

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M}\right)$$

Otherwise,

$$RSeff = \frac{RSC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RS}{Weff}$$

Drain Resistance

If NRD is specified then,

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M}\right)$$

Otherwise,

$$RDeff \ = \ \frac{RDC}{M} + \frac{HDIFeff \cdot RSH + (LDscaled + LDIFscaled) \cdot RD}{Weff}$$

ACM = 3 MOS Diode

The ACM=3 is used to model MOS diodes of the stacked devices properly. Also, the CJGATE model parameter separately models the drain and source periphery capacitances along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. CJGATE defaults to CJSW, which, in turn, defaults to 0.

The AD, AS, PD, PS calculations depend on the layout of the device, which is determined by the value of element parameter GEO. The GEO can be specified on the MOS element description. It can have the following values:

GEO=0: indicates the drain and source of the device are not shared by other devices (default).

GEO=1: indicates the drain is shared with another device.

GEO=2: indicates the source is shared with another device.

GEO=3: indicates the drain and source are shared with another device.

Figure 15-14: – Stacked Devices and Corresponding GEO Values

Effective Areas and Peripheries Calculations

For ACM=3, the effective areas and peripheries are calculated differently, depending on the value of GEO.

If AD is not specified, then,

For GEO=0 or 2,

$$ADeff \ = \ 2 \cdot HDIFeff \cdot Weff$$

For GEO=1 or 3,

$$ADeff \ = \ HDIFeff \cdot Weff$$

Otherwise,

$$ADeff \ = \ M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

If AS is not specified, then,

For GEO=0 or 1,

$$ASeff \ = \ 2 \cdot HDIFeff \cdot Weff$$

For GEO=2 or 3,

$$ASeff \ = \ HDIFeff \cdot Weff$$

Otherwise,

$$ASeff \ = \ M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

If PD is not specified, then,

For GEO=0 or 2,

$$PDeff \ = \ 4 \cdot HDIFeff + Weff$$

For GEO=1 or 3,

$$PDeff \ = \ 2 \cdot HDIFeff$$

Otherwise,

$$PDeff \ = \ M \cdot PD \cdot WMLT \cdot SCALE$$

If PS is not specified, then,

For GEO=0 or 1,

$$PSeff \ = \ 4 \cdot HDIFeff + Weff$$

For GEO=2 or 3,

$$PSeff \ = \ 2 \cdot HDIFeff$$

Otherwise,

$$PSeff \ = \ M \cdot PS \cdot WMLT \cdot SCALE$$

The Weff and HDIFeff is calculated as follows:

$$Weff \ = \ M \cdot (Wscaled \cdot WMLT + XWscaled)$$

$$HDIFeff \ = \ HDIFscaled \cdot WMLT$$

Note: *The Weff is not quite the same as the Weff given in the model LEVEL 1,*
2, 3, and 6 sections. The term $2 \cdot WDscaled$ *is not subtracted.*

Effective Saturation Current Calculations

The ACM=3 model calculates the MOS diode effective saturation currents the
same as ACM=2.

Effective Drain and Source Resistances

The ACM=3 model calculates the effective drain and source resistances the
same as ACM=2.

Using MOS Diode Equations

This section describes the MOS diode equations.

DC Current

The drain and source MOS diodes are paralleled with GMINDC conductance in the DC analysis and with GMIN in the transient analysis. The total DC current is the sum of diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

vbs > 0,

$$ibs = isbs \cdot (e^{vbs/(N \cdot vt)} - 1)$$

vbd > 0,

$$ibd = isbd \cdot (e^{vbd/(N \cdot vt)} - 1)$$

Drain and Source Diodes Reverse Biased

For 0>vbs>VNDS,

$$ibs = gsbs \cdot vbs$$

For vbs < VNDS,

$$ibs = gsbs \cdot VNDS + \left(\frac{gsbs}{NDS}\right) \cdot (vbs - VNDS)$$

For 0 > vbd > VNDS,

$$ibd = gsbd \cdot vbd$$

For vbd < VNDS,

$$ibd = gsbd \cdot VNDS + \left(\frac{gsbd}{NDS}\right) \cdot (vbd - VNDS)$$

where

$$|gsbs| = |isbs| \, , and \, |gdbd| = |isbd|$$

MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. The diffusion capacitance is evaluated in both in terms of the small signal conductance of the diode and a model parameter TT, representing the transit time of the diode. The depletion capacitance depends on the choice of ACM, and is discussed below.

The bias-dependent depletion capacitance must be calculated by defining the intermediate quantities: C0BS, C0BD, C0BS_SW, and C0BD_SW, which depend on geometric parameters, such as ASeff and PSeff calculated under various ACM specifications.

When ACM=3, the intermediate quantities C0BS_SW, and C0BD_SW include an extra term to account for CJGATE.

For ACM=2, the parameter CJGATE has been added in a backward compatible manner. Therefore, the default behavior of CJGATE makes the intermediate quantities C0BS_SW and C0BD_SW the same as for previous versions. The default patterns are:

If neither CJSW nor CJGATE is specified, both default to zero.

If CJGATE is not specified, it defaults to CJSW, which in turn defaults to zero.

If CJGATE is specified, and CJSW is not specified, then CJSW defaults to zero.

The intermediate quantities C0BS, C0BS_SW, C0BD, and C0BD_SW are calculated as follows.

```
C0BS = CJscaled*ASeff
C0BD = CJscaled*ADeff
```

If (ACM= 0 or 1), then:

```
C0BS_SW = CJSWscaled*PSeff
C0BD_SW = CJSWscaled*PDeff
```

If (ACM=2):

If (PSeff < Weff), then:

```
C0BS_SW = CJGATEscaled*PSeff
```
Otherwise:

```
C0BS_SW = CJSWscaled*(PSeff-Weff) + CJGATEscaled*Weff
```
If (PDeff < Weff), then:

```
C0BD_SW = CJGATEscaled*PDeff
```
Otherwise:

```
C0BD_SW = CJSWscaled*(PDeff-Weff) + CJGATEscaled*Weff
```

if (ACM=3), then:

```
C0BS_SW = CJSWscaled*PSeff + CJGATEscaled*Weff
C0BD_SW = CJSWscaled*PDeff + CJGATEscaled*Weff
```

Source Diode Capacitance

If (C0BS + C0BS_SW) > 0, then:
For vbs < 0,

$$
vbs \ = \ TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 - \frac{vbs}{PB}\right)^{-\prime}
$$

$$
C0BS\_SW \cdot \left(1 - \frac{vbs}{PHP}\right)^{-MJSW}
$$

For vbs > 0,

$$
vbs \ = \ TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{v}{P}\right.
$$

$$
C0BS\_SW \ \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right.
$$

Otherwise, if (C0BS + C0BS_SW) ≤ 0, then:
For vbs < 0,

$$capbs \ = \ TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$$

For vbs > 0,

$$\imath bs \ = \ TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{v\iota}{P}\right.$$

Drain Diode Capacitance

If (C0BD + C0BD_SW) > 0, then:
For vbd < 0,

$$capbd \ = \ TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ}$$

$$PDeff \cdot C0BD\_SW \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For vbd > 0,

$$\imath bd \ = \ TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{v\iota}{P}\right.$$
$$C0BD\_SW \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right.$$

Otherwise, if (ADeff · CJscaled + PDeff · CJSWscaled) ≤ 0, then:
For vbd < 0,

$$\imath apbd \ = \ TT \cdot \frac{\partial\ bd}{\partial vbd} + M \cdot CBD \cdot \left(1 - \frac{vbd}{PB}\right)^{-m}$$

For vbd > 0,

$$\imath pbd \ = \ TT \cdot \frac{\partial ibd}{\partial vbd} + M \cdot CBD \cdot \left(1 + MJ \cdot \frac{vb}{P\iota}\right.$$

Using Common Threshold Voltage Equations

This section describes the common threshold voltage equations.

Common Threshold Voltage Parameters

The parameters described in this section are applicable to all MOSFET models except Levels 5 and 13.

Name(Alias)	Units	Default	Description
DELVTO	V	0.0	zero-bias threshold voltage shift
GAMMA	$V^{1/2}$	0.5276 25	body effect factor. If GAMMA is not set, it is calculated from NSUB.
NGATE	cm^3		polysilicon gate doping, used for analytical model only. Undoped polysilicon is represented by a small value. If NGATE $\leq$ 0.0, it is set to 1e+18.
NSS	$1/cm^2$	1.0	surface state density
NSUB (DNB, NB)	$1/cm^3$	1e15	substrate doping
PHI	V	0.5760 36	surface potential. NSUB default=1e15.
TPG (TPS)		1.0	type of gate material, used for analytical model only Level 4 TPG default=0 where TPG = 0 al-gate TPG = 1 gate type same as source-drain diffusion TPG = -1 fate type opposite to source-drain diffusion
VTO (VT)	V		zero-bias threshold voltage

Calculation of PHI, GAMMA, and VTO

The model parameters PHI, GAMMA, and VTO are used in threshold voltage calculations. If these parameters are not user-specified, they are calculated as follows, except for the Level 5 model.

If PHI is not specified, then,

$$PHI = 2 \cdot vt \cdot \ln\left(\frac{NSUB}{ni}\right)$$

If GAMMA is not specified, then,

$$GAMMA = \frac{(2 \cdot q \cdot \varepsilon si \cdot NSUB)^{1/2}}{COX}$$

The energy gap, eg, and intrinsic carrier concentration for the above equations are determined by:

$$eg = 1.16 - 7.02e\text{-}4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e{+}10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]}(1/\text{cm}^3)$$

where,

$$tnom = TNOM + 273.15$$

If VTO is not specified, then for Al-Gate (TPG=0), the work function Φms is determined by:

$$\Phi ms = -\frac{eg}{2} - type \cdot \frac{PHI}{2} - 0.05$$

where type is +1 for n-channel and -1 for p-channel.

For Poly-Gate (TPG=±1), the work function is determined by:

If the model parameter NGATE is not specified,

$$\Phi ms \ = \ type \cdot \left(- \ TPG \cdot \frac{eg}{2} - \frac{PHI}{2} \right)$$

Otherwise,

$$\Phi ms \ = \ type \cdot \left[- \ TPG \cdot vt \cdot \ln\left(\frac{NGATE \cdot 1e6}{ni} \right) - \frac{PHI}{2} \right]$$

Then VTO voltage is determined by:

$$VTO \ = \ vfb + type \cdot (GAMMA \cdot PHI^{1/2} + PHI)$$

where,

$$vfb \ = \ \Phi ms - \frac{q \cdot NSS}{COX} + DELVTO$$

If VTO is specified, then,

$$VTO \ = \ VTO + DELVTO$$

Performing MOSFET Impact Ionization

The impact ionization current for MOSFETs is available for all levels. The controlling parameters are ALPHA, VCR, and IIRAT. The parameter IIRAT sets the fraction of the impact ionization current that goes to the source.

```
I_ds = I_ds_normal + IIRAT·I_impact
I_db = I_db_diode + (1-IIRAT)·I_impact
```

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

Impact Ionization Model Parameters

Name(Alias)	Units	Default	Description
ALPHA	1/V	0.0	impact ionization current coefficient
LALPHA	µm/V	0.0	ALPHA length sensitivity
WALPHA	µm/V	0.0	ALPHA width sensitivity
VCR	V	0.0	critical voltage
LVCR	µm · V	0.0	VCR length sensitivity
WVCR	µm · V	0.0	VCR width sensitivity
IIRAT		0.0	portion of impact ionization current that goes to source

Impact Ionization Equations

The current I_impact due to impact ionization effect is calculated as follows:

$$\text{I\_impact} = Ids \cdot ALPHAeff \cdot (vds - vdsat) \cdot e^{\frac{-VCReff}{vds - vdsat}}$$

where

$$ALPHAeff = ALPHA + LALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff} \right)$$

$$WALPHA \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFe} \right.$$

$$VCReff = VCR + LVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREFeff} \right)$$

$$WVCR \cdot 1e\text{-}6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREFe} \right.$$

where

$$LREFeff = LREF + XLREF - 2 \cdot LD \text{ and}$$

$$WREFeff = WREF + XWREF - 2 \cdot WD$$

Effective Output Conductance

The element template output allows gds to be output directly, for example,
```
.PRINT I(M1) gds=LX8(M1)
```

However, when using impact ionization current, it is important to note that gds is the derivative of I_{ds} only, rather than the total drain current, which is $I_{ds}+I_{db}$. The complete drain output conductance is

$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of device M1,
```
.PRINT rout=PAR('1.0/(LX8(M1)+LX10(M1))')
```

**Figure 15-15: Drain, Source, and Bulk Currents for vgs=3, with
IIRAT=0.5**

Cascode Example

Drain to bulk impact ionization current limits the use of cascoding to increase
output impedance. The following cascode example shows the affect of changing
IIRAT. When IIRAT is less than 1.0, the drain to bulk current lowers the output
impedance of the cascode stage.

**Figure 15-16: Low-frequency AC Analysis Measuring Output
Impedance**

Cascode Circuit

Example

iirat	gout_ac	rout
0.0	8.86E-6	113 K
0.5	4.30E-6	233 K
1.0	5.31E-8	18.8 Meg

Input File:

```
$ cascode test
.param pvds=5.0 pvref=1.4 pvin=3.0

vdd dd 0 pvds ac 1
$ current monitor vd
vd  dd d 0
vin in 0 pvin
vref ref 0 pvref
x1 d in ref cascode
.macro cascode out in ref
m1  out in 1 0    n L=1u W=10u
mref 1 ref 0 0    n L=1u W=10u
.eom

.param xiirat=0
.ac dec 2 100k 1x sweep xiirat poi 3   0, 0.5, 1.0
.print  ir(vd)
.measure  gout_ac avg ir(vd)

.model n nmos level=3
+ tox=200 vto=0.8 gamma=0.7 uo=600 kappa=0.05
+ alpha=1 vcr=15 iirat=xiirat
.end
```

MOS Gate Capacitance Models

Capacitance model parameters can be used with all MOSFET model statements.

Model charge storage using fixed and nonlinear gate capacitances and junction capacitances. Gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances are represented by three fixed-capacitance parameters: CGDO, CGSO, and CGBO. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of model parameter CAPOP.

Model MOS gate capacitances, as a nonlinear function of terminal voltages, using Meyer's piece-wise linear model for all MOS levels. The charge conservation model is also available for MOSFET model Levels 2, 3, 4, 5, 6, 7, 13, and 27. For Level 1, the model parameter TOX must be specified to invoke the Meyer model. The Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models are described in detail in the following subsections.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause "timestep too small" errors when no other nodal capacitances are present.

Capacitor Model Selection

Gate capacitance model selection has been expanded to allow various combinations of capacitor models and DC models. Older DC models can now be incrementally updated with the new capacitance equations without having to move to a new DC model. You can select the gate capacitance with the CAPOP model parameter to validate the effects of different capacitance models.

The capacitance model selection parameter CAPOP is associated with the MOS models. Depending on the value of CAPOP, different capacitor models are used to model the MOS gate capacitance: the gate-to-drain capacitance, the gate-to-source capacitance, or the gate-to-bulk capacitance. CAPOP allows for the selection of several versions of the Meyer and charge conservation model.

Some of the capacitor models are tied to specific DC models (DC model level in parentheses below). Others are designated as general and can be used by any DC model.

CAPOP=0	SPICE original Meyer model (general)
CAPOP=1	modified Meyer model (general)
CAPOP=2	parameterized Modified Meyer model (general default)
CAPOP=3	parameterized Modified Meyer model with Simpson integration (general)
CAPOP=4	charge conservation model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	no capacitor model
CAPOP=6	AMI capacitor model (Level 5)
CAPOP=9	charge conservation model (Level 3)
CAPOP=13	generic BSIM model (default for Levels 13, 28, 39)
CAPOP=11	Ward-Dutton model (specialized, Level 2)
CAPOP=12	Ward-Dutton model (specialized, Level 3)
CAPOP=39	BSIM 2 Capacitance model (Level 39)

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the given DC model.

Table 15-6: CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12
13, 28, 39	13	13
other levels	2	11

The proprietary models, Level 5, 17, 21, 22, 25, 31, 33, and the SOS model Level 27, have their own built-in capacitance routines.

Introduction to Transcapacitance

If you have a capacitor with two terminals, 1 and 2 with charges Q1 and Q2 on the two terminals that sum to zero, for example, Q1=−Q2, the charge is a function of the voltage difference between the terminals, V12=V1−V2. The small-signal characteristics of the device are completely described by one quantity, C=dQ1/dV12.

If you have a four-terminal capacitor, the charges on the four terminals must sum to zero (Q1+Q2+Q3+Q4=0), and they can only depend on voltage differences, but they are otherwise arbitrary functions. So there are three independent charges, Q1, Q2, Q3, that are functions of three independent voltages V14, V24, V34. Hence there are nine derivatives needed to describe the small-signal characteristics.

It is convenient to consider the four charges separately as functions of the four terminal voltages, Q1(V1,V2,V3,V4), ... Q4(V1,V2,V3,V4). The derivatives form a four by four matrix, dQi/dVj, i=1,.4, j=1,.4. This matrix has a direct interpretation in terms of AC measurements. If an AC voltage signal is applied to terminal j with the other terminals AC grounded, and AC current into terminal i is measured, the current is the imaginary constant times 2*pi*frequency times dQi/dVj.

The fact that the charges sum to zero requires each column of this matrix to sum to zero, while the fact that the charges can only depend on voltage differences requires each row to sum to zero.

In general, the matrix is not symmetrical:

dQi/dVj need not equal dQj/dVi

This is not an expected event because it does not occur for the two terminal case. For two terminals, the constraint that rows and columns sum to zero

$$\frac{dQ1}{dV1} + \frac{dQ2}{dV1} = 0$$

$$\frac{dQ1}{dV1} + \frac{dQ1}{dV2} = 0$$

forces dQ1/dV2 = dQ2/dV1. For three or more terminals, this relation does not hold in general.

The terminal input capacitances are the diagonal matrix entries
```
Cii = dQi/dVi     i=1,.4
```

and the transcapacitances are the negative of off-diagonal entries
```
Cij = -dQi/dVj     i not equal to j
```

All of the Cs are normally positive.

Figure 15-17: MOS Capacitances

In Figure 15-17:, Cij determines the current transferred out of node i from a voltage change on node j. The arrows, representing direction of influence, point from node j to node i.

A MOS device with terminals D G S B provides the following:

$$CGG = \frac{dQg}{dVG}$$

$$CGD = -\frac{dQg}{dVD}$$

$$CDG = -\frac{dQD}{dVG}$$

CGG represents input capacitance: a change in gate voltage requires a current equal to CGG×dVG/dt into the gate terminal. CGD represents Miller feedback: a change in drain voltage gives a current equal to CGG×dVG/dt out of the gate terminal. CDG represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To see how CGD might not be equal to CDG, the following example presents a simplified model with no bulk charge, with gate charge a function of VGS only, and 50/50 partition of channel charge into QS and QD:

$$QG = Q(vgs)$$

$$QS = -0.5 \cdot Q(vgs)$$

$$QD = -0.5 \cdot Q(vgs)$$

$$QB = 0$$

As a result of this:

$$CGD = -\frac{dQG}{dVD} = 0$$

$$CGD = -\frac{dQD}{dVG} = 0.5 \cdot \frac{dQ}{dvgs}$$

Therefore, in this model there is Miller feedthrough, but no feedback.

Operating Point Capacitance Printout

Six capacitances are reported in the operating point printout:

cdtot	dQD/dVD
cgtot	dQG/dVG
cstot	dQS/dVS
cbtot	dQB/dVB
cgs	-dQG/dVS
cgd	-dQG/dVD

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element, that is, physical instead of electrical.

For the Meyer models, where the charges QD and so on are not well defined, the printout quantities are

cdtot	cgd+cdb
cgtot	cgs+cgd+cgb
cstot	cgs+csb
cbtot	cgb+csb+cdb
cgs	cgs
cgd	cgd

Element Template Printout

The MOS element template printouts for gate capacitance are LX18 – LX23 and LX32 – LX34. From these nine capacitances the complete four by four matrix of transcapacitances can be constructed. The nine LX printouts are:

```
LX18(m)  =  dQG/dVGB  =  CGGBO
LX19(m)  =  dQG/dVDB  =  CGDBO
LX20(m)  =  dQG/dVSB  =  CGSBO
LX21(m)  =  dQB/dVGB  =  CBGBO
LX22(m)  =  dQB/dVDB  =  CBDBO
LX23(m)  =  dQB/dVSB  =  CBSBO
LX32(m)  =  dQD/dVG  =  CDGBO
LX33(m)  =  dQD/dVD  =  CDDBO
LX34(m)  =  dQD/dVS  =  CDSBO
```

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element, that is, physical instead of electrical.

For an NMOS device with source and bulk grounded, LX18 represents the input capacitance, LX33 the output capacitance, -LX19 the Miller feedback capacitance (gate current induced by voltage signal on the drain), and -LX32 represents the Miller feedthrough capacitance (drain current induced by voltage signal on the gate).

A device that is operating with node 3 as electrical drain, for example, an NMOS device with node 3 at higher voltage than node 1 is said to be in reverse mode. The LXs are physical, but you can translate them into electrical definitions by interchanging D and S:

```
CGG(reverse) = CGG = LX18
CDD(reverse) = CSS = dQS/dVS = d(-QG-QB-QD)/dVS = -
LX20-LX23-LX34
CGD(reverse) = CGS = -LX20
CDG(reverse) = CSG = -dQS/dVG = d(QG+QB+QD)/dVG =
LX18+LX21+LX32
```

For the Meyer models, the charges QD, and so forth, are not well defined. The formulas LX18= CGG, LX19= -CGD, and so forth, are still true, but the transcapacitances are symmetrical; for example, CGD=CDG. In terms of the six independent Meyer capacitances, cgd, cgs, cgb, cdb, csb, cds, the LX printouts are:

```
LX18(m)  = CGS+CGD+CGB
LX19(m)  = LX32(m)  = -CGD
LX20(m)  = -CGS
LX21(m)  = -CGB
LX22(m)  = -CDB
LX23(m)  = -CSB
LX33(m)  = CGD+CDB+CDS
LX34(m)  = -CDS
```

Example Gate Capacitance Calculation

This example shows a gate capacitance calculation in detail for a BSIM model. TOX is chosen so that

$$\frac{eox}{tox} = 1e - 3F/m^2$$

Vfb0, phi, k1 are chosen so that vth=1v. The AC sweep is chosen so that $2 \cdot \pi \cdot freq = 1e6s^{-1}$ for the last point.

HSPICE Input File

```
$
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 5
vg g 0 5 ac 1
vb b 0 0
.ac dec 1 1.59155e4 1.59155e5
.print   CGG=lx18(m) CDD=lx33(m) CGD=par('-lx19(m)')
CDG=par('-lx32(m)')
.print   ig_imag=ii2(m)  id_imag=ii1(m)
.model nch nmos level=13 update=2
+ xqc=0.6 toxm=345.315 vfb0=-1 phi0=1 k1=1.0 muz=600
mus=650 acm=2
+ xl=0 ld=0.1u meto=0.1u cj=0.5e-4 mj=0 cjsw=0
.alter
vd d 0 5 ac 1
vg g 0 5
.end
```

Calculations

$$Leff = 0.6u$$

$$\frac{eox}{tox} = 1e - 3F/m^2$$

$$Cap = \frac{Leff \cdot Weff \cdot eox}{tox} = 60e - 15F$$

BSIM equations for internal capacitance in saturation with xqc=0.4:

$$body = 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364 \cdot (PHI0 + vsb))}\right) \cdot \frac{K1}{\sqrt{(PHI0 + vsb)}}$$

$$1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364)}\right) = 1.3C$$

$$cgg = Cap \cdot \left(1 - \frac{1}{(3 \cdot body)}\right) = Cap \cdot 0.7448 = 44.69F$$

$$cgd = 0$$

$$cdg = \left(\frac{4}{15}\right) \cdot Cap = 16F$$

$$cdd = 0$$

Gate-drain overlap $= (ld + meto) \cdot Weff \cdot \dfrac{eox}{tox} = 20e - 15F$

Adding the overlaps,

$$cgg = 44.69F + 2 \cdot 20F = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 20F$$

Drain-bulk diode cap $cj \cdot ad = (0.5e - 4) \cdot (200e - 12) = 1$

Adding the diodes,

$$cgg = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 30F$$

HSPICE Results

```
subckt
element  0:m
model    0:nch
cdtot     30.0000f
cgtot     84.6886f
cstot     74.4684f
cbtot     51.8898f
cgs       61.2673f
cgd       20.0000f
freq        cgg          cdd         cgd         cdg
15.91550k  84.6886f    30.0000f  20.0000f   35.9999f
159.15500k 84.6886f    30.0000f   20.0000f   35.9999f
freq        ig_imag       id_imag
15.91550k   8.4689n      -3.6000n
159.15500k  84.6887n     -35.9999n
Alter results
freq      ig_imag         id_imag
15.91550k     -2.0000n     3.0000n
159.15500k   -20.0000n  30.0000n
```

The calculation and the HSPICE results match.

Plotting Gate Capacitances

This input file shows how to plot gate capacitances as a function of bias. The .OPTION DCCAP needs to be set to turn on capacitance calculations for a DC sweep. The model used is the same as for the above calculations.

Example

```
$ gate capacitance plots
.option dccap=1 post
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 0
vg g 0 5
vb b 0 0
.dc vd 0 5 .1
.print   vds=v(d) CGG=lx18(m)
+        CGD=par('-lx19(m)') CDG=par('-lx32(m)')
+        CGS=par('-lx20(m)')
CSG=par('lx18(m)+lx21(m)+lx32(m)')
+        CGB=par('lx18(m)+lx19(m)+lx20(m)')
CBG=par('-lx21(m)')

.model nch nmos
+ level=13 update=2 xqc=0.6 toxm=345.315
+ vfb0=-1 phi0=1 k1=1.0 muz=600 mus=650
+ acm=2 xl=0 ld=0.1u meto=0.1u
+ cj=0.5e-4 mj=0 cjsw=0
.end
```
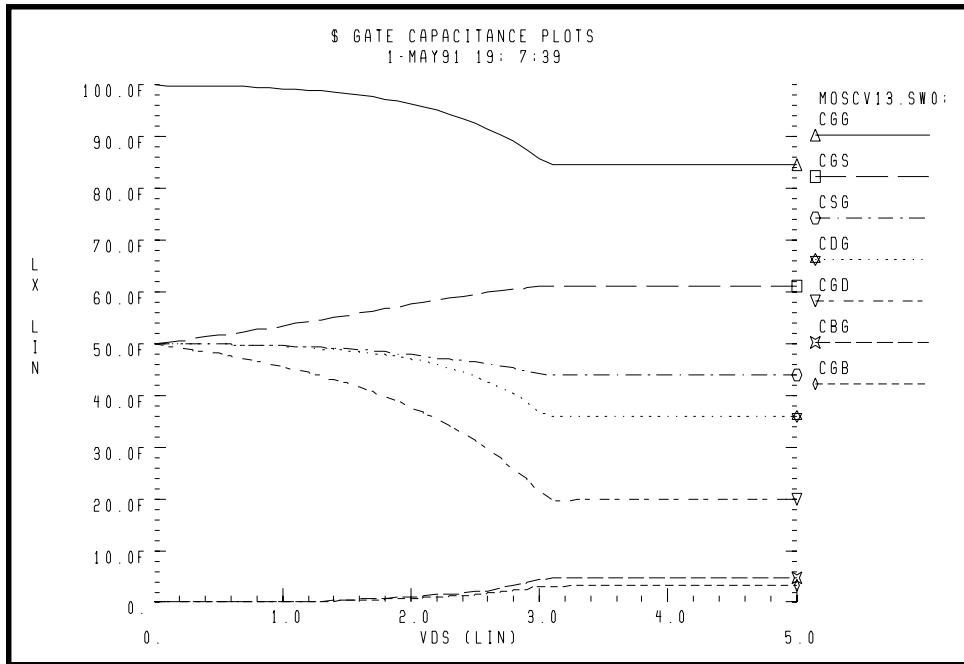
Figure 15-18: Gate Capacitance

Capacitance Control Options

The control options affecting the CAPOP models are SCALM, CVTOL, DCSTEP, and DCCAP. SCALM scales the model parameters, CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see "CAPOP=3 — Gate Capacitances (Simpson Integration)" on page 15-90). DCSTEP models capacitances with a conductance during DC analysis. DCCAP invokes calculation of capacitances in DC analysis.

Scaling

The parameters scaled by the option SCALM are: CGBO, CGDO, CGSO, COX, LD, and WD. SCALM scales these parameters according to fixed rules that are a function of the parameter's units. When the model parameter's units are in meters, the parameter is multiplied by SCALM. For example, the parameter LD has units in meters, its scaled value is obtained by multiplying the value of LD by SCALM. When the units are in meters squared, the parameter is multiplied by $SCALM^2$. If the units are in reciprocal meters, the parameter's value is divided by SCALM. For example, since CGBO is in farads/meter the value of CGBO is divided by SCALM. When the units are in reciprocal meters squared, then the parameter is divided by $SCALM^2$. The scaling equations specific to each CAPOP level are given in the individual CAPOP subsections.

MOS Gate Capacitance Model Parameters

Basic Gate Capacitance Parameters

Name(Alias)	Units	Default	Description
CAPOP		2.0	capacitance model selector
COX (CO)	F/m^2	3.453e-4	oxide capacitance. If COX is not input, it is calculated from TOX. The default value corresponds to the TOX default of 1e-7: COXscaled = $COX/SCALM^2$
TOX	m	1e-7	represents the oxide thickness, calculated from COX when COX is input. Program uses default if COX is not specified. For TOX>1, unit is assumed to be Angstroms. There can be a level-dependent default that overrides.

Gate Overlap Capacitance Model Parameters

Name(Alias)	Units	Default	Description
CGBO (CGB)	F/m	0.0	gate-bulk overlap capacitance per meter channel length. If CGBO is not set but WD and TOX are set, then CGBO is calculated. CGBOscaled = CGBO/SCALM
CGDO (CGD, C2)	F/m	0.0	gate-drain overlap capacitance per meter channel width. If CGDO is not set but LD or METO and TOX are set, then CGDO is calculated. CGDOscaled = CGDO/SCALM
CGSO *(CGS, C1)*	F/m	0.0	gate-source overlap capacitance per meter channel width. If CGSO is not set but LD or METO and TOX are set, then CGSO is calculated. CGSOscaled = CGSO/SCALM
LD (LATD, DLAT)	m		lateral diffusion into channel from source and drain diffusion. When both LD and XJ are unspecified: LD default=0.0. If LD is not set but XJ is specified, then LD is calculated from XJ. LD default=0.75 · XJ for all levels except Level 4, for which LD default=0.75. LDscaled = LD · SCALM Level 4: LDscaled = LD · XJ · SCALM
METO	m	0.0	fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation METOscaled = METO · SCALM
WD	m	0.0	lateral diffusion into channel from bulk along width WDscaled = WD · SCALM

Meyer Capacitance Parameters CAPOP=0, 1, 2

Name(Alias)	Units	Default	Description
CF1	V	0.0	modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (only for CAPOP=2)
CF2	V	0.1	modified MEYER control for transition of cgs from weak to strong inversion region (only for CAPOP=2)
CF3		1.0	modified MEYER control for transition of cgs and cgd from saturation to linear region as a function of vds (only for CAPOP=2)
CF4		50.0	modified MEYER control for contour of cgb and cgs smoothing factors
CF5		0.667	modified MEYER control capacitance multiplier for cgs in saturation region
CF6		500.0	modified MEYER control for contour of cgd smoothing factor
CGBEX		0.5	cgb exponent (only for CAPOP=1)

Charge Conservation Parameter, CAPOP=4

Name(Alias)	Units	Default	Description
XQC		0.5	coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases.

XQC & XPART Specification for CAPOP=4, 9, 11, 12 and 13

Parameter rule for gate capacitance charge sharing coefficient, XQC & XPART, in the saturation region:

- If neither XPART or XQC is specified, the 0/100 model is used.
- If both XPART and XQC are specified, XPART overrides XQC.
- If XPART is specified:

XPART=0 → 40/60

XPART=0.4 → 40/60

XPART=0.5 → 50/50

XPART=1 → 0/100

XPART = any other value less than 1 → 40/60

XPART >1 → 0/100If XQC is specified:

XQC=0 → 0/100

XQC=0.4 → 40/60

XQC=0.5 → 50/50

XQC=1 → 0/100

XQC = any other value less than 1 → 40/60

XQC>1 → 0/100

The only difference is the treatment of the parameter value 0.

After XPART/XQC is specified, the gate capacitance is ramped from 50/50 at Vds=0 volt (linear region) to the value (with Vds sweep) in the saturation region specified by XPART/XQC. This charge sharing coefficient ramping will assure the smoothness of the gate capacitance characteristic.

Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly, or the program calculates them. These overlap capacitors are added into the respective voltage-variable capacitors before integration and the DC operating point reports the combined parallel capacitance.

Gate to Bulk Overlap Capacitance

If CGBO is specified,

$$CGBOeff = M \cdot Leff \cdot CGBOscaled$$

Otherwise,

$$CGBOeff = 2 \cdot WDscaled \cdot Leff \cdot COXscaled \cdot M$$

Gate to Source Overlap Capacitance

If CGSO is specified,

$$CGSOeff = Weff \cdot CGSOscaled$$

Otherwise,

$$CGSOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

Gate to Drain Overlap Capacitance

If CGDO is specified,

$$CGDOeff = Weff \cdot CGDOscaled$$

Otherwise,

$$CGDOeff = Weff \cdot (LDscaled + METOscaled) \cdot COXscaled$$

The Leff is calculated for each model differently, and it is given in the corresponding model section. The Weff calculation is not quite the same as weff given in the model Level 1, 2, 3, 6, 7 and 13 sections.

$$Weff = M \cdot (Wscaled \cdot WMLT + XWscaled)$$

The 2·WDscaled factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition:

$$cap = COXscaled \cdot Weff \cdot Leff$$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vth-PH1

$$cgb = cap$$

Depletion, vgs < vth

$$cgb = cap \cdot \frac{vth - vgs}{PH1}$$

Strong Inversion, vgs ≥ vth

$$cgb = 0$$

Gate-Source Capacitance (cgs)

Accumulation, $vgs \leq vth - \dfrac{PHI}{2}$

$$cgs = 0$$

Depletion, vgs ≤ vth

$$cgs = CF5 \cdot cap + \frac{cap \cdot (vgs - cth)}{0.75 \cdot PHI}$$

Strong Inversion Saturation Region, vgs > vth and vds ≥ vdsat

$$cgs = CF5 \cdot cap$$

Strong Inversion Linear Region, vgs > vth and vds < vdsat

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vdsat - vds}{2 \cdot (vdsat + vsb) - vds - vsb} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

The gate-drain capacitance has value only in the linear region.

Strong Inversion Linear Region, vgs > vth and vds < vdsat

$$cgd = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vdsat + vsb}{2 \cdot (vdsat + vsb) - vds - vsb} \right]^2 \right\}$$

Example

```
*file capop0.sp---capop=0 capacitances
*
*this file is used to create spice meyer gate c-v
```

```
plots
**
*(capop=0) for low vds and high vds
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)')
cgd_vdsp05=par('-lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-
lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances
for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances
for vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*******************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ uo = 817 ucrit = 3.04e4 phi=.6
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ tox = 9.77e-8 cj = 0 cjsw = 0 js = 0
+ capop=0 )
.end
```
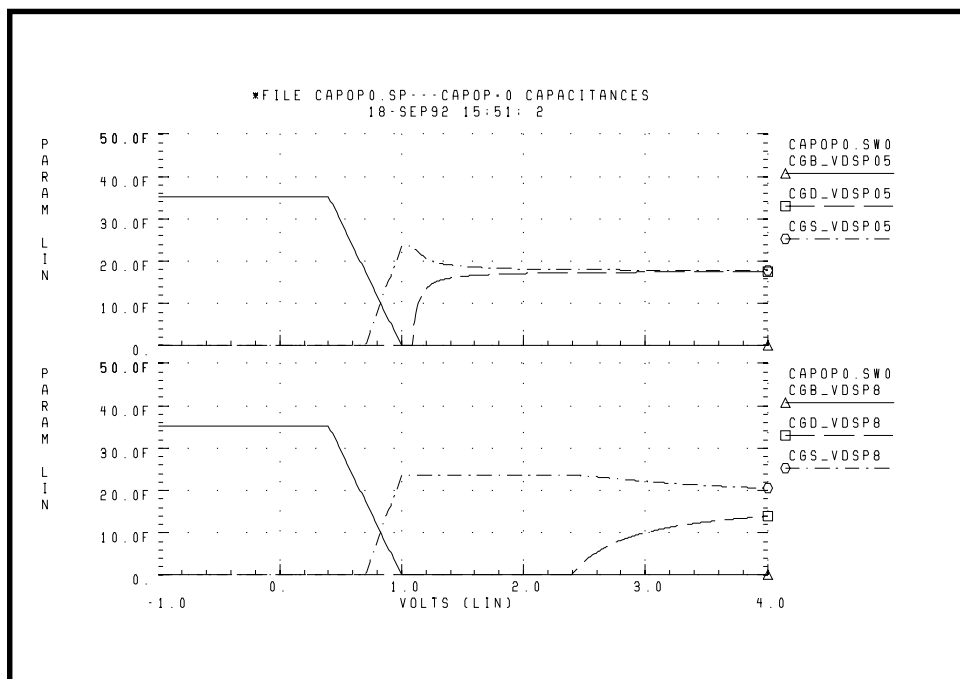
Figure 15-19: CAPOP=0 Capacitances

CAPOP=1 — Modified Meyer Gate Capacitances

Define

$$cap = COXscaled \cdot Weff \cdot Leff$$

In the following equations, G^-, G^+, D^-, and D^+ are smooth factors. They are not user-defined parameters.

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb – vsb

$$cgb = cap$$

Depletion, vgs ≤vth

$$cgb = \frac{cap}{\left[1 + 4 \cdot \dfrac{vgs + vsb - vfb}{GAMMA^2}\right]^{CGBEX}}$$

Strong Inversion, vgs > vth

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \dfrac{GAMMA \cdot (vsb + PHI)^2 + vsb + PHI}{GAMMA^2}\right]^{CGBEX}}$$

Note: In the above equations, GAMMA is replaced by effective γ for model level higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs ≤ vth

$$cgs = CF5 \cdot cap \cdot G^- \cdot D^-$$

Weak Inversion, vgs < vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{ \frac{vgs - vth}{0.1} \cdot \left[1 - \left(\frac{0.1 - vds}{0.2 - vds}\right)^2 - D^-\right] + D^- \right\}$$

Strong Inversion, vgs ≥ vth + 0.1

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds}\right]^2 \right\}$$

High vds (vds $\geq$ *0.1*)

Accumulation, vgs $\leq$vth

$$cgs = CF5 \cdot cap \cdot G^-$$

Saturation Region, vgs < vth + vds

$$cgs = CF5 \cdot cap$$

Linear Region, vgs $\geq$ vth + vds

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

Gate-Drain Capacitance (cgd)

Low vds (vds < 0.1)

Accumulation, vgs $\leq$ vth

$$cgd = CF5 \cdot cap \cdot G^- \cdot D^+$$

Weak Inversion, vgs < vth + 0.1

$$cgd = CF5 \cdot cap \cdot \left\{ D^+ + \frac{vgs - vgh}{0.1} \cdot \max\left[0, \ 1 - \left(\frac{0.1}{0.2 - vds} \right)^2 - D^+ \right] \right\}$$

Strong Inversion, vgs $\geq$ vth + 0.1

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^+, \ 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

High vds (vds $\geq$ *0.1*)

Accumulation, vgs $\leq$ vth

$$cgd \ = \ CF5 \cdot cap \cdot G^- \cdot D^+$$

Saturation Region, vgs < vth + vds

$$cgd \ = \ CF5 \cdot cap \cdot D^+$$

Strong Inversion, vgs $\geq$ vth + vds

$$cgd \ = \ CF5 \cdot cap \cdot \max\left\{ D^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}$$

Example

```
*file capop1.sp---capop1 capacitances
*
*this file creates the modified meyer gate c-v plots
*(capop=1) for low vds and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)')
cgd_vdsp05=par('-lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-
lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
```

```
for vds=0.80
*****************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*********************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ phi = 0.6 cj = 0 cjsw = 0 js = 0
+ capop=1 )
.end
```
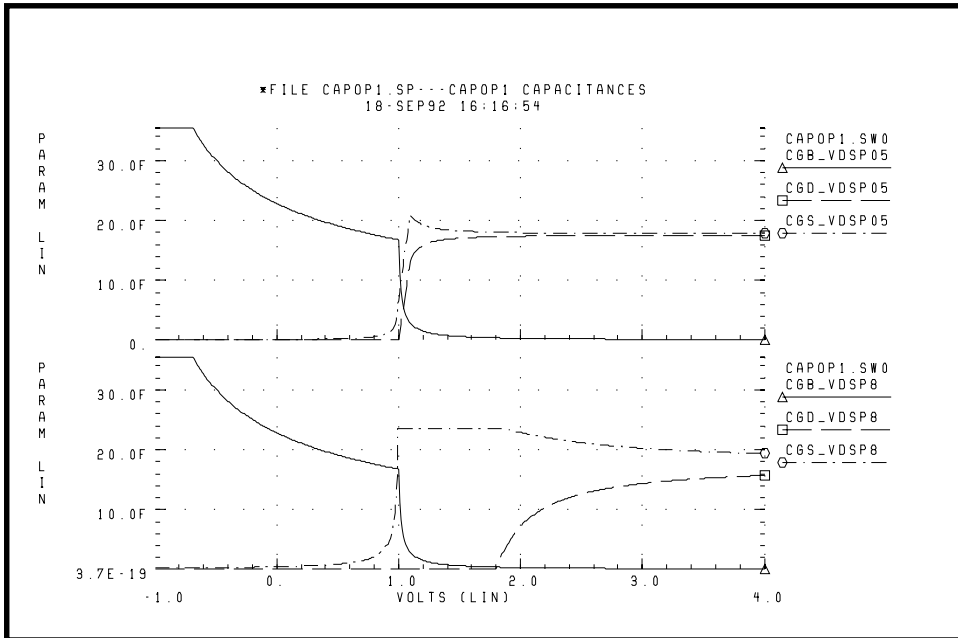

Figure 15-20: CAPOP=1 Capacitances

CAPOP=2 — Parameterized Modified Meyer Capacitances

The CAPOP=2 Meyer capacitance model is the more general form of Meyer capacitance. The CAPOP=1 Meyer capacitance model is the special case of CAPOP=2 when CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^-, G^+, D^-, and DD^+ are smooth factors. They are not user-defined parameters.

Definition

$$cap = COXscaled \cdot Weff \cdot Leff$$

Gate-Bulk Capacitance (cgb)

Accumulation, vgs ≤ vfb - vsb

$$cgb = cap$$

Depletion, vgs ≤ vth

$$cgs = \frac{cap}{\left(1 + 4 \cdot \dfrac{vgs + vsb - vfb}{GAMMA^2}\right)^{1/2}}$$

Inversion, vgs > vth

$$cgb = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \dfrac{GAMMA \cdot (PHI + vsb)^{1/2} + PHI + vsb}{GAMMA^2}\right]^{1/2}}$$

Note: In the above equations, GAMMA is replaced by effective γ for model level higher than 4.

Gate-Source Capacitance (cgs)

Low vds (vds < 0.1)

Accumulation, vgs < vth – CF1

$$cgs = CF5 \cdot cap \cdot G^- \cdot D^-$$

Depletion, vgs ≤ vth + CF2 – CF1

$$cgs = CF5 \cdot cap \cdot \left\{ \frac{vgs - vth + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{vds}{2 \cdot CF2 - vds} \right)^2 - D^- \right] + D^- \right\}$$

Strong Inversion, vgs > vth + max (CF2 – CF1, CF3 · vds) UPDATE=0

Strong Inversion, vgs > vth + CF2 – CF1,UPDATE=1

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth + CF1 - vds}{2 \cdot (vgs - vth + CF1) - vds} \right]^2 \right\}$$

High vds (vds ≥ *0.1)*

Accumulation, vgs < vth – CF1

$$cgs = CF5 \cdot cap \cdot G^- \cdot D^+, \quad CF1 \neq 0$$

$$cgs = CF5 \cdot cap \cdot G^-, \quad\quad CF1 = 0$$

Weak Inversion, vgs < vth + CF2 – CF1,   CF1 ≠ 0

$$cgs = CF5 \cdot cap \cdot \max\left(\frac{vgs - vth + CF1}{CF2}, D^+ \right)$$

Saturation Region, vgs < vth + CF3 · vds

$$cgs = CF5 \cdot cap$$

Linear Region, vgs > vth · CF3 · vds

$$cgs = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - vds}{2 \cdot (vgs - vth) - vds} \right]^2 \right\}, \quad UPDATE=0, \quad CF1=0$$

$$cgs = CG5 \cdot cap \cdot \left\{ 1 - \left[\frac{vgs - vth - CF3 \cdot vds}{2 \cdot (vgs - vth) - CF3 \cdot vds} \right]^2 \right\}, \quad UPDATE=1$$

Gate-Drain Capacitance (cgd)

Low vds, (vds < 0.1)

Accumulation, vgs ≤ vth – CF1

$$cgd = CF5 \cdot cap \cdot G^- \cdot D^-$$

Weak Inversion, vgs < vth + CF2 – CF1

$$cgd = CF5 \cdot cap \cdot \left\{ D^- + \frac{vgs - vth + CF1}{CF2} \cdot \max\left[0, \, 1 - \left(\frac{CF2}{2 \cdot CF2 - vds} \right)^2 - D^- \right] \right\}$$

Strong Inversion, vgs ≥ vth + CF2 – CF1

$$cgd = CF5 \cdot cap \cdot \max\left\{ D^-, \, 1 - \left[\frac{vgs - vth + CF1}{2 \cdot (vgs - vth + CF1) - vds} \right]^2 \right\}$$

High vds (vds > 0.1)

Accumulation, vgs ≤ vth – CF1

$$cgd = CF5 \cdot cap \cdot G^- \cdot DD^+$$

Saturation Region, vgs ≤ vth + CF3 · vds

$$cgd = CF5 \cdot cap \cdot DD^+$$

Note: In the above equation, DD^+ is a function of CF3, if UPDATE=1.

Linear Region, vgs > vth + CF3 · vds

$$cgd = CF5 \cdot cap \cdot \max\left\{DD^+, 1 - \left[\frac{vgs - vth}{2 \cdot (vgs - vth) - CF3 \cdot vds}\right]^2\right\}$$

Example

```
*file capop2.sp capop=2 capacitances
*
*this file creates parameterized modified gate
capacitances
*(capop=2) for low and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)')
cgd_vdsp05=par('-lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-
lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****************************************
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
for vds=0.05
```

```
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances
for vds=0.80
******************************************
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*********************************************
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 phi = 0.6
+ vmax = 4.59e5 cj = 0 cjsw = 0 js = 0
+ capop=2 cf1=0.15 cf2=.2 cf3=.8 cf5=.666)
.end
```
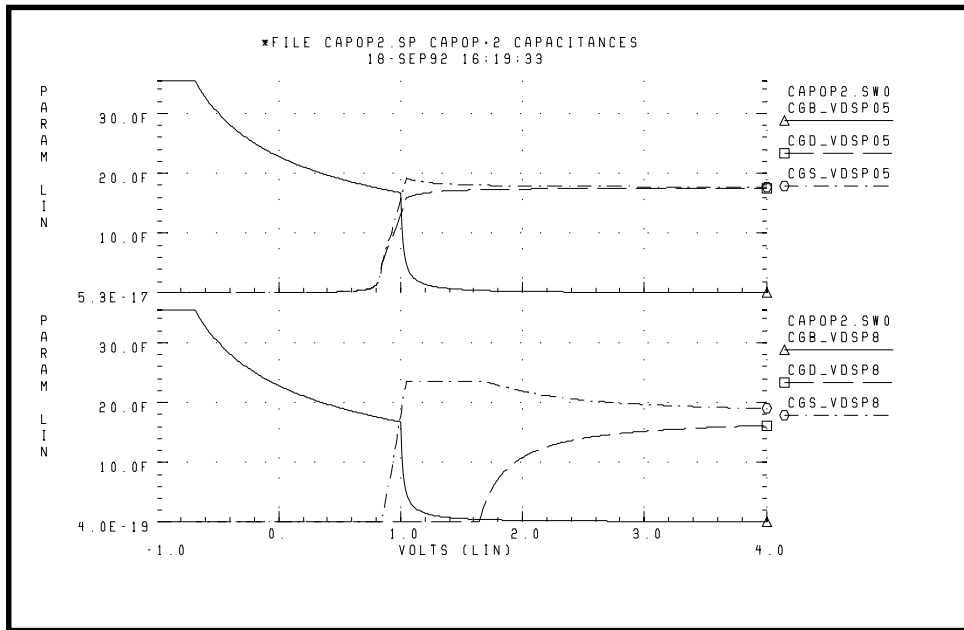

Figure 15-21: CAPOP=2 Capacitances

CAPOP=3 — Gate Capacitances (Simpson Integration)

The CAPOP 3 model is the same set of equations and parameters as the CAPOP 2 model. The charges are obtained by Simpson numeric integration instead of the box integration found in CAPOP models 1, 2, and 6.

Gate capacitances are not constant values with respect to voltages. The capacitance values can best be described by the incremental capacitance:

$$C(v) = \frac{dq(v)}{dv}$$

where q(v) is the charge on the capacitor and v is the voltage across the capacitor. The formula for calculating the differential is often intractable or difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

The charge is:

$$q(v) = \int_{0}^{v} C(v)dv$$

For the calculation of current:

$$i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right)\int_{0}^{v} C(v)dv$$

For small intervals:

$$I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$$

The integral has been approximated in SPICE by:

$$I(n+1) \ = \ \left(\frac{V(n+1)-V(n)}{t(n+1)-t(n)} \right) \cdot \left(\frac{C[V(n+1)]+C[V(n)]}{2} \right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. The charge can be estimated accurately by using Simpson's numerical integration rule. This method provides charge conservation control.

To use this model, set the model parameter CAPOP to 3 and use the existing CAPOP=2 model parameters. The OPTIONS settings RELV (relative voltage tolerance), RELMOS (relative current tolerance for MOSFETs), and CVTOL (capacitor voltage tolerance) might have to be modified. The default of 0.5 is a good nominal value for CVTOL. The option CVTOL sets the number of integration steps with the formula:

$$n \ = \ \frac{|V(n+1)-V(n)|}{CVTOL}$$

The effect of using a large value for CVTOL is to decrease the number of integration steps for the time interval n to n+1; this yields slightly less accurate integration results. Using a small CVTOL value increases the computational load, in some instances severely.

CAPOP=4 — Charge Conservation Capacitance Model

The charge conservation method (See *Ward, Donald E. and Robert W. Dutton 'A Charge-Oriented Model for MOS Transistor*) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in Level 3 models. Also channel charge partition is not continuous going from linear to saturation regions.

In HSPICE the above problems are corrected. By specifying model parameter CAPOP=4, the level-dependent recommended charge conservation model is selected. The ratio of channel charge partitioning between drain and source is selected by the model parameter XQC. For example, if XQC=.4 is set, then the saturation region 40% of the channel charge is associated to drain and the

remaining 60% is associated to the source. In the linear region, the ratio is 50/ 50. In HSPICE an empirical equation is used to make the transition from 50/50 (linear region) to 40/60 (saturation region) smoothly.

Also, the capacitance coefficients which are the derivative of gate, bulk, drain, and source charges are continuous. Model Levels 2, 3, 4, 6, 7, and 13 have a charge conservation capacitance model which is invoked by setting CAPOP=4.

In the following example the charge conservation capacitances CAPOP=4 and the improved charge conservation capacitance CAPOP=9 for the model Level 3 only is compared. The capacitances CGS and CGD for CAPOP=4 model (SPICE2G.6) show discontinuity at the saturation and linear region boundary while the CAPOP=9 model does not have discontinuity. For the purpose of comparison the modified Meyer capacitances (CAPOP=2) also is provided. The shape of CGS and CGD capacitances resulting from CAPOP=9 are much closer to those of CAPOP=2.

Example

```
FILE MCAP3.SP CHARGE CONSERVATION MOSFET CAPS.,
CAPOP=4,9 LEVEL=3
*
* CGGB = LX18(M) DERIVATIVE OF QG WITH RESPECT TO
VGB.
* CGDB = LX19(M) DERIVATIVE OF QG WITH RESPECT TO
VDB.
* CGSB = LX20(M) DERIVATIVE OF QG WITH RESPECT TO
VSB.
* CBGB = LX21(M) DERIVATIVE OF QB WITH RESPECT TO
VGB.
* CBDB = LX22(M) DERIVATIVE OF QB WITH RESPECT TO
VDB.
* CBSB = LX23(M) DERIVATIVE OF QB WITH RESPECT TO
VSB.
* CDGB = LX32(M) DERIVATIVE OF QD WITH RESPECT TO
VGB.
* CDDB = LX33(M) DERIVATIVE OF QD WITH RESPECT TO
```

```
VDB.
* CDSB = LX34(M) DERIVATIVE OF QD WITH RESPECT TO
VSB.
* THE SIX NONRECIPROCAL CAPACITANCES CGB, CBG, CGS,
CSG, CGD, AND CDG
* ARE DERIVED FROM THE ABOVE CAPACITANCE FACTORS.
*
.OPTIONS DCCAP=1 POST NOMOD
.PARAM XQC=0.4 CAPOP=4
.DC VGG -2 5 .02
.print CGB=PAR('LX18(M)+LX19(M)+LX20(M)')
+ CBG=PAR('-LX21(M)')
+ CGS=PAR('-LX20(M)')
+ CSG=PAR('LX18(M)+LX21(M)+LX32(M)')
+ CGD=PAR('-LX19(M)')
+ CDG=PAR('-LX32(M)')
.print
+ CG =par('LX14(M)')
VDD D 0 2.5
VGG G 0 0
VBB B 0 -1
M D G 0 B MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=3 COX=1E-4 VTO=.3 CAPOP=CAPOP
+ UO=1000 GAMMA=.5 PHI=.5 XQC=XQC
+ THETA=0.06 VMAX=1.9E5 ETA=0.3 DELTA=0.05 KAPPA=0.5
XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0 CJ=0 JS=0 IS=0
*
.ALTER
.PARAM CAPOP=9
.END
```
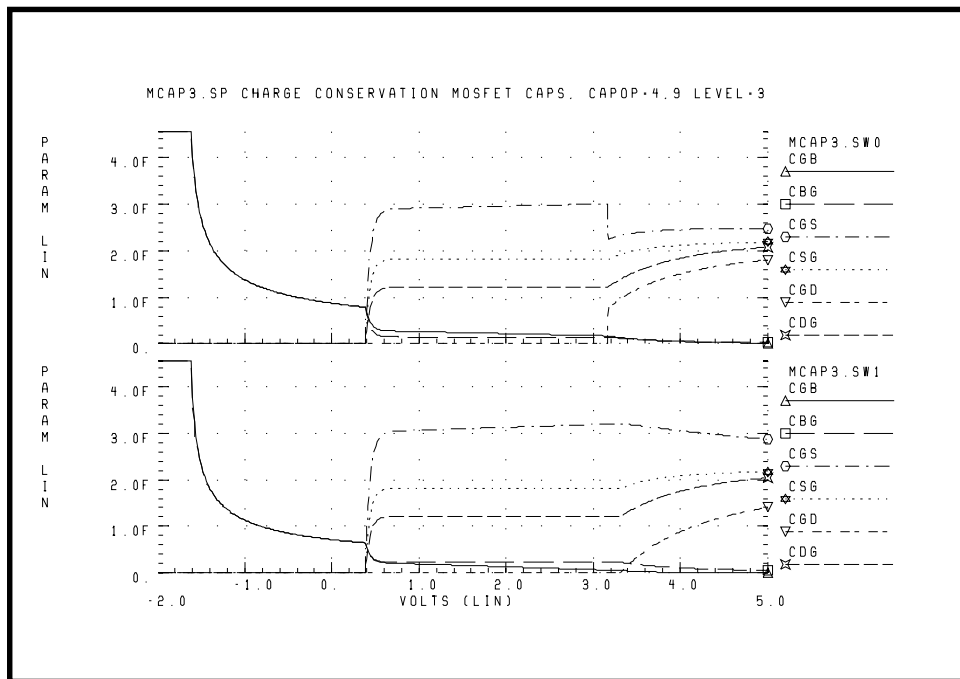
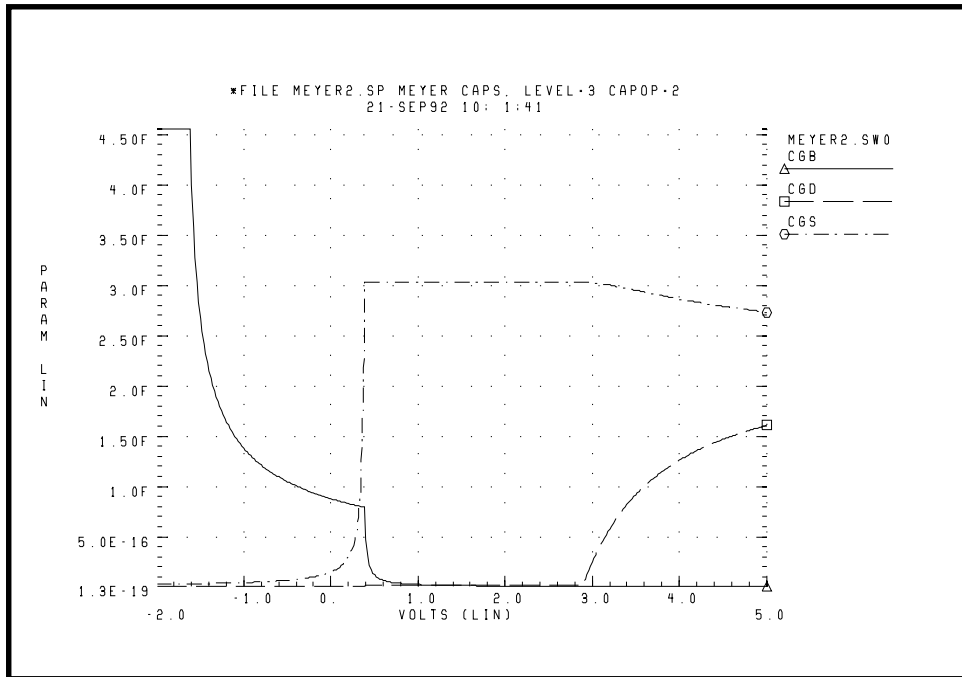**Figure 15-22: CAPOP=4, 9 Capacitances for Level 3 Model**

Figure 15-23: CAPOP=2 Capacitances for Level 3 Model

The following example tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chaterjee 'An Investigation of the Charge Conservation Problem) and compares the Meyer model and charge conservation model. As the following graph illustrates, the charge conservation model gives more accurate results.

Example

```
*FILE:CHRGPUMP.SP CHARGE CONSERVATION TEST FOR CHARGE
PUMP CIRCUIT
*TEST CIRCUIT OF A MOSFET CAPACITOR AND A LINEAR
CAPACITOR
.OPTIONS ACCT LIST NOMOD POST
+ RELTOL=1E-3 ABSTOL=1E-6 CHGTOL=1E-14
.PARAM CAPOP=2
```

```
.OP
.TRAN 2NS 470NS SWEEP CAPOP POI 2 2,9
.IC V(S)=1
*
VIN G 0 PULSE 0 5 15NS 5NS 5NS 50NS 100NS
VBB 0 B PULSE 0 5 0NS 5NS 5NS 50NS 100NS
VDD D D- PULSE 0 5 25NS 5NS 5NS 50NS 100NS
*
RC D- S 10K
C2 S 0 10P
M1 D G S B MM W=3.5U L=5.5U
+AD=100P AS=100P PD=50U PS=50U NRD=1 NRS=1
*
.MODEL MM NMOS LEVEL=3 VTO=0.7 KP=50E-6 GAMMA=0.96
+PHI=0.5763 TOX=50E-9 NSUB=1.0E16 LD=0.5E-6
+VMAX=268139 THETA=0.05 ETA=1 KAPPA=0.5 CJ=1E-4
+CJSW=0.05E-9 RSH=20 JS=1E-8 PB=0.7
+CGD=0 CGS=0 IS=0 JS=0
+CAPOP=CAPOP
*
.PRINT TRAN VOUT=V(S) VIN=V(D) VBB=V(B)
+ VDD=V(D,D-)
.END
```
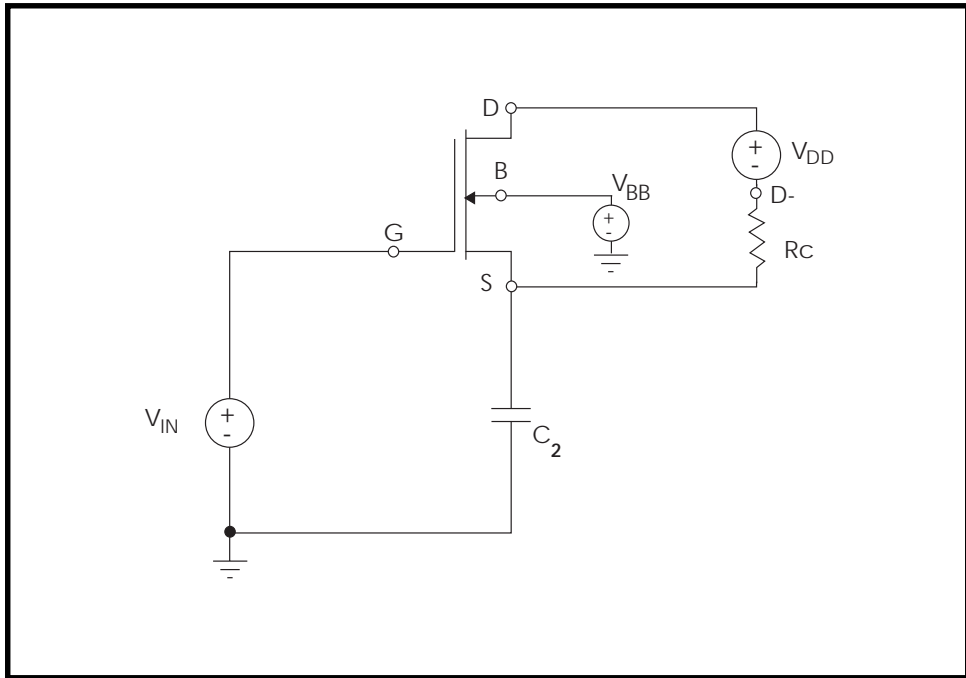
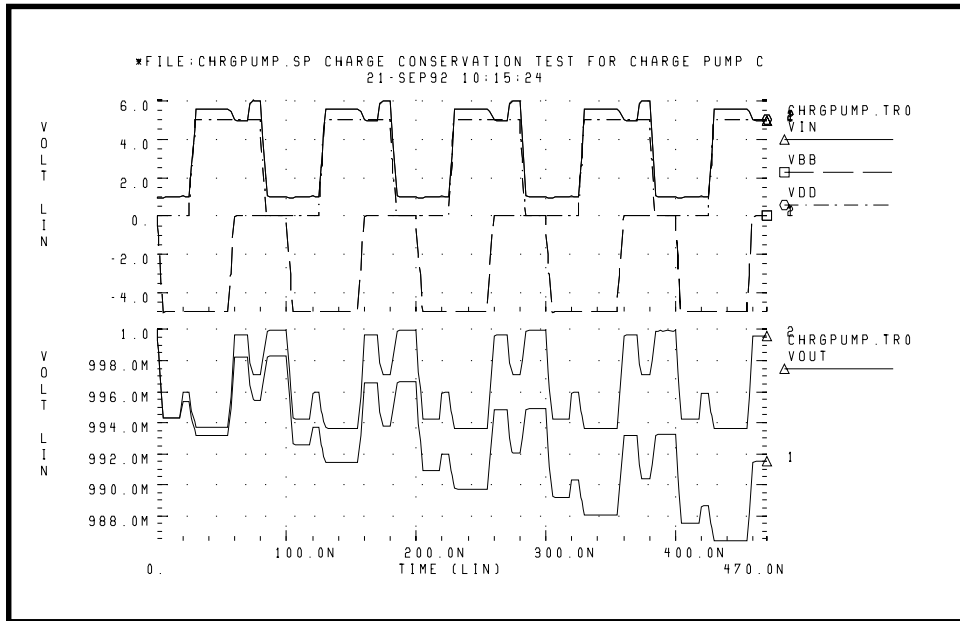**Figure 15-24: Charge Pump Circuit**

Figure 15-25: Charge Conservation Test: CAPOP=2 or 9

The following example applies a pulse through a constant capacitance to the gate of MOS transistor. Ideally, if the model conserves charge, the voltage at node 20 should becomes zero when the input pulse goes to zero. Consequently, the model that provides voltage closer to zero for node 20 conserves charge better. As results indicate, the CAPOP=4 model is better than the CAPOP=2 model.

This example also compares the charge conservation models in SPICE2G.6 and HSPICE. The results indicate that HSPICE is more accurate.

Example

```
FILE MCAP2_A.SP
.OPTIONS SPICE NOMOD DELMAX=.25N
.PARAM CAPOP=4
.TRAN 1NS 40NS SWEEP CAPOP POI  2  4  2
.PRINT TRAN  V(1) V(20)
VIN 1 0 PULSE (0V, 5V, 0NS, 5NS, 5NS, 5NS, 20NS)
```

```
CIN 1 20 1PF
RLEAK 20 0 1E+12
VDD 10 0 1.3
VBB 30 0 -1
M 10 20 0 30 MOS  W=10U L=5U
.MODEL MOS NMOS LEVEL=2 TOX=250E-10 VTO=.3
+ UO=1000 LAMBDA=1E-3 GAMMA=.5 PHI=.5 XQC=.5
+ THETA=0.067 VMAX=1.956E5  XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0
+ CJ=0 JS=0 IS=0
+ CAPOP=CAPOP
.END
```
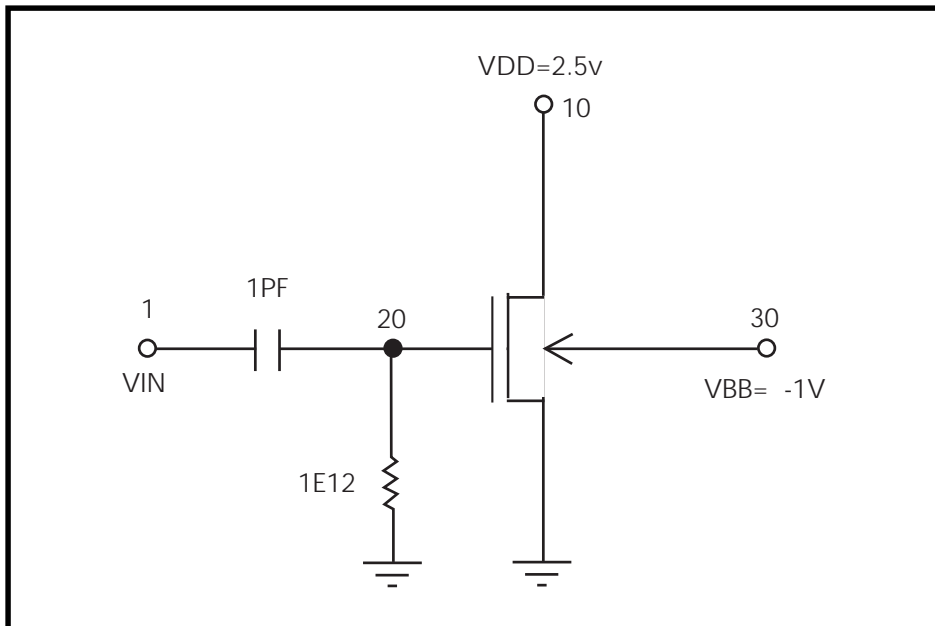

Figure 15-26: Charge Conservation Test Circuit

CAPOP=5 — Gate Capacitance

Use CAPOP=5 for no capacitors, and HSPICE will not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define:

$$vgst = vgs - \frac{(vth + vfb)}{2}$$

$$cox = \frac{\varepsilon ox}{TOX \cdot 1e\text{-}10} \cdot Weff \cdot Leff$$

The gate capacitance *cgs* is calculated according to the equations below in the different regions.

0.5 · (vth + vfb) > vgs

$$cgs = 0$$

0.5 · (vth + vfb) <vgs <vth

For vgst < vds,

$$cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

For vgst > vds,

$$cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$$

vgs > vth

For vgst < vds,

$$cgs = \frac{2}{3} \cdot cox$$

For vgst > vds,

$$cgs = arg \cdot \frac{2}{3} \cdot cox$$

$$arg = vgst \cdot \frac{(3 \cdot vgst - 2 \cdot vds)}{(2 \cdot vgst - vds)^2}$$

The gate capacitance *cgd* is calculated according to the equations below in the different regions.

vgs < vth

$$cgd = 0$$

vgs > vth and vgst < vds

$$cgd = 0$$

vgs > vth and vgst > vds

$$cgd = arg \cdot \frac{2}{3} \cdot cox$$

$$arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

The gate capacitance cgb is combined with the calculation of both oxide capacitance and depletion capacitance as shown below.

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

Oxide capacitance cgbx, is calculated as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance cd is voltage-dependent.

$$cd = \frac{\varepsilon si}{wd} \cdot Weff \cdot Leff$$

$$wd = \left(\frac{2 \cdot \varepsilon si \cdot vc}{q \cdot NSUB} \right)^{1/2}$$

$$vc = \textit{The effective voltage from channel to substrate (bulk)}$$

The following shows the equations for vc under various conditions:

vgs + vsb < vfb

$$vc = 0$$

vgs + vsb > vfb

$$vc = vgs + vsb - vfb$$

vgst > 0, vgs < vth, vgst < vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

vgst > 0, vgs < vth, vgst > vds

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

vgs > vth, vgst < vds

$$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$$

vgs > vth, vgst > vds

$$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$$

CAPOP=13 — BSIM 1-based Charge-Conserving Gate Capacitance Model

See "Level 13 BSIM Model" on page 16-104.

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See "Level 39 BSIM2 Model" on page 16-183.

Effective Length and Width for AC Gate Capacitance Calculations

For some MOS processes and parameter extraction methods, it is helpful to allow different Leff and Weff values for AC analysis than for DC analysis. For AC gate capacitance calculations, model parameters LDAC and WDAC can be substituted for LD and WD in Leff and Weff calculations. LD and WD are still used in Leff and Weff calculations for DC current.

To use LDAC and WDAC, enter XL, LD, LDAC, XW, WD, WDAC in the .MODEL statement. The model uses the following equations for DC current calculations

$$Leff \ = \ L + XL - 2 \cdot LD$$

$$Weff \ = \ W + XW - 2 \cdot WD$$

and uses the following equations for AC gate capacitance calculations

$$Leff \ = \ L + XL - 2 \cdot LDAC$$

$$Weff \ = \ W + XW - 2 \cdot WDAC$$

The noise calculations use the DC Weff and Leff values.

Use LDAC and WDAC with the standard HSPICE parameters XL, LD, XW, and WD. They should not be used with other parameters such as DL0 and DW0.

Using Noise Models

This section describes how to use noise models.

Noise Parameters

Name(Alias)	Units	Default	Description
AF		1.0	flicker noise exponent
KF		0.0	flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V^2F.
NLEV		2.0	noise equation selector
GDSNOI		1.0	channel thermal noise coefficient (use with NLEV=3)

Noise Equations

The HSPICE MOSFET model noise equations have a selector parameter NLEV that is used to select either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

Thermal noise generation in the drain and source resistors is modeled by the two sources inrd and inrs (units amp/$(Hz)^{1/2}$), as shown in Figure 15-4. The values of these sources can be determined by:

$$inrs = \left(\frac{4kt}{rs}\right)^{1/2}$$

$$inrd = \left(\frac{4kt}{rd}\right)^{1/2}$$

Channel thermal noise and flicker noise are modeled by the current source ind and defined by the equation:

$$ind^2 = (channel\ thermal\ noise)^2 + (flicker\ noise)^2$$

If the model parameter NLEV is less than 3, then

$$channel\ thermal\ noise = \left(\frac{8kT \cdot gm}{3}\right)^{1/2}$$

The above formula is used in both saturation and linear regions, which can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If NLEV model parameter is set to 3, HSPICE uses a different equation which is valid in both linear and saturation regions. See *Tsivids, Yanis P., Operation and Modeling of the MOS Transistor, McGraw-Hill, 1987, p. 340*.

For NLEV=3,

$$channel\ thermal\ noise = \left(\frac{8kt}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNOI\right)^{1/2}$$

where

$$a = 1 - \frac{vds}{vdsat} \qquad\qquad Linear\ region$$

$$a = 0 \qquad\qquad\qquad Saturation\ region$$

The two parameters AF and KF are used in the small-signal AC noise analysis to determine the equivalent flicker noise current generator connected between drain and source.

NLEV=0 (SPICE):

$$flicker\ noise = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Leff^2 \cdot f}\right)^{1/2}$$

For NLEV=1 the Leff^2 in the above equation is replaced by Weff $\cdot$ Leff.

NLEV=2, 3:

$$flicker\ noise\ = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}}\right)^{1/2}$$

Noise Summary Printout Definitions

RD, V^2/Hz	output thermal noise due to drain resistor
RS, V^2/Hz	output thermal noise due to source resistor
RX	transfer function of channel thermal or flicker noise to the output. This is not a noise, it is a transfer coefficient, reflecting the contribution of channel thermal or flicker noise to the output.
ID, V^2/Hz	output channel thermal noise: $ID = RX^2 \cdot$ *(channel thermal noise)^2*
FN, V^2/Hz	output flicker noise: $FN = RX^2 \cdot$ *(flicker noise)^2*
TOT, V^2/Hz	total output noise: $TOT = RD + RS + ID + FN$

Using Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The temperature equations used for the calculation of temperature effects on the model parameters are selected by the TLEV and TLEVC parameters.

Temperature Effects Parameters

Name(Alias)	Units	Default	Description
BEX		-1.5	low field mobility, UO, temperature exponent
CTA	1/°K	0.0	junction capacitance CJ temperature coefficient. Set TLEVC to 1 to enable CTA to override default HSPICE temperature compensation.
CTP	1/°K	0.0	junction sidewall capacitance CJSW temperature coefficient. Set TLEVC to 1 to enable CTP to override default HSPICE temperature compensation.
EG	eV		energy gap for pn junction diode. Set default=1.11, for TLEV=0 or 1 and default=1.16, for TLEV=2. 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide
F1EX		0	bulk junction bottom grading coefficient

Name(Alias)	Units	Default	Description
GAP1	eV/°K	7.02e-4	first bandgap correction factor (from Sze, alpha term) 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide
GAP2	°K	1108	second bandgap correction factor (from Sze, beta term) 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide
LAMEX	1/°K	0	LAMBDA temperature coefficient
N		1.0	emission coefficient
MJ		0.5	bulk junction bottom grading coefficient
MJSW		0.33	bulk junction sidewall grading coefficient
PTA	V/°K	0.0	junction potential PB temperature coefficient. Set TLEVC to 1 or 2 to enable PTA to override default HSPICE temperature compensation.
PTC	V/°K	0.0	Fermi potential PHI temperature coefficient. Set TLEVC to 1 or 2 to enable PTC to override default HSPICE temperature compensation.
PTP	V/°K	0.0	junction potential PHP temperature coefficient. Set TLEVC to 1 or 2 to enable PTP to override default HSPICE temperature compensation.
TCV	V/°K	0.0	threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel.

Name(Alias)	Units	Default	Description
TLEV		0.0	temperature equation level selector. Set TLEV=1 for ASPEC style – default is SPICE style.
			When option ASPEC is invoked, the program sets TLEV for ASPEC.
TLEVC		0.0	temperature equation level selector for junction capacitances and potentials, interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style.
			When option ASPEC is invoked, the program sets TLEVC for ASPEC.
TRD	1/°K	0.0	temperature coefficient for drain resistor
TRS	1/°K	0.0	temperature coefficient for source resistor
XTI		0.0	saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode.

MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) have length and width sensitivity parameters associated with them as shown in the following table. These parameters are used in conjunction with the Automatic Model Selector capability and enable more accurate modelling for various device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Table 15-7:

Parameter	Description	Sensitivity Parameters		
		Length	Width	Product
BEX	low field mobility, UO, temperature exponent	LBEX	WBEX	PBEX
FEX	velocity saturation temperature exponent	LFEX	WFEX	PFEX
TCV	threshold voltage temperature coefficient	LTCV	WTCV	PTCV
TRS	temperature coefficient for source resistor	LTRS	WTRS	PTRS
TRD	temperature coefficient for drain resistor	LTRD	WTRD	PTRD

Temperature Equations

This section describes how to use temperature equations.

Energy Gap Temperature Equations

To determine energy gap for temperature compensation use the following equations.

TLEV = 0 or 1:

$$egnom = 1.16 - 7.02e{-}4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e{-}4 \cdot \frac{t^2}{t + 1108.0}$$

TLEV = 2:

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

$$isbd(t) = isbd(tnom) \cdot e^{facln/N}$$

$$isbs(t) = isbs(tnom) \cdot e^{facln/N}$$

where

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

These isbd and isbs are defined in "Using a MOSFET Diode Model" on page 15-29.

MOS Diode Capacitance Temperature Equations

TLEVC selects the temperature equation level for MOS diode capacitance.

TLEVC=0:

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1 \right) \right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1 \right) \right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1 \right) \right]$$

TLEVC=1:

$$PB(t) = PB - PTA \cdot \Delta t$$

$$PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t)$$

$$CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t)$$

$$CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

TLEVC=2:

$$PB(t) = PB - PTA \cdot \Delta t$$

$$PHP(t) = PHP - PTP \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}$$

$$CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)} \right)^{MJ}$$

$$CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)} \right)^{MJSW}$$

TLEVC=3:

$$PB(t) = PB + dpbdt \cdot \Delta t$$

$$PHP(t) = PHP + dphpdt \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB} \right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB} \right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot dpbdt \cdot \frac{\Delta t}{PB} \right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot dphpdt \cdot \frac{\Delta t}{PHP} \right)$$

where for TLEV=0 or 1:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108} \right) - PB \right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108} \right) - PHP \right]}{tnom}$$

and TLEV=2:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \dfrac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \dfrac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Surface Potential Temperature Equations

TLEVC=0:

$$PHI(t) = PHI \cdot \left(\frac{t}{tnom}\right) - vt(t) \cdot \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

TLEVC=1:

$$PHI(t) = PHI - PTC \cdot \Delta t$$

If the PHI parameter is not specified, it is calculated as follows:

$$PHI(t) = 2 \cdot vt(t) \cdot \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, ni, must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \left(\frac{t}{tnom}\right)^{3/2} \cdot \exp\left[EG \cdot \left(\frac{t}{tnom} - 1\right) \cdot \left(\frac{1}{2 \cdot vt(t)}\right)\right]$$

TLEVC=2:

$$PHI(t) = PHI - PTC \cdot \Delta t$$

TLEVC=3:

$$PHI(t) = PHI + dphidt \cdot \Delta t$$

where for TLEV=0 or 1:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHI\right]}{tnom}$$

and for TLEV=2:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHI\right]}{tnom}$$

Threshold Voltage Temperature Equations

The threshold temperature equations are:

TLEV=0:

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=1:

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

TLEV=2:

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot (PHI(t))^{1/2}$$

Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Channel Length Modulation Temperature Equation

The LAMBDA is modified with temperature if model parameter LAMEX is specified.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t)$$

Diode Resistance Temperature Equations

Effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t)$$

$$RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$