http://eecs.oregonstate.edu/~moon/ece423

Prof. Un-Ku Moon
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Office hours: Zoom URL on Canvas and sent via the mailing list

Books
Analysis and Design of Analog Integrated Circuits, Gray/Hurst/Lewis/Meyer
Analog Integrated Circuit Design, Carusone/Johns/Martin
Design of analog CMOS integrated circuits, Razavi

Content
This class is a continuation of ECE 422/522 and a prerequisite to ECE 520. This course is geared towards learning commonly practiced CMOS IC design and analysis. We will do some IC layout work to expose you to tools commonly used today (this portion will be taught by the TA). At the end of the course, you will have learned a circuit designer’s approach (less mathematical and more intuition driven) to transistor-level design. The final class project will be a design of fully differential opamp, which will involve schematic capture, transistor-level simulation, IC layout, layout versus schematic (LVS) verification, layout design rule check (DRC)...

HW
The homework assignments are essentially the same each year. The homework is intended for your learning/benefit. They will be handed back with a “√” (3 pts) for good work or “√ –” (2 pts) for lacking work. The “best” among the submitted homework will be scanned and posted on the class web page as “solutions.”

Exams
The in-person exams are closed book/notes. I provide a reference sheet along with the exam. This reference sheet is already made available on the class web page, so you should get used to the content well ahead of time.

Grading
The course grading will be weighted as follows.

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight</th>
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<tbody>
<tr>
<td>Homework (seven of them)</td>
<td>25%</td>
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<tr>
<td>Midterm</td>
<td>25%</td>
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<tr>
<td>Final</td>
<td>25%</td>
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<tr>
<td>Circuit design project</td>
<td>25%</td>
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Midterm: (Wednesday Feb-9 2-3:20pm)
Final: (Tuesday Mar-15 2-3:20pm)
Circuit design project: (Due Friday Mar-11 midnight)
## Dates

<table>
<thead>
<tr>
<th>Dates</th>
<th>Activities</th>
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<tbody>
<tr>
<td>Jan. 3, 5</td>
<td>Basic opamp design review</td>
</tr>
<tr>
<td>Jan. 10, 12</td>
<td>Biasing variations</td>
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<td></td>
<td>Poles/settling</td>
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<td></td>
<td>HW1 due</td>
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<tr>
<td>Jan. 17, 19</td>
<td>HW2 due</td>
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<td></td>
<td>Folded cascode opamp</td>
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<td>MLK Jr. Holiday</td>
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<td>Jan. 24, 26</td>
<td>Opamp variations</td>
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<td>HW3 due</td>
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<td>Jan. 31, Feb. 2</td>
<td>IC layout (TA)</td>
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<td>IC layout (TA)</td>
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<td>HW4 due</td>
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<td>Feb. 7, 9</td>
<td>Stability/loopgain</td>
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<td>MIDTERM</td>
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<td>HW5 due</td>
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<td>Feb. 14, 16</td>
<td>Common-mode feedback</td>
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<td>Differential stability/loopgain</td>
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<td>HW6 due</td>
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<td>Feb. 21, 23</td>
<td>ISSCC</td>
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<td>HW7 due</td>
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<td>ISSCC</td>
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<tr>
<td>Feb. 28, Mar. 2</td>
<td>Noise/distortion</td>
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<tr>
<td>Mar. 7, 9</td>
<td>Project/discussion/help (TA)</td>
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**PROJECT due at midnight on Friday Mar-11**  
**FINAL EXAM at 2-3:20pm on Tuesday 3/15**