ECE 423/523 **CMOS Integrated Circuits–II** **Winter 2025**

http://eecs.oregonstate.edu/~moon/ece423

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	Mon	Tue	Wed	Thu	Fri
10:00	ECE 323 class		ECE 323 class		ECE 323 class
11:00	Moon KEC 4093		Moon KEC 4093		
12:30					
1:30		Evan (323)		Evan (323)	Evan (323)
2:00	ECE 4/523 class		ECE 4/523 class		
2:30		Amartya		Amartya	Amartya
3:30	Moon KEC 4093	Runpeng (323)	Moon KEC 4093	Runpeng (323)	Runpeng (323)
4:30		Ashwanth (323)		Ashwanth (323)	Ashwanth (323)
5:30		Ahmed		Ahmed	Ahmed
6:30					

TA office hours are held in the KEC atrium (4/523: sometimes in the computer lab)

Books Analysis and Design of Analog Integrated Circuits, Gray/Hurst/Lewis/Meyer
Analog Integrated Circuit Design, Carusone/Johns/Martin
Design of analog CMOS integrated circuits, Razavi

I do not follow any textbook outline for this course, but these are excellent and helpful books.

Content This class is a continuation of ECE 422/522 and a prerequisite to ECE 520. This course is geared towards learning commonly practiced CMOS IC design and analysis. We will do some IC layout work to expose you to tools commonly used today (this portion will be taught by the TA). At the end of the course, you will have learned a circuit designer's approach (less mathematical and more intuition driven) to transistor-level design. The final class project will be a design of fully differential opamp, which will involve schematic capture, transistor-level simulation, IC layout, layout versus schematic (LVS) verification, layout design rule check (DRC)...

HW The homework assignments are essentially the same each year. The homework is intended for *your* learning/benefit. They will be handed back with a "✓" (3 pts) for good work or "✓–" (2 pts) for lacking work. The "best" among the submitted homework will be scanned and posted on the class web page as "solutions."

Exams The in-person exams are **closed** book/notes/etc. I provide a reference sheet along with the exam. This reference sheet is already made available on the class web page, so you should get used to the content well ahead of time.

Grading The course grading will be weighted as follows.

Homework (seven of them)	25%
Midterm	25% (**Wednesday Feb-12** 2-3:20pm)
Final	25% (**Wednesday Mar-19** 12-1:20pm)
Circuit design project	25% (**Due Friday Mar-14** midnight)