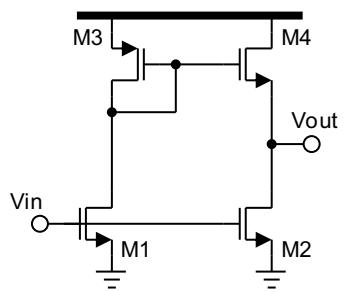


Find the output-referred noise and the input-referred noise.

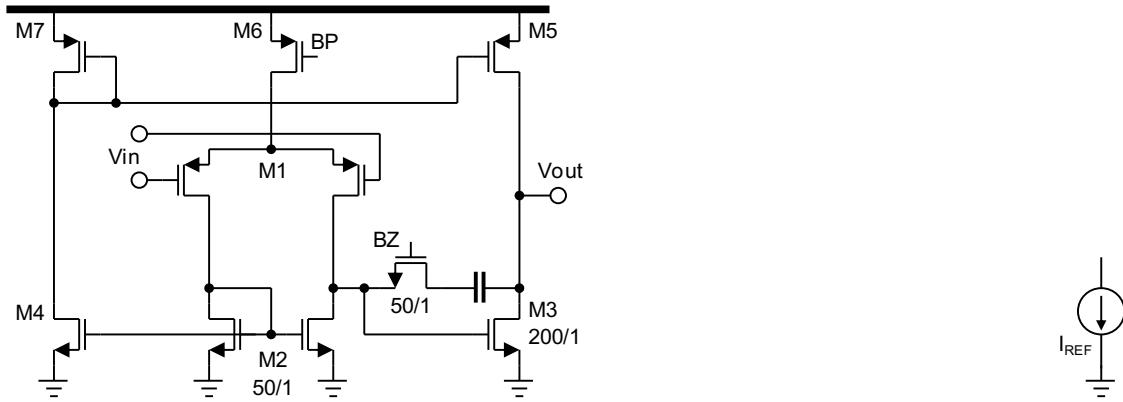


In the amplifier shown below...

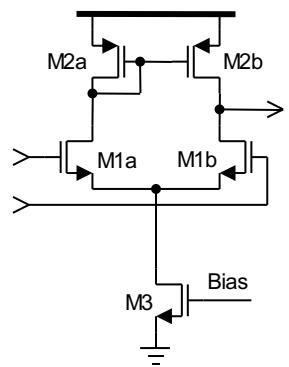
Design the bias BP and specify transistor sizing for zero systematic offset.

Design the bias BZ for right-half-plane zero cancellation.

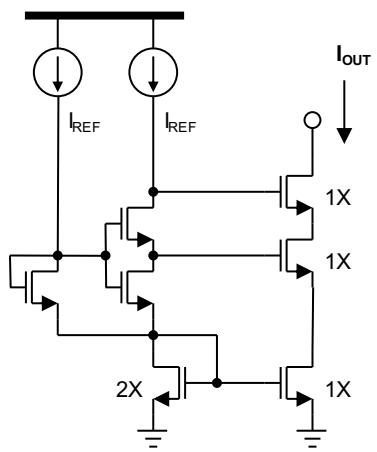
Find the input to output small-signal gain expression.



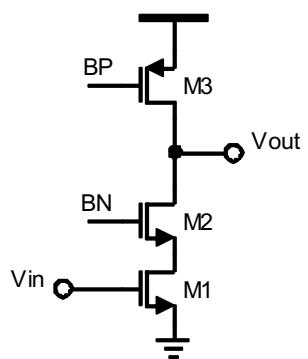
In the circuit shown below, find the output-referred noise. Assume that the circuit is balanced (i.e. $M1a=M1b$, $M2a=M2b$).



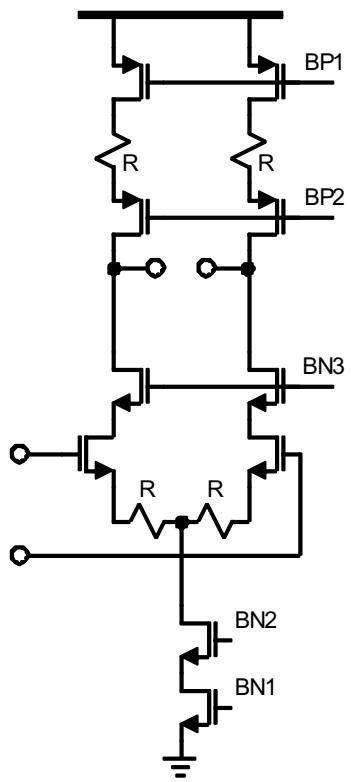
In the current source shown below, appropriately specify the three transistor sizes for optimum biasing.



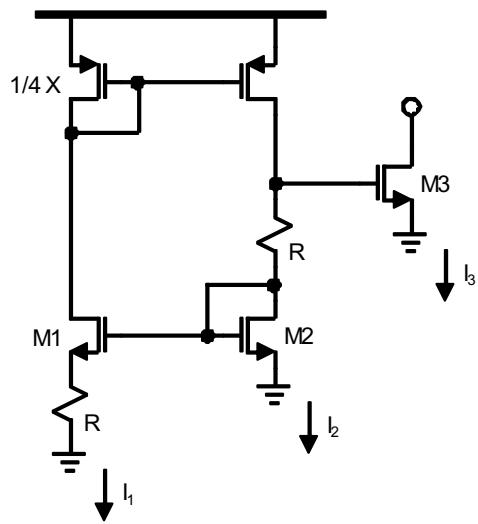
For the amplifier shown below, find the input-referred noise (expression).



Design optimum bias and CMFB circuits for the amplifier shown below. Use one ideal current source to ground and one ideal CM voltage reference. Specify device sizes as needed – 1X device size is assumed unless specified. Then find the input to output small-signal gain (expression) and CMFB loopgain (expression).



In the bias circuit shown below, find the resulting current ratio I_1 to I_2 and I_2 to I_3 . Also find the resulting gm_1 , gm_2 , and gm_3 of transistors M1/M2/M3 (expression).



Design optimum bias and CMFB circuits for the amplifier shown below. Find the small signal input to output gain (expression) and CMFB loopgain (expression). Specify device sizes as needed. A “1X” device size will be assumed if a device size is not specified.

