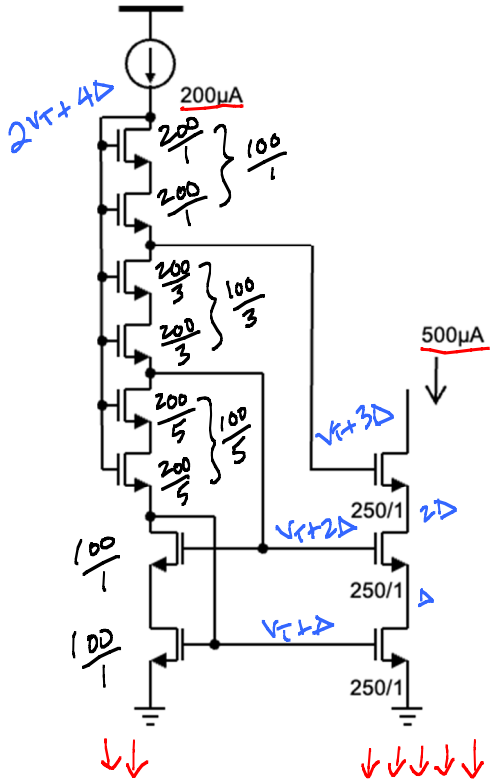
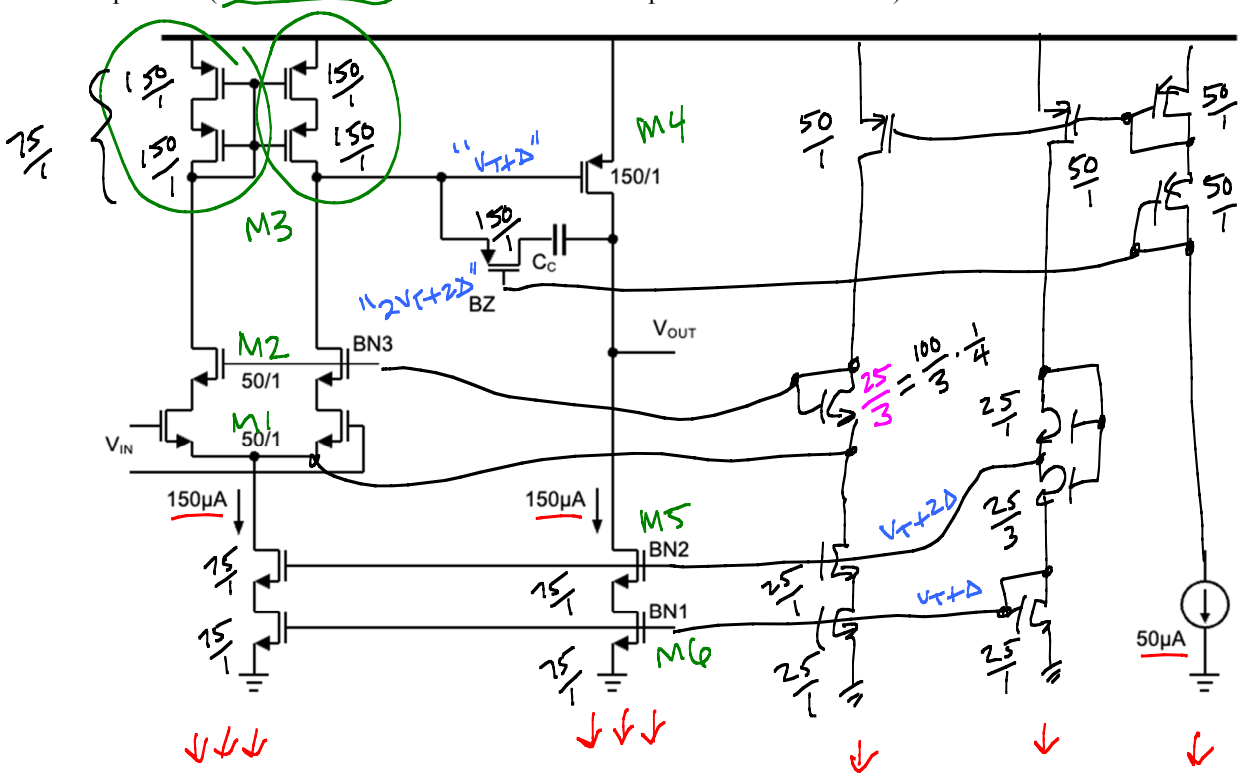
1. [10 pts total] Optimally bias the current source by specifying all transistor sizes where W/L is not given.

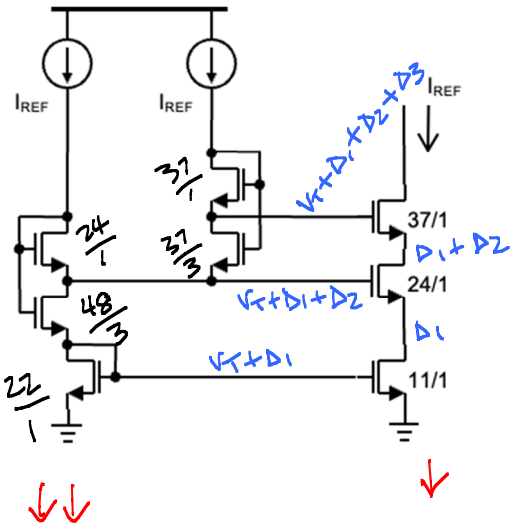


2. [10 pts total] Design the optimum bias for BN1, BN2, BN3, BZ (for no/minimal systematic offset and RHP zero cancellation). Specify all transistor sizes where W/L is not given. Find the small-signal gain expression (label transistors as needed and treat composite as one transistor).

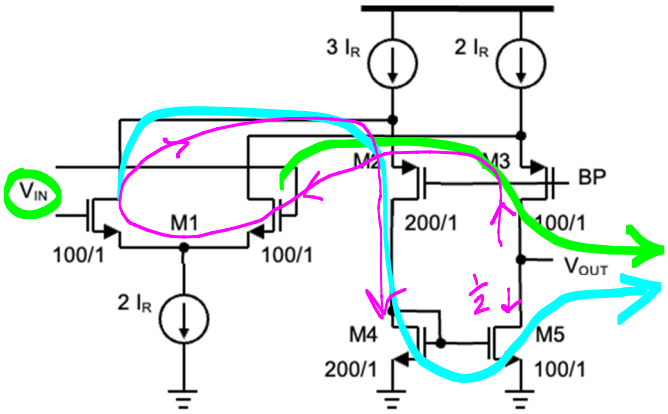


gain ≅ $g_{m1}(r_{02} g_{m2} r_{01} \| r_{03})\, g_{m4}(r_{04} \| r_{05} g_{m5} r_{06})$

3. [10 pts total] Optimally bias the current source by specifying all transistor sizes where W/L is not given.



4. [10 pts total] Find the Norton-equivalent small-signal Gm and Rout.



$$G_m \cong \frac{1}{2} g_{m1} + \frac{1}{2} g_{m1} \cdot \frac{1}{2} = \frac{3}{4} g_{m1}$$

$$R_{out} \cong r_{o5} \parallel \frac{r_{o3} g_{m3} (2 r_{o1})}{1 + \frac{1}{2}}$$