ECE 423/523 – CMOS Integrated Circuits II

Problem Set #1

Design a differential input singled-ended output operational amplifier meeting the following specifications. Simulations are to be done using ad=as=W·0.5μm and pd=ps=2·W+1μm using 0.18μm CMOS BSIM3 typical models. Use the models made available on the class webpage http://web.engr.oregonstate.edu/~moon/ece423. LTSPICE is a free tool that can be downloaded to your laptop. We also have HSPICE on our system.

If you have some other working Cadence setup for 0.18μm CMOS (e.g. ECE 4/522 setup), you may use that instead. Use any setup at your own risk, but ECE 4/522 setup may be the path of least resistance, since you just used it for your final project in ECE 4/522. That setup would automatically take care of those parameters (ad, as, pd, ps). While I would allow anything you want to do, I am *not* encouraging you to use the new ECE 4/523 setup, as you are not yet proficient with that setup.

If you do not meet the specifications fully, comment why you could not meet them. You may use one ideal current source tied to ground for biasing. You may use any ideal input common-mode voltage for test bench.

Specifications

Power supply	V_{DD} = 1.8V
Load	C_{load} = 4pF
DC gain	> 60 dB
Unity-gain BW	> 160 MHz
Phase Margin	> 60 º
Output swing	> 1 Vpp
Power consumption	< 10 mW