Some comments (in lecture mode here): This design operates with relative large “delta” (smaller W/L ratio for a given current), leading to barely yielding 1Vpp swing despite the 1.8V supply. It does result in very low power consumption. The other thing is the use of nulling resistor. Normally that is meant to cancel RHP zero, but in this case it’s cancelling the second pole, which would have caused bandwidth/ phase margin problem. You won’t have this option in real applications (with process/temperature/supply variation), rather, you can’t really use it to this extreme in real applications. As you know, nulling resistor is all together not allow for the final project.

Design Results and Measurements

Table 1.
Table of project requirements and design performance specifications

	Requirements	Design Outputs
DC Gain	>60dB	60.808dB
Power Supply	VDD = 1.8V	VDD = 1.8V
Load Capacitance	4pF	4pF
Phase Margin	>60º	60.7º
Unity Gain Frequency	>160MHz	194.986 MHz
Output Swing	>1Vpp	1.068V
Power Consumption	<10mW	569.564µW

Table 2.
Table of TSMC 0.18um MOSFET sizing and drain-to-source currents based on Figure 1

Device	Width (μm)	Length (nm)
M0	16	240
M1	16	240
M2	16	240
M3	10	240
M4	10	240
M5	5	240
M6	5	240
M7	10	240

** You should start getting into the habit of placing W/L in the schematic right next to each transistor. That is required for final project (read project tips at the end)

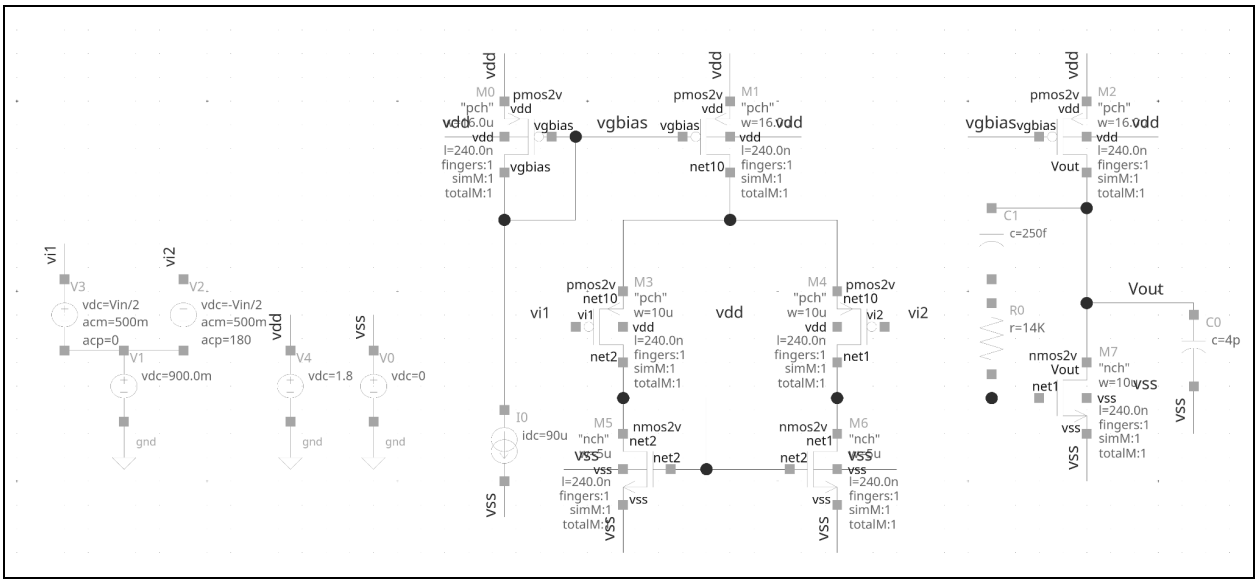

Figure 1. Sizing and biasing of all devices for differential amplifier

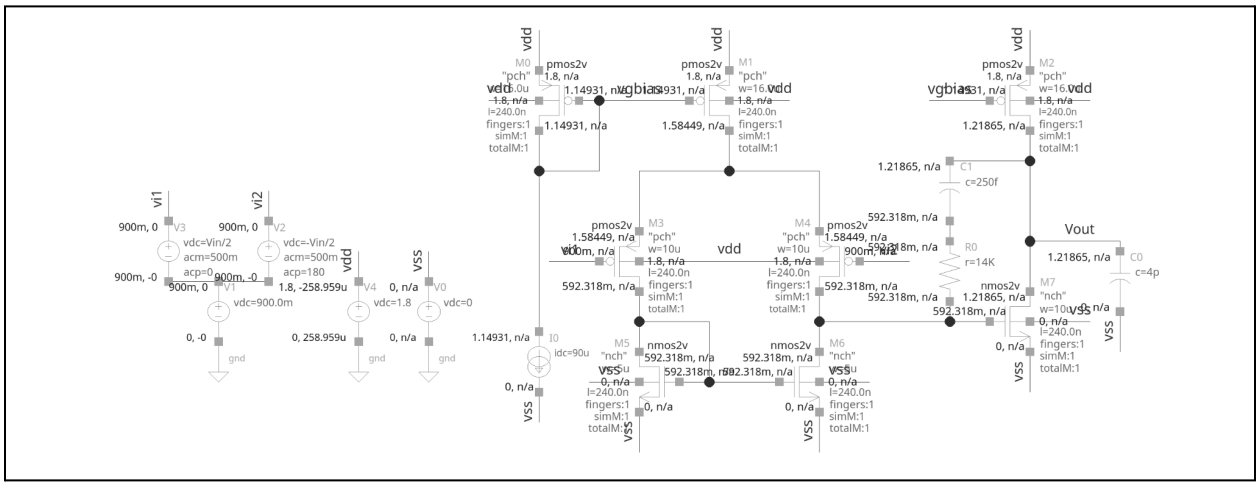

Figure 2. DC voltages and currents at all nodes on schematic

** Placing W/L in the schematic right next to each transistor would help the grader clearly see what you did. As you can see it's hard to read (figure out) W/L from the default schematic, because the schematic is intended to provide all the information you might want, not how to help easily read W/L ratios.

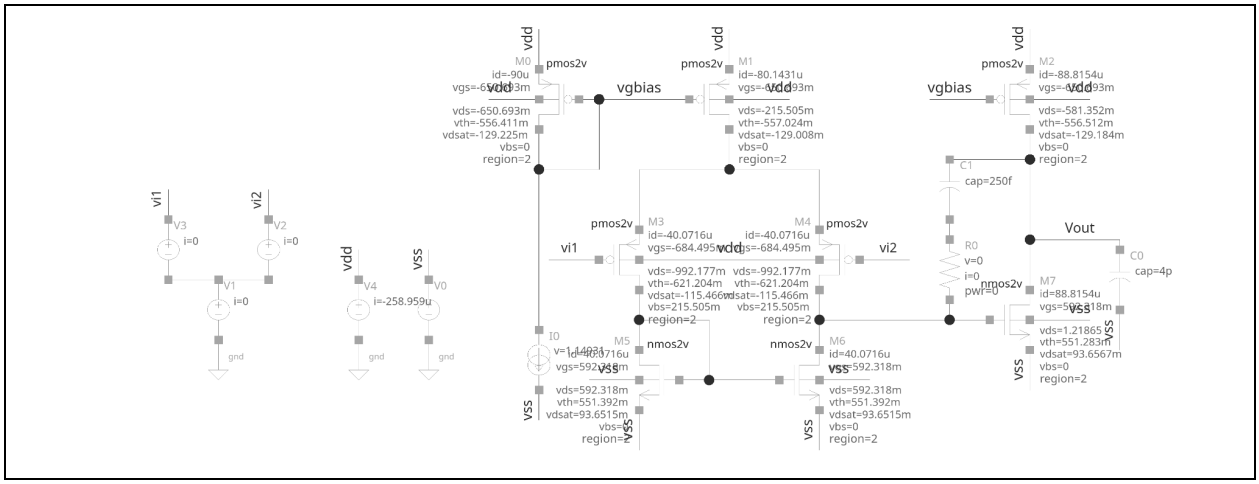

Figure 3. Operating points and regions

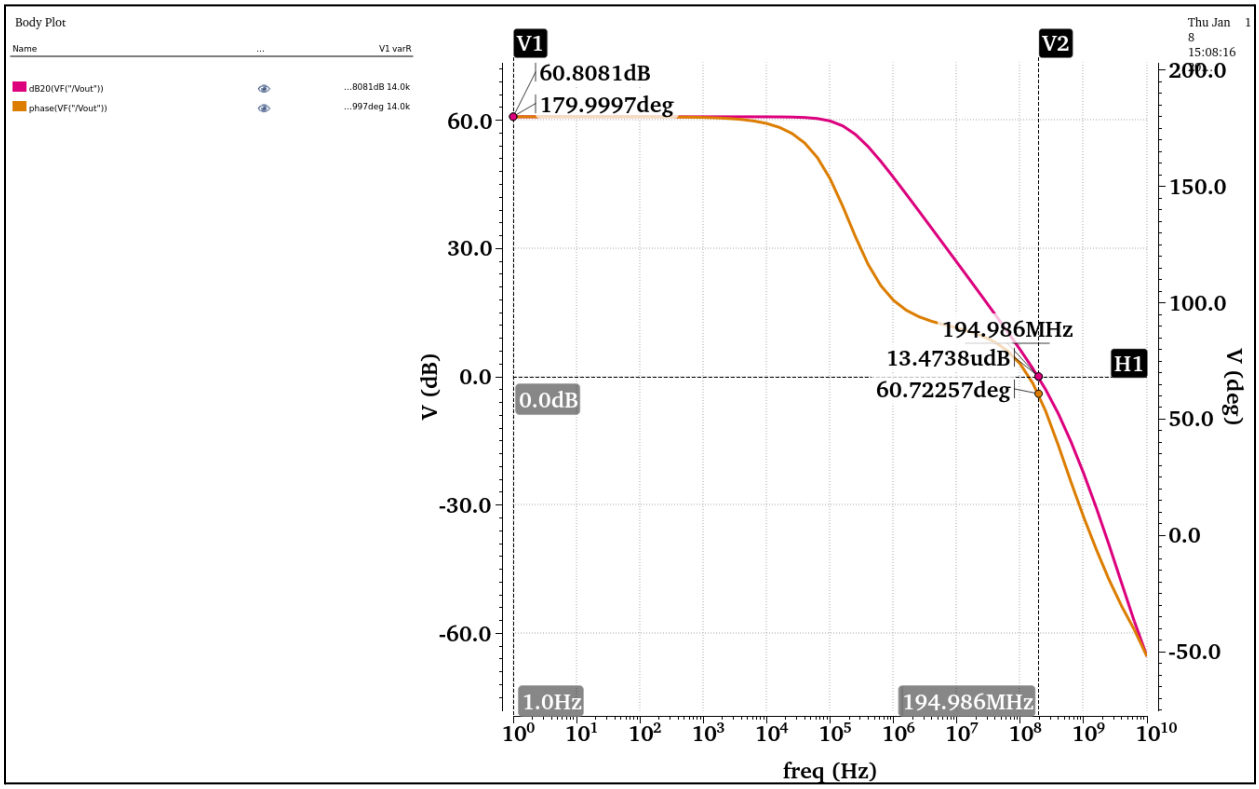

Figure 4. Body plot of differential amplifier showing phase margin and gain

To measure the output swing, I did a sweep of the differential input voltage and measured the output voltage as well as taking the derivative of the gain. I plotted the two against each other and measured -3dB points to get the output swing minimum and maximum voltages. I then took the difference between the two points

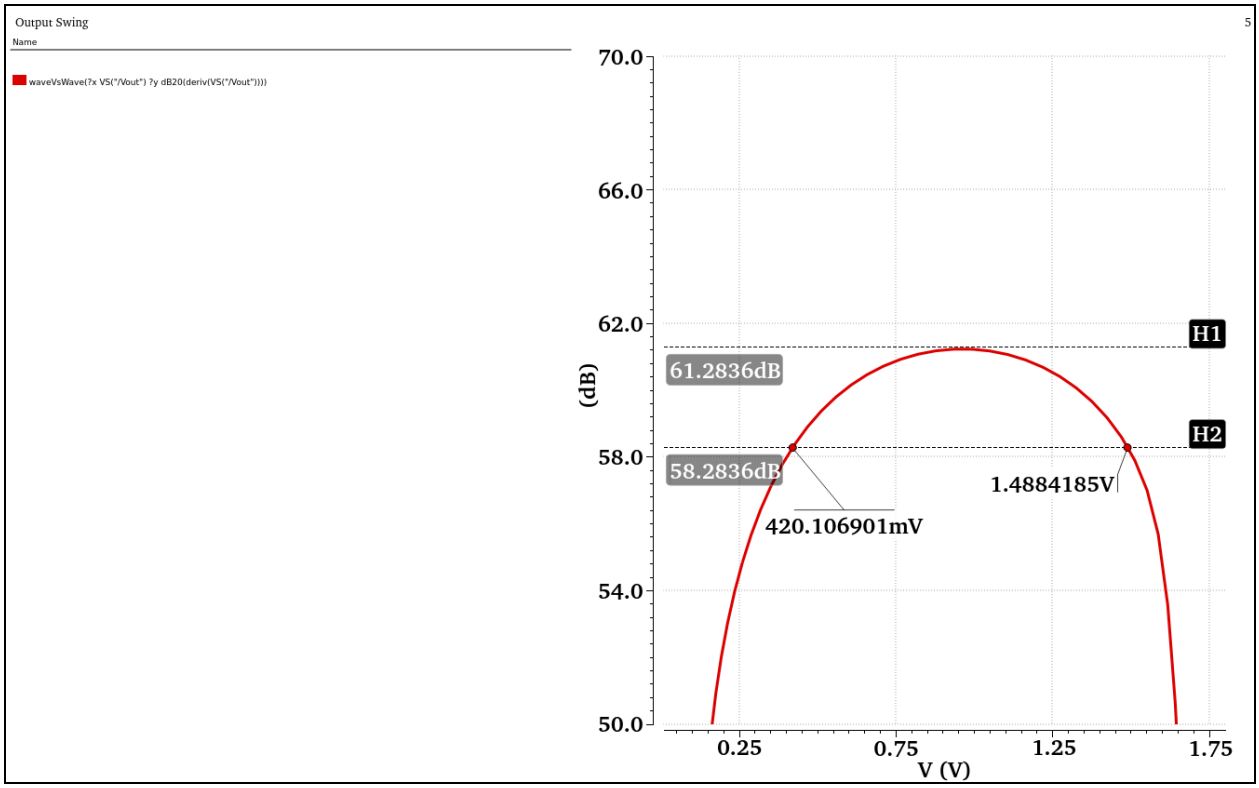

Figure 5. Output swing measurement using derivative of DC differential gain

Design Implementation

To build a two-stage operation amplifier with a single- ended output, a five-transistor amplifier was used for the first stage. The design was similar to Figure 1, except with a PMOS current source, PMOS input mosfets, and NMOS current mirror. For the second stage, a common source with an active PMOS load was used for a wider voltage swing.

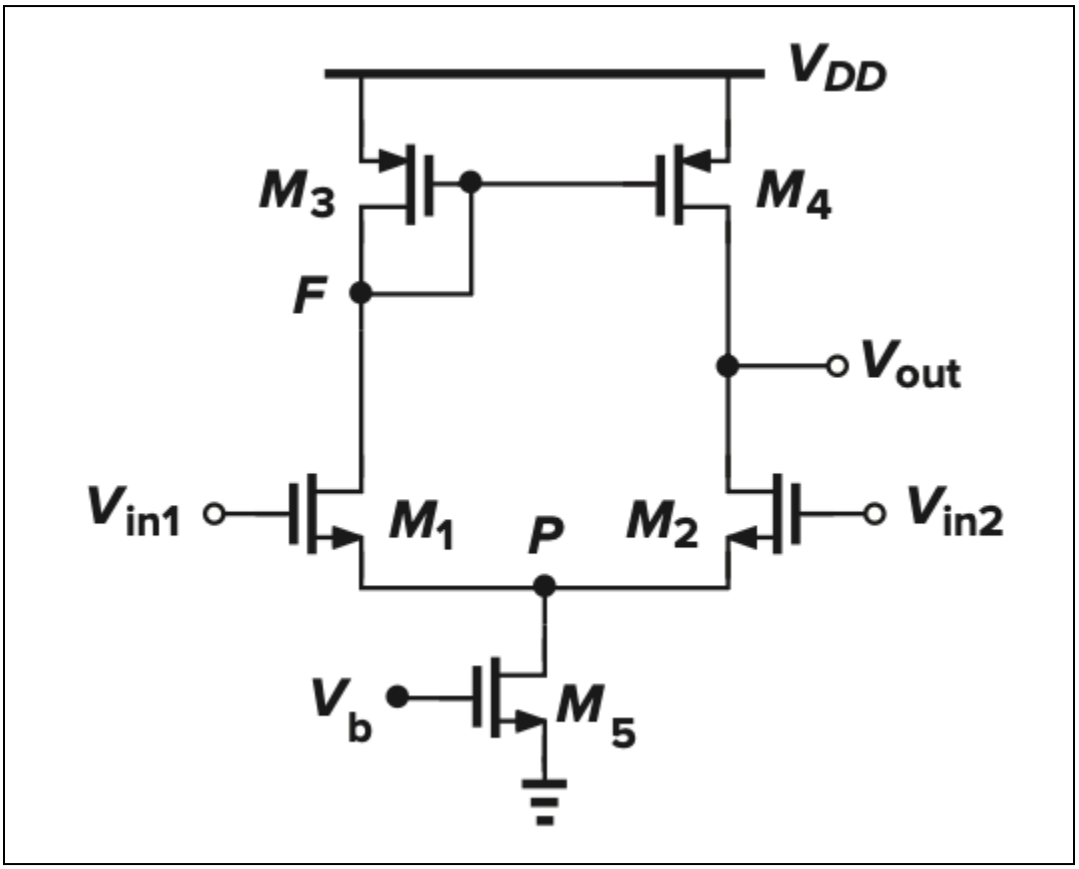

Figure 1. Differential pair with active current mirror (Razavi 2nd Ed. Figure 5.27, p. 149)

My approach to sizing all mosfets began with the lengths of the mosfets. By doubling the length of all mosfets, the resistance of all devices increased which is necessary for large small-signal gain. To avoid unprecedented behavior and operation regions, all mosfets had their widths doubled. The general widths followed a doubling pattern from bottom to top. The bottom NMOS current mirror would be the smallest width. Then the PMOS mosfets at the input and the common source NMOS would be double the width. The three PMOS current sources at the top would be four times the width and must all be the same width to have the same currents since they all have the same bias voltage. Through parameter sweeps, the widths of the input mosfets, current mirror, and common source input were found to have the greatest gain at 5um and 10um with the current source being used. Then the current sources, the top PMOSs, were swept to find

what width led to the greatest gain to find that they could be 16um, and not four times the width of the current mirror in the five transistor stage opamp. A current source sweep was done last to check for greatest gain while keeping all mosfets, especially the PMOS current sources on top in saturation. For the Miller compensation capacitor, a suggested 30-40% of the load capacitance was used as a starting point and decreased until unity gain frequency was maximized while still using integer values for capacitance. A nulling resistor was added last and swept to meet the project requirements of a greater than 60º phase margin at unity gain.

Netlist (for proof or verification):

```
// Point Netlist Generated on: Jan 10 16:06:50 2026
// Generated for: spectre
// Design Netlist Generated on: Jan 10 16:06:49 2026
// Design library name: homework1
// Design cell name: diffopamp
// Design view name: schematic
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global 0
parameters Vin=0
include
"/nfs/guille/moon/users/moon/public_html/ece423/pdk/tsmc018/tsmc18/../models/spectre/cmn01
8_assp_v1d3.scs" section=tt_dio_m
include
"/nfs/guille/moon/users/moon/public_html/ece423/pdk/tsmc018/tsmc18/../models/spectre/cmn01
8_assp_v1d3.scs" section=tt_dio_3m
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8_assp_v1d3.scs" section=tt_rtmom
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"/nfs/guille/moon/users/moon/public_html/ece423/pdk/tsmc018/tsmc18/../models/spectre/cmn01
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include
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// Library name: homework1
// Cell name: diffopamp
// View name: schematic
I0 (vgbias vss) isource dc=90u type=dc
V4 (vdd 0) vsource dc=1.8 type=dc
V3 (vi1 net6) vsource dc=Vin/2 mag=500m phase=0 type=dc
```

```
V2 (vi2 net6) vsource dc=-Vin/2 mag=500m phase=180 type=dc
V1 (net6 0) vsource dc=900.0m type=dc
V0 (vss 0) vsource dc=0 type=dc
M4 (net1 vi2 net10 vdd) pch l=240.0n w=10u m=1 nf=1 sd=540.0n ad=4.8e-12 \
      as=4.8e-12 pd=20.96u ps=20.96u nrd=0.027 nrs=0.027 sa=480.0n \
      sb=480.0n sca=0 scb=0 scc=0
M3 (net2 vi1 net10 vdd) pch l=240.0n w=10u m=1 nf=1 sd=540.0n ad=4.8e-12 \
      as=4.8e-12 pd=20.96u ps=20.96u nrd=0.027 nrs=0.027 sa=480.0n \
      sb=480.0n sca=0 scb=0 scc=0
M2 (Vout vgbias vdd vdd) pch l=240.0n w=16.0u m=1 nf=1 sd=540.0n \
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      nrs=0.016875 sa=480.0n sb=480.0n sca=0 scb=0 scc=0
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      ad=7.68e-12 as=7.68e-12 pd=32.96u ps=32.96u nrd=0.016875 \
      nrs=0.016875 sa=480.0n sb=480.0n sca=0 scb=0 scc=0
M0 (vgbias vgbias vdd vdd) pch l=240.0n w=16.0u m=1 nf=1 sd=540.0n \
      ad=7.68e-12 as=7.68e-12 pd=32.96u ps=32.96u nrd=0.016875 \
      nrs=0.016875 sa=480.0n sb=480.0n sca=0 scb=0 scc=0
M7 (Vout net1 vss vss) nch l=240.0n w=10u m=1 nf=1 sd=540.0n ad=4.8e-12 \
      as=4.8e-12 pd=20.96u ps=20.96u nrd=0.027 nrs=0.027 sa=480.0n \
      sb=480.0n sca=0 scb=0 scc=0
M6 (net1 net2 vss vss) nch l=240.0n w=5u m=1 nf=1 sd=540.0n ad=2.4e-12 \
      as=2.4e-12 pd=10.96u ps=10.96u nrd=0.054 nrs=0.054 sa=480.0n \
      sb=480.0n sca=0 scb=0 scc=0
M5 (net2 net2 vss vss) nch l=240.0n w=5u m=1 nf=1 sd=540.0n ad=2.4e-12 \
      as=2.4e-12 pd=10.96u ps=10.96u nrd=0.054 nrs=0.054 sa=480.0n \
      sb=480.0n sca=0 scb=0 scc=0
C1 (Vout net3) capacitor c=250f
C0 (Vout vss) capacitor c=4p
R0 (net3 net1) resistor r=14K
simulatorOptions options psfversion="1.4.0" temp=27 tnom=27 scalem=1.0 \
   scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 digits=5 cols=80 \
   pivrel=1e-3 sensfile="../psf/sens.output" checklimitdest=sqldb
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dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
dc dc param=Vin start=-0.05 stop=0.05 lin=2000 oppoint=rawfile \
   maxiters=150 maxsteps=10000 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
```

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outputParameter info what=output where=rawfile
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primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
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