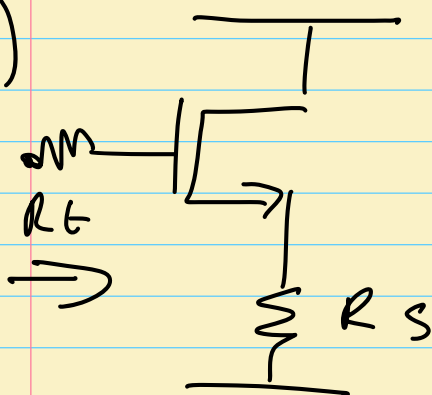


## HW 2 .

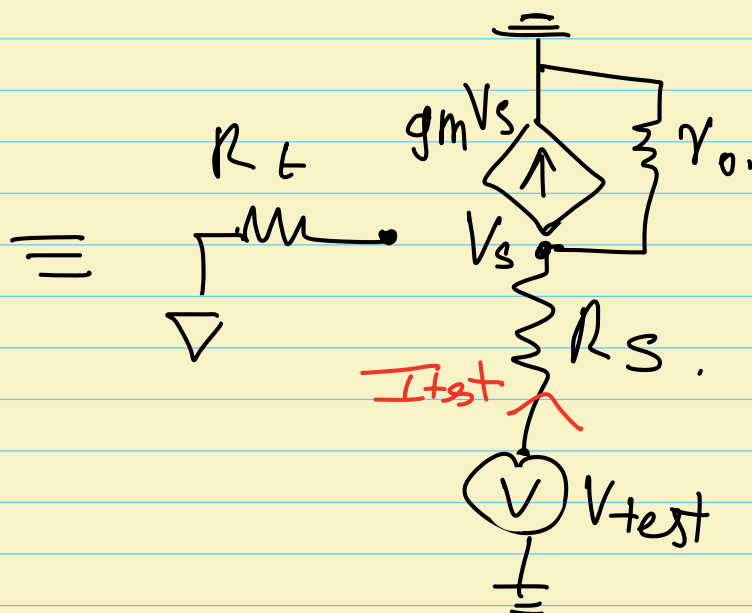
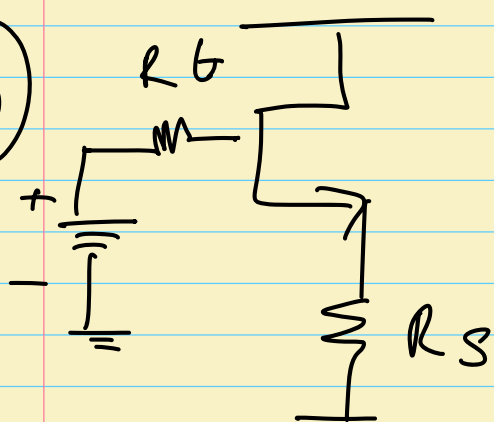
1) a)



$$R_{in} = \infty$$

Reason: gate is open ckt.

b)



$$I_{test} = \frac{V_{test} - V_s}{R_s} = g_m V_s + \frac{V_s}{r_o}$$

$$V_{test} - V_s = g_m V_s R_s + \frac{V_s R_s}{r_o}$$

$$V_{test} = V_s \left[ 1 + g_m R_s + \frac{R_s}{r_o} \right]$$

$$I_{test} = V_{test} - \frac{V_{test}}{\left[ 1 + g_m R_s + \frac{R_s}{r_o} \right]}$$

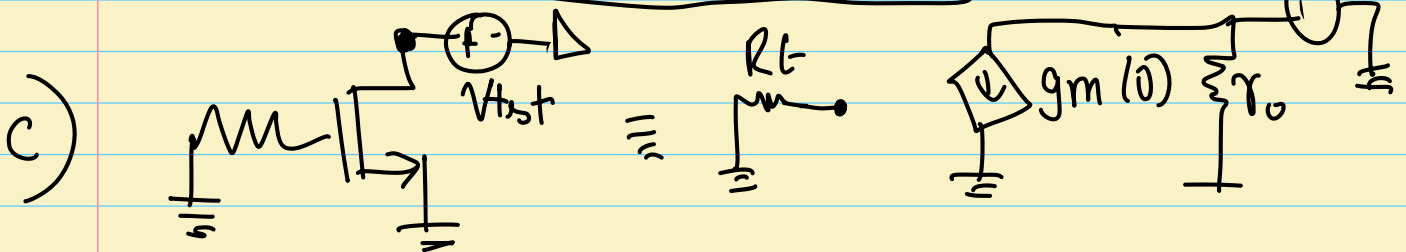
$R_s$ .

$$I_{test} = \frac{V_{test} [g_m R_s + R_s / r_o]}{R_s [1 + g_m R_s + R_s / r_o]}$$

$$\therefore R_{eq} = R_s \left[ \frac{1 + g_m R_s + R_s / r_o}{g_m R_s + R_s / r_o} \right]$$

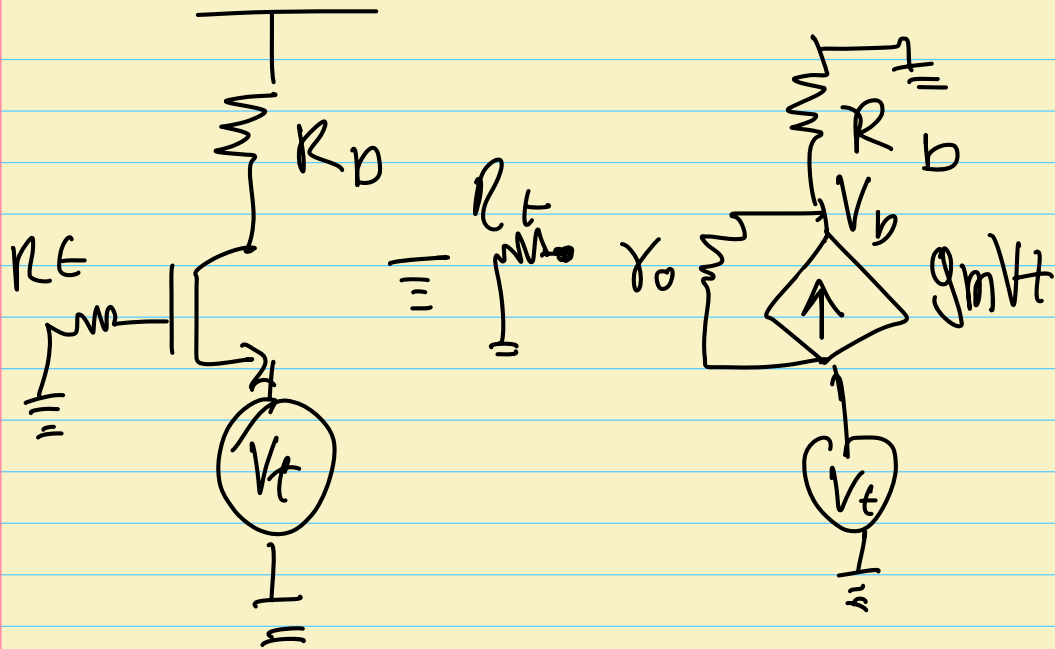
$$= R_s + \frac{R_s}{g_m R_s + R_s / r_o}$$

$$R_{eq} = R_s + \frac{r_o}{1 + g_m r_o}$$



$$r_{eq} = r_o$$

d)



$$I_x = \frac{V_D}{R_D} = \frac{V_t - V_D}{r_o} + g_m V_t,$$

$$\therefore \frac{r_o V_D}{R_D} = V_t - V_D + g_m r_o V_t$$

$$\therefore V_D \left[ 1 + \frac{r_o}{R_D} \right] = V_t [1 + g_m r_o]$$

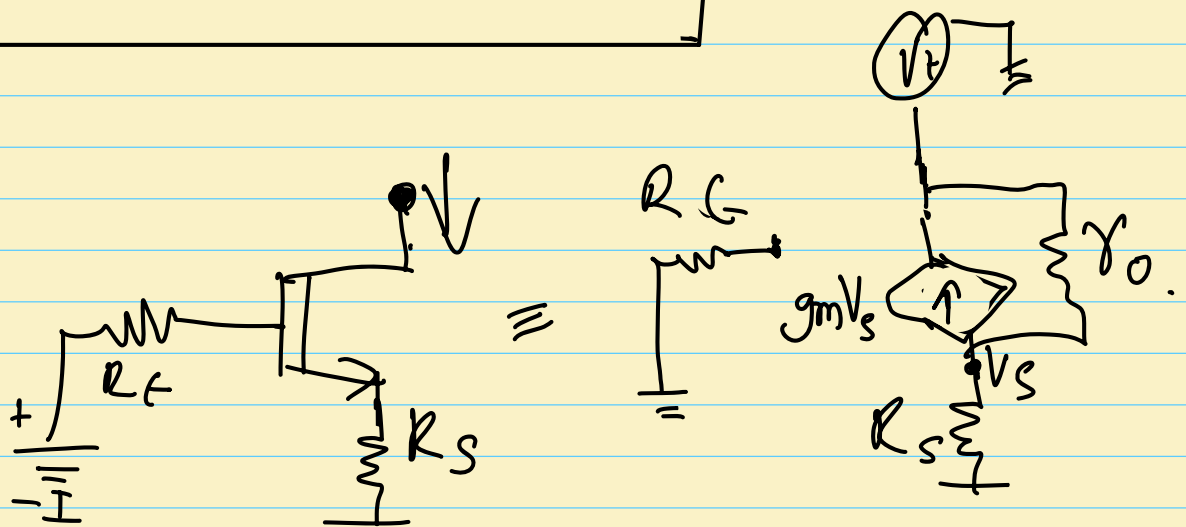
$$\therefore V_D = V_t \frac{[1 + g_m r_o]}{\left[ 1 + \frac{r_o}{R_D} \right]}$$

$$\therefore I_{x+} = \frac{V_t [1 + g_m r_o]}{R_D \left[ 1 + \frac{r_o}{R_D} \right]}$$

$$\therefore I_t = \frac{V_t [1 + g_m r_o]}{R_D + r_o}$$

$$\therefore R_{eq} = \frac{R_D + r_o}{1 + g_m r_o}$$

c)



$$\therefore I_t = \frac{V_s}{R_S} = g_m V_s + \frac{V_t - V_s}{r_o}$$

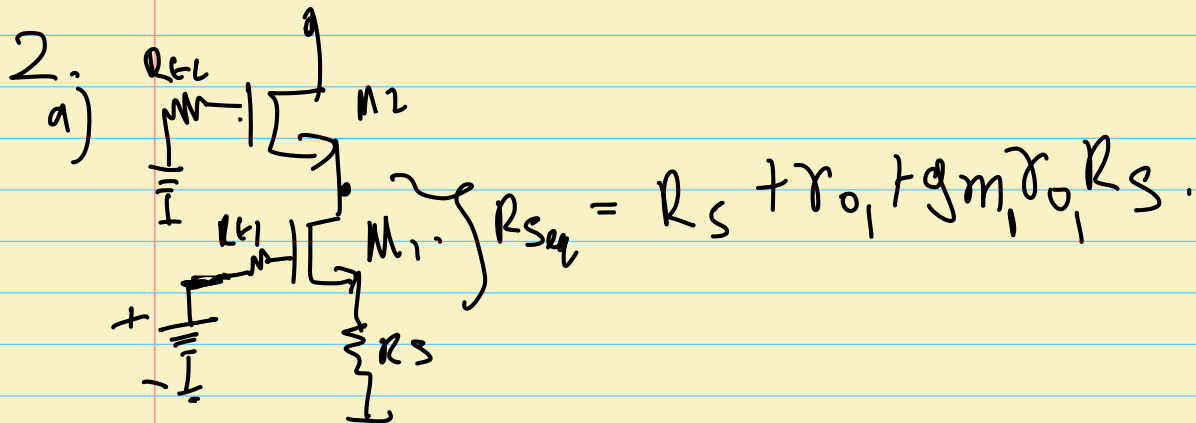
$$\therefore \frac{V_s r_o}{R_S} = -g_m r_o V_s + V_t - V_s$$

$$\therefore V_t = V_s \left[ \frac{r_o}{R_S} + g_m r_o + 1 \right]$$

$$\frac{V_t}{R_S \left[ \frac{r_o}{R_S} + g_m r_o + 1 \right]} = I_t$$

$$\frac{V_t}{r_o + g_m r_o R_s + R_s} = I_t$$

$$R_{eq} = R_s + r_o + g_m r_o R_s$$



$$R_{eq} = R_{seq} + r_{o2} + g_{m2} r_{o2} R_{seq}.$$

$$R_{eq} = \overbrace{R_s + r_{o1} + g_{m1} r_{o1} R_s}^{R_{seq}} + r_{o2} + g_{m2} r_{o2} R_s + g_{m2} r_{o2} r_{o1} + g_{m2} g_{m1} r_{o2} r_{o1} R_s.$$

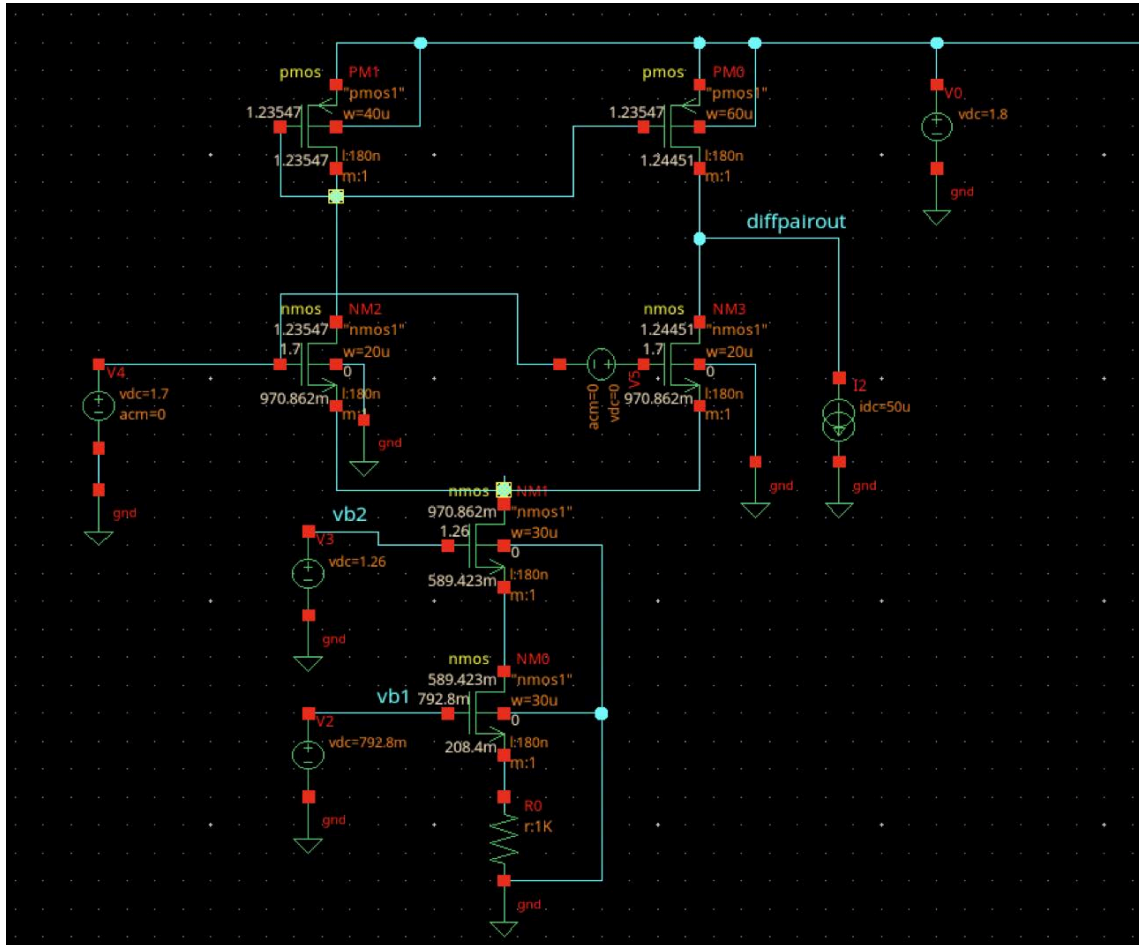


$$R_{eq} = r_{o1} + r_{o2} \parallel \frac{1}{g_{m3}} \parallel r_{o3} \\ + g_{m1} \cdot r_{o1} \cdot (r_{o2} \parallel \frac{1}{g_{m3}} \parallel r_{o3})$$

Q3.

**Transistor bias voltages:**

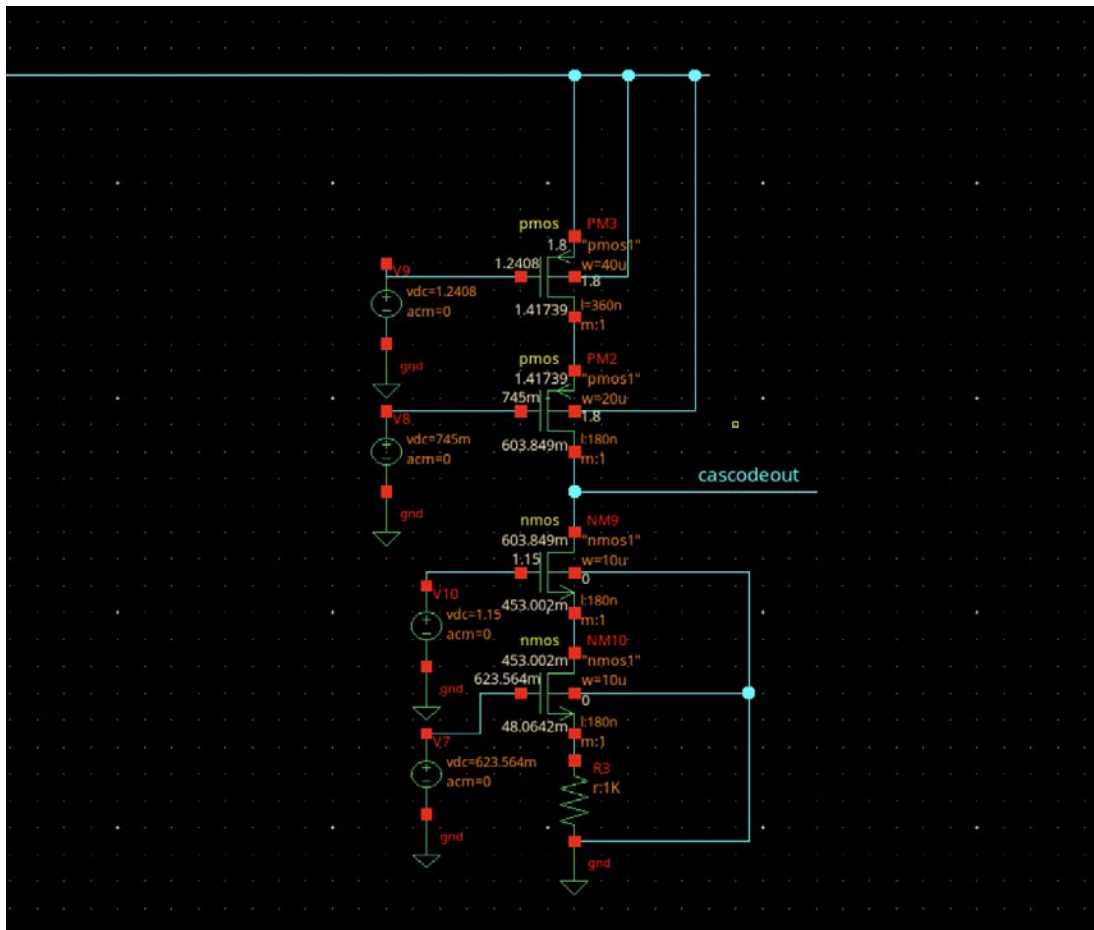
Diff pair:



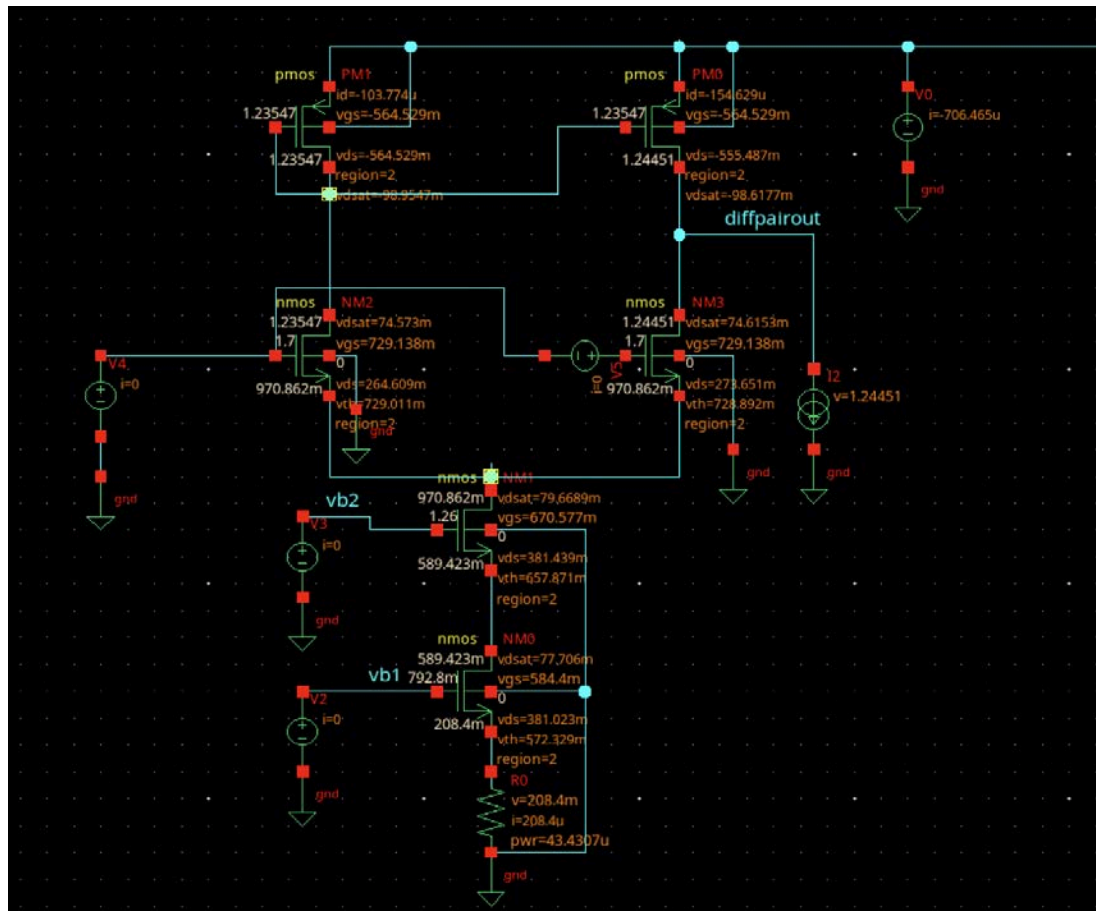
The gates of NM2 and NM3 are biased at 1.7V. Voltage source V5 is set to 0 V.



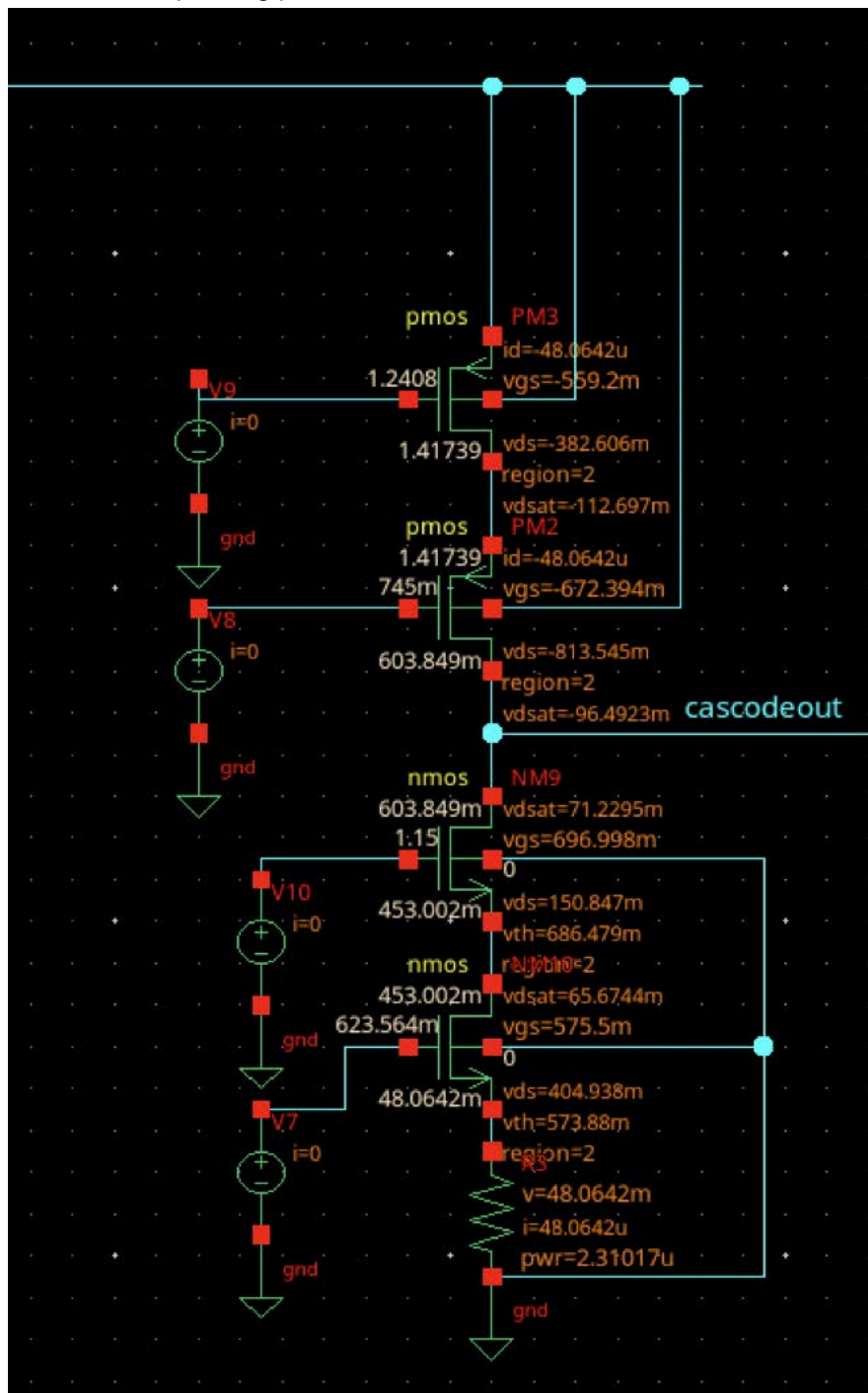
Cascode :



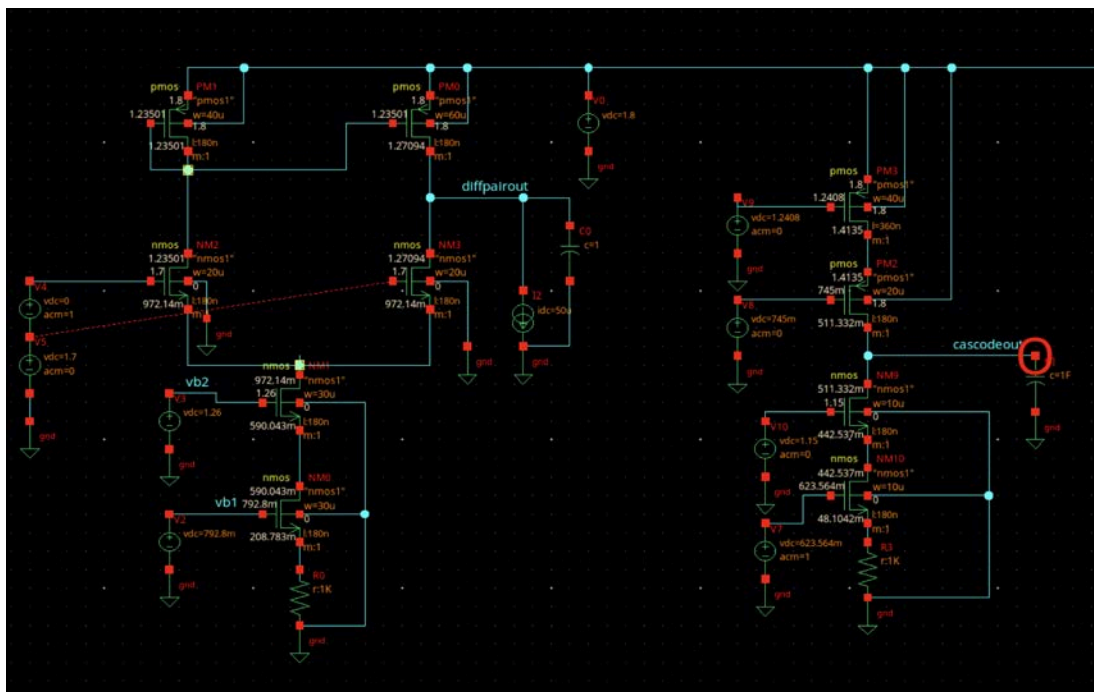
Diff pair:



Cascode DC operating points:

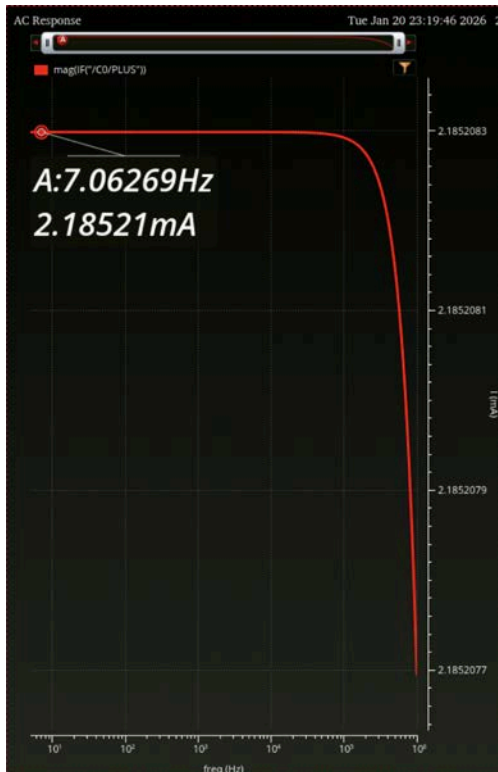


**Gm calculation:** I put a large capacitor at the output node, gave an AC input of 1 volt to the input transistor and measured the output current going into the large capacitor.

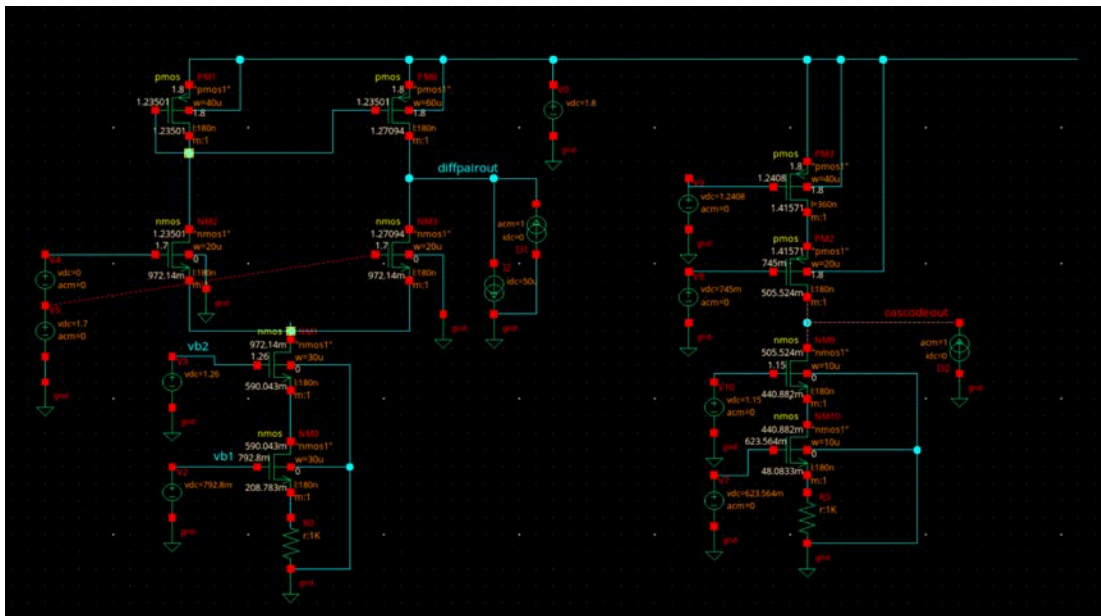


Diffpair measured Gm = 2.18521mS

Cascode measured Gm = 392.832 uS

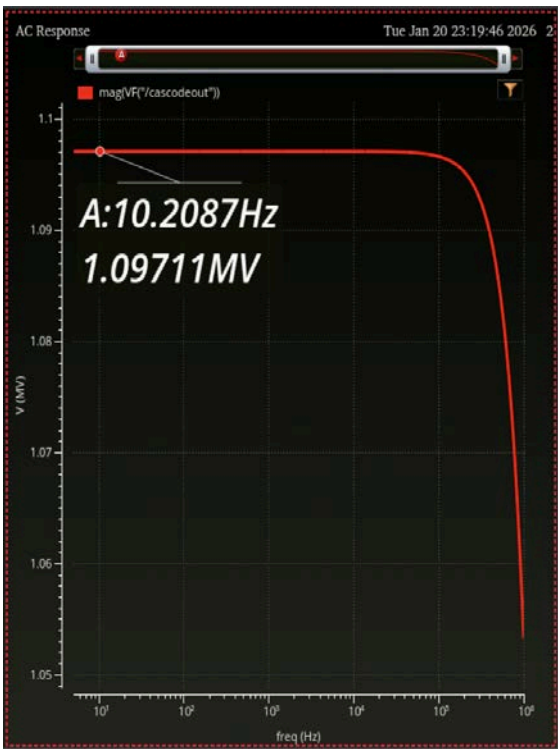
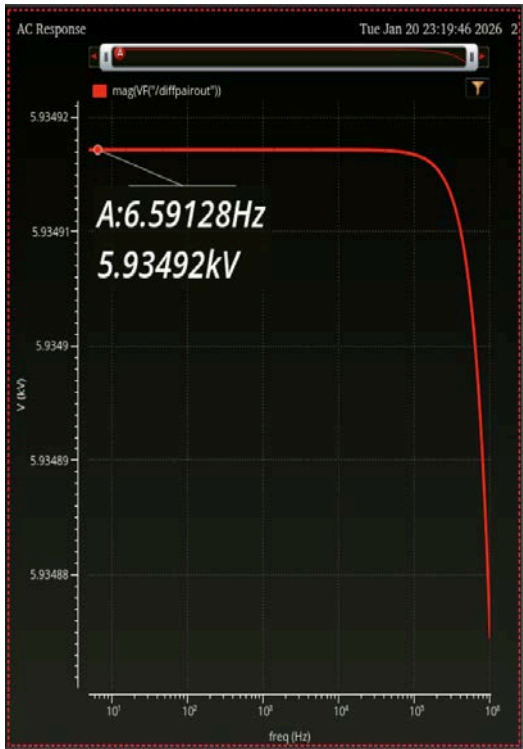


**Rout calculation:** I put an AC current source of 1 A at the output, shorted the AC inputs to gnd, then measured the voltage developed at the output node.



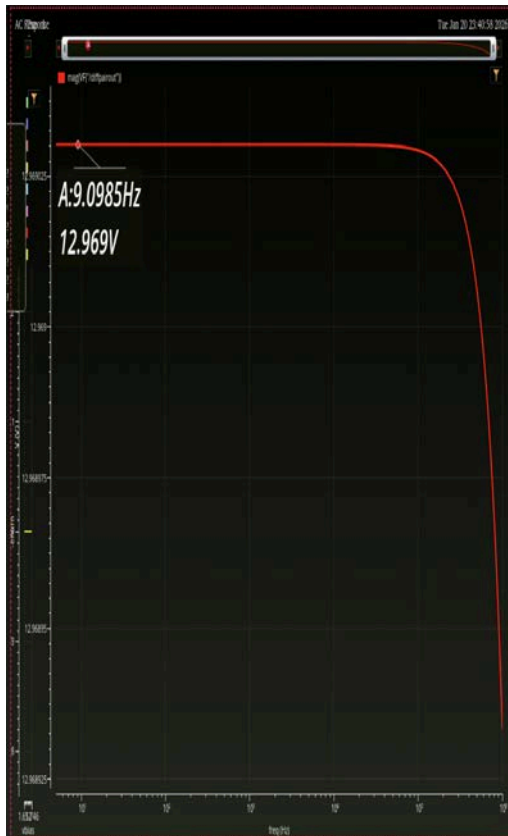
Diff pair Rout: 5.93492 Kilo Ohms

Cascode Rout: 1.09711 Mega Ohms



Diffpair Gm\*Rout gain =  $2.18521 \text{ mS} * 5.93492 \text{ kohm} = 12.96904653$   
 Cascode Gm\*Rout gain =  $392.832 \text{ uS} * 1.09711 \text{ Mega Ohms} = 430.9799155$

Measured gain through regular AC gain simulation:



Diff pair gain: 12.969 V/V

Cascode gain = 430.98 V/V

The gains from both methods match