ECE 423/523 – CMOS Integrated Circuits II

Problem Set #4

Design a differential input singled-ended output *folded-cascode* operational amplifier meeting the following specifications. Use one ideal current source tied to ground for bias and one ideal voltage source for V_{DD}. Simulations should be performed using 0.18µm CMOS models (on class web page) with ad=as=W·(0.5µm) and pd=ps=2·W+1µm. If you have some other working Cadence setup for 0.18µm CMOS (e.g. ECE 4/522 setup), you may use that instead (probably the path of least resistance). Simulations are to be completed for three "cases/corners" including *typical* (temp=27ºC), *slow* (temp=100ºC), and *fast* (temp=-40ºC). Temperature is specified using the *.TEMP* command (in the netlist). Use ideal resistors and capacitors for simulation, but +20% values for *slow* case and –20% for *fast* case. Your goal should be to meet the specifications for all three cases. If you do not meet specifications for all cases/corners, comment why you could not meet certain specs. In the test bench use any fixed ideal input common-mode voltage for all cases.

Specifications

Power supply	V_{DD}=1.8V
Load	C_{load}=6pF±1.2pF
DC gain	> 50 dB
Unity-gain BW	> 200 MHz
Phase Margin	> 60 º
Output swing	> 0.5 Vpp
Power consumption	< 12 mW
Input-referred systematic offset	< 3mV

There are some useful reading materials in Gray/Hurst/Lewis/Meyer text:
e.g. MOS current mirrors & MOS opamps with cascodes