Once again let me point out that W/L dimensions should be separated and clearly annotated in the schematic itself. I'm commenting w.r.t. final project writeup. One should really separately draw the schematic with W/L dimensions (even clearly hand drawn is fine). If you do not separately draw up the schematic, you should at least figure out a way to invert the schematic so there is no black background (and eliminate the miscellaneous annotations that might be useful for simulation but not useful for reviewing the writeup).

# ECE 423 HW 4

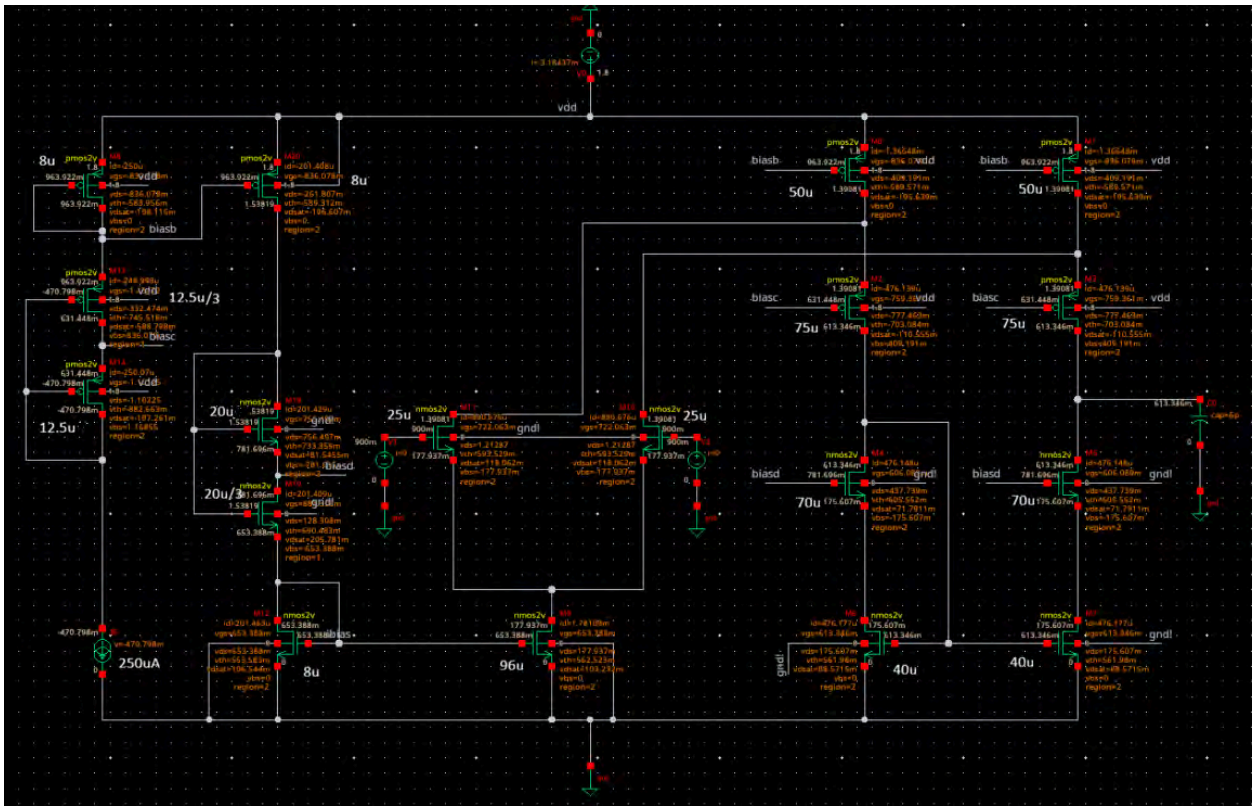


**Figure 1:** Folded Cascode Circuit

| | Specifications | 27°C | 100°C | -40°C |
|---|---|---|---|---|
| **DC Gain** | > 50 dB | 51.89 dB | 51.19 dB | 52.45 dB |
| **Unity-Gain BW** | > 200 MHz | 341 MHz | 252 MHz | 503.187 MHz |
| **Phase Margin** | > 60° | 82° | 84° | 80° |
| **Output Swing** | > 0.5 Vpp | 0.8 Vpp | 0.9 Vpp | 0.86 Vpp |
| **Power Consumption** | < 12 mW | 5.73 mW | 5.89 mW | 5.55 mW |
| **Systematic Offset** | < 3 mV | 1.436 mV | 1.785 mV | 1.171 mV |

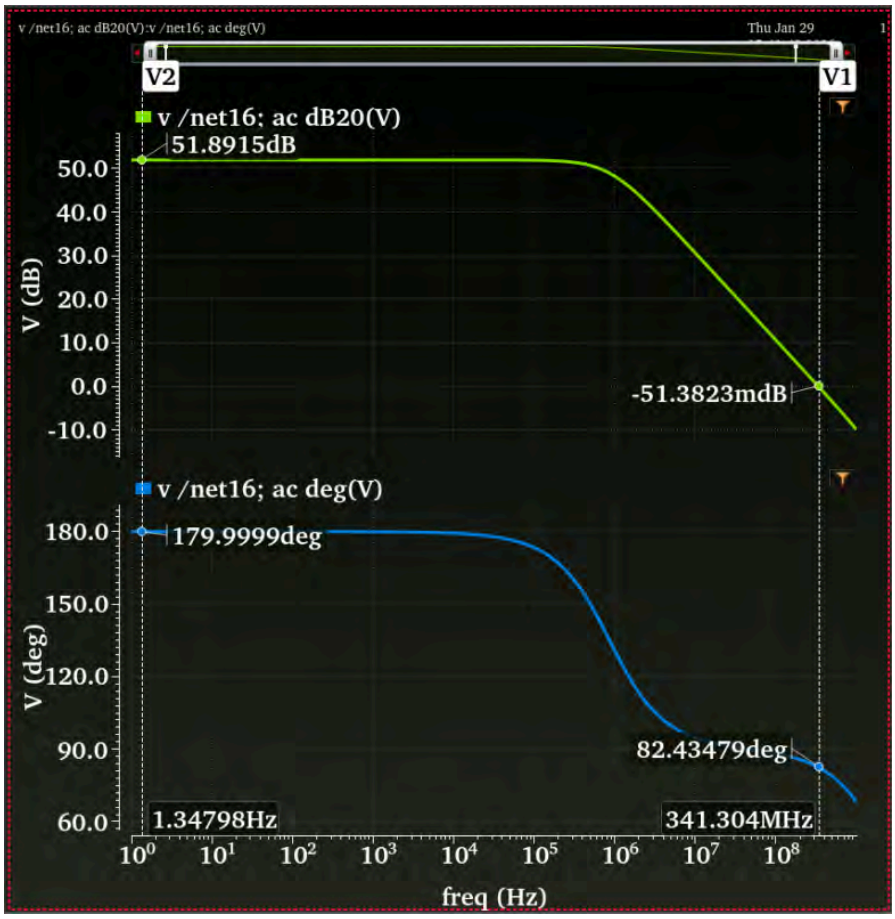


**Figure 2:** Gain & Phase Margin for 27°C & 6pF Capacitor

The **27°** temperature gave a gain of **51.89 dB**, phase margin of **82°,** unity-gain bandwidth of **341 MHz** and pulled a current of **3.1844 mA** causing a **5.73 mW** power consumption. Meeting all of the specifications wanted in the problem statement.

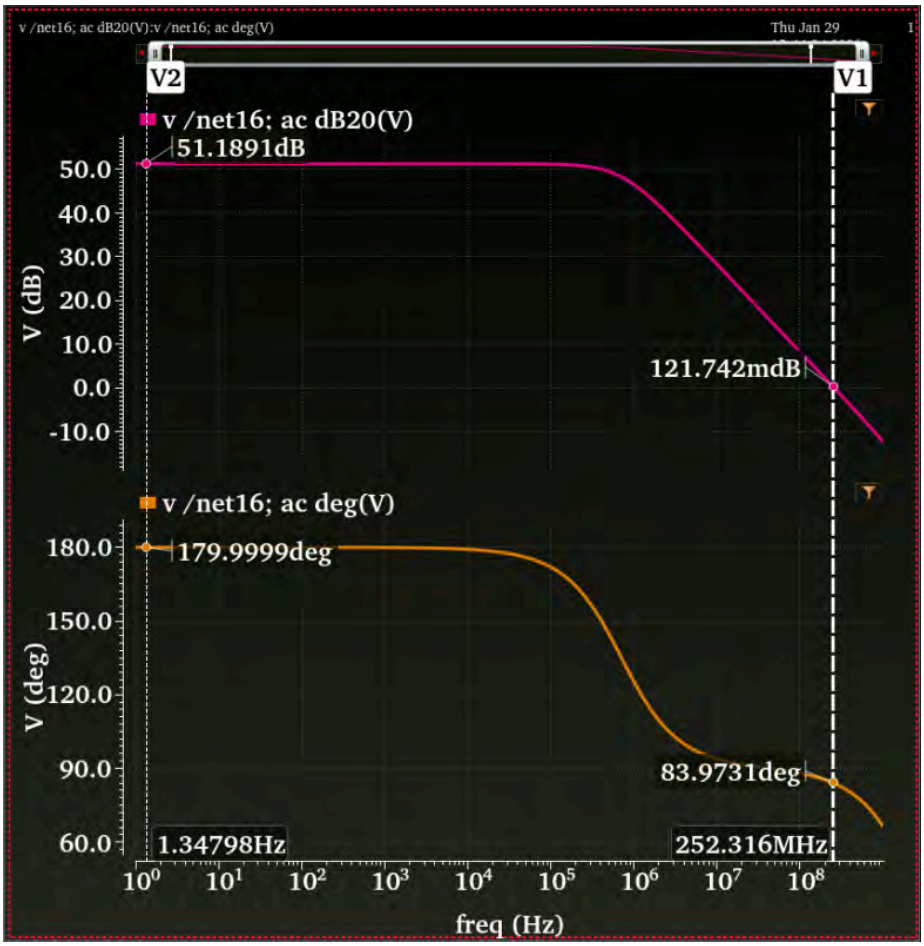


**Figure 3:** Gain & Phase Margin for 100°C & 7.2pF Capacitor

The **100°** temperature gave a gain of **51.18 dB**, phase margin of **84°,** unity-gain bandwidth of **252 MHz** and pulled a current of **3.2761 mA** causing a **5.89 mW** power consumption. Meeting all of the specifications wanted in the problem statement. For a high temperature, the gain and UGB went down while everything else went up.

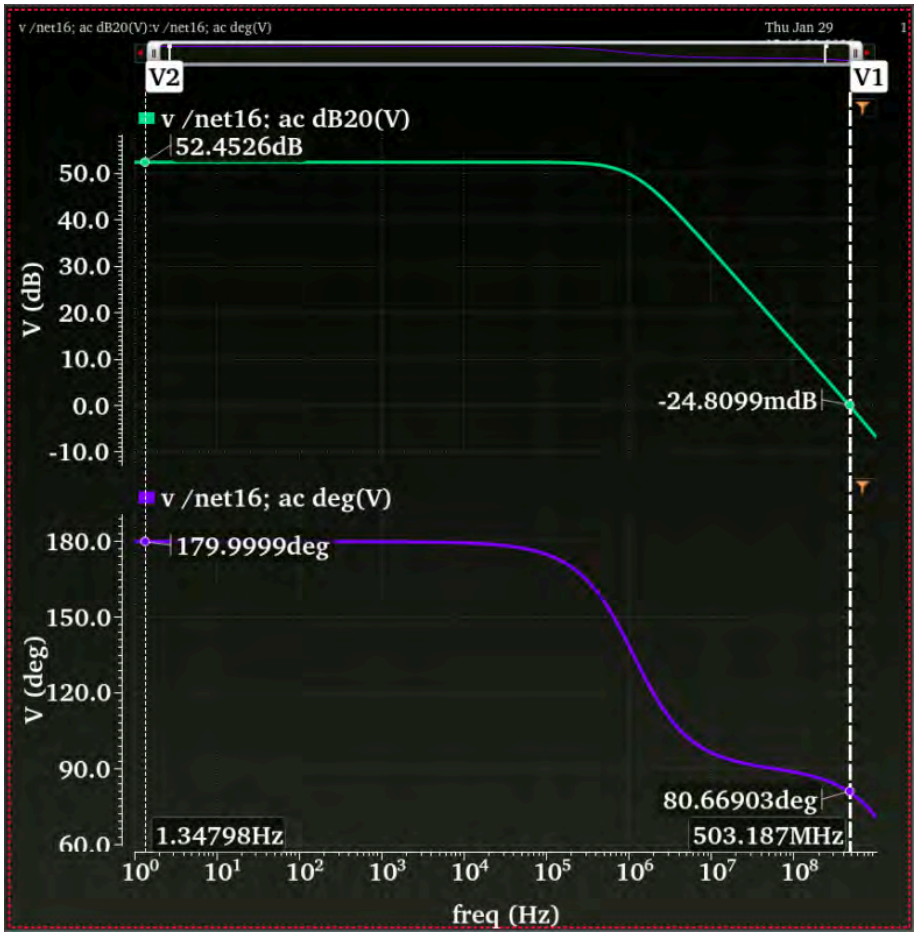


**Figure 4:** Gain & Phase Margin for -40°C & 4.8pF Capacitor

The **-40°** temperature gave a gain of **52.45 dB**, phase margin of **80°,** unity-gain bandwidth of **503 MHz** and pulled a current of **3.0845 mA** causing a **5.55 mW** power consumption. Meeting all of the specifications wanted in the problem statement. For a low temperature, the gain, phase margin, power consumption, systematic offset, and UGB went down while everything else went up.

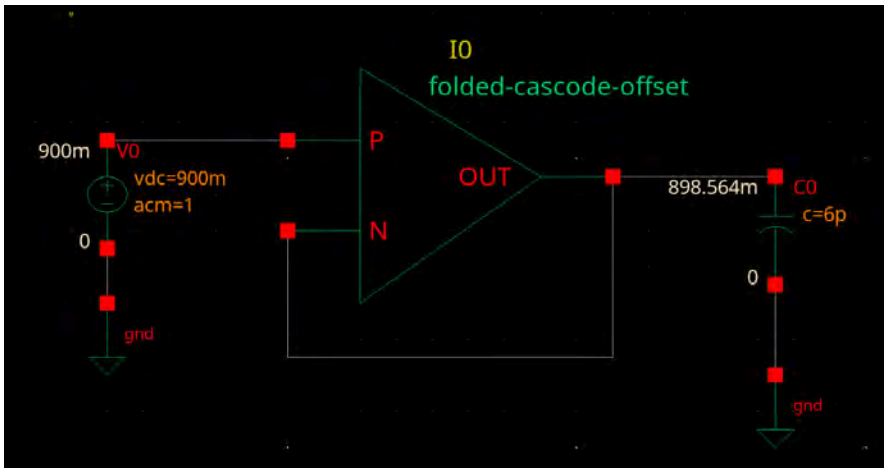


**Figure 5:** Systematic Offset for 27°C & 6pF Capacitor

The input-referred systematic offset for **27°** was 900mV - 898.564 mV = **1.436 mV**.

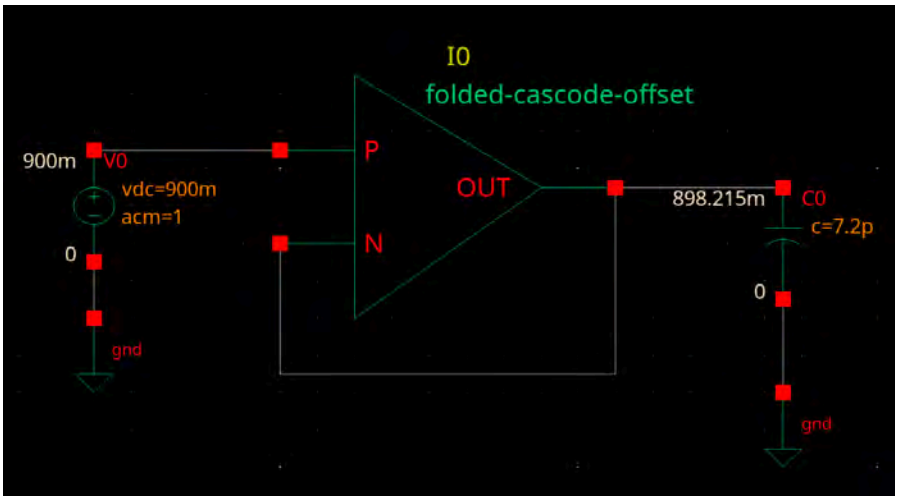


**Figure 6:** Systematic Offset for 100°C & 7.2pF Capacitor

The input-referred systematic offset for **100°** was 900mV - 898.215 mV = **1.785 mV**.

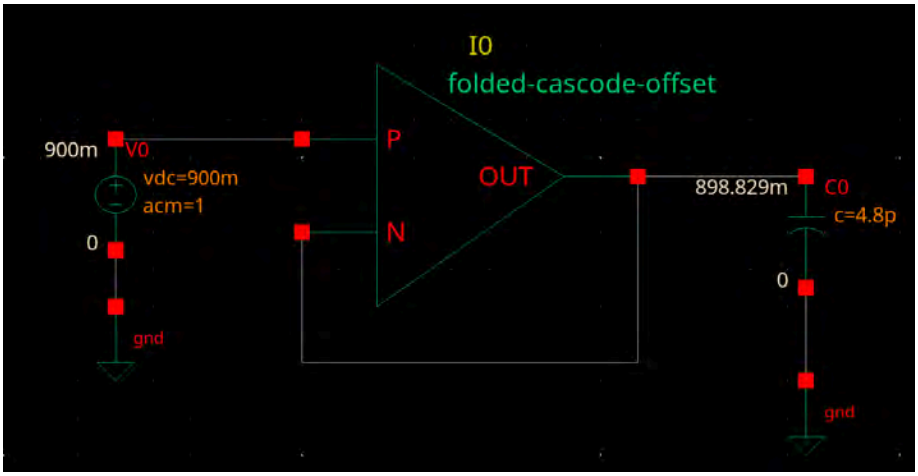


**Figure 7:** Systematic Offset for -40°C & 4.8pF Capacitor

The input-referred systematic offset for **-40°** was 900mV - 898.829 mV = **1.436 mV**.

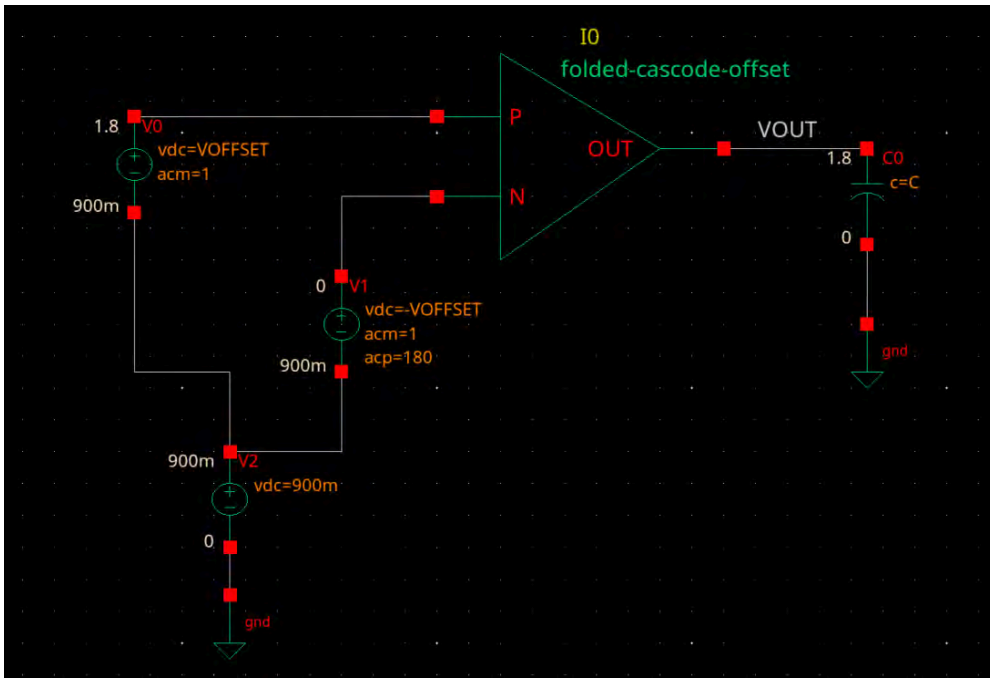


**Figure 8:** Testbench for Output Swing

**Figure 8** shows the testbench set up I used to graph and calculate the output swing for each temperature and capacitor value.

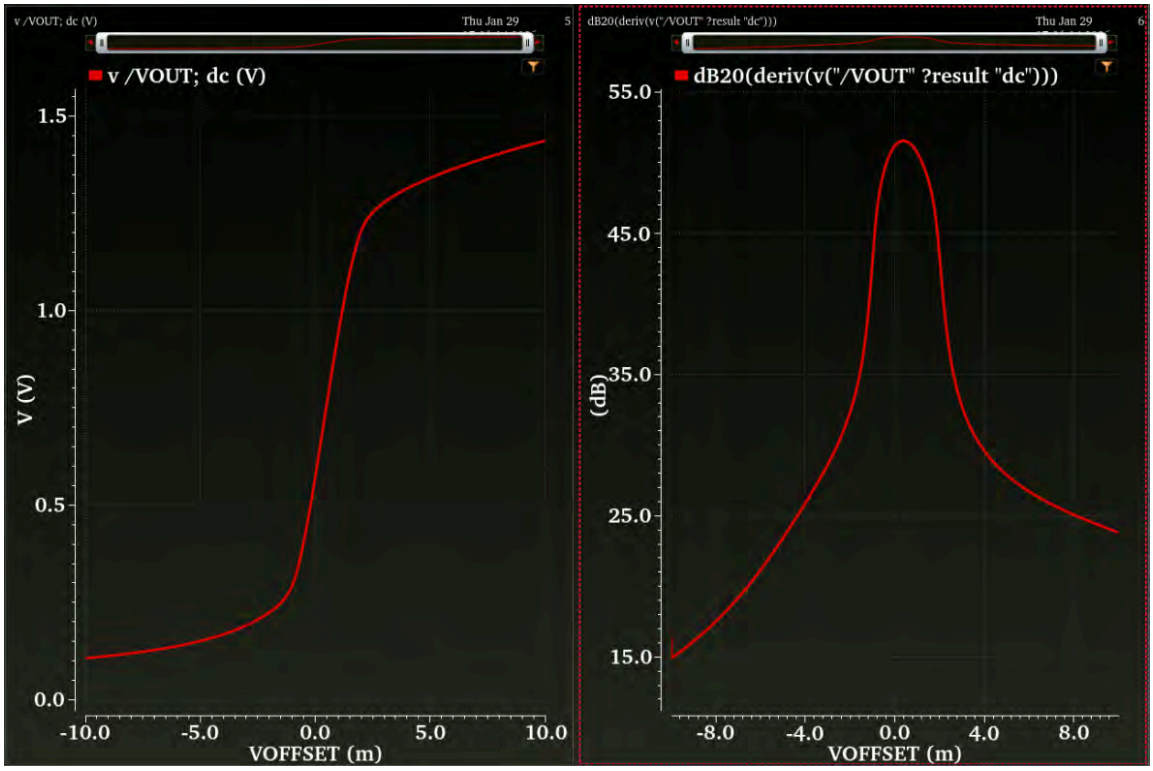


**Figure 9:** Measurements Taken to Plot Output Swing

After running a DC sweep for the offset from -10 mV to 10 mV and an AC analysis, I plotted the DC voltage and took the db20 of the derivative of it. Combining these two graphs together, I utilized the Y vs. Y function on the graph to get the output swing curve.

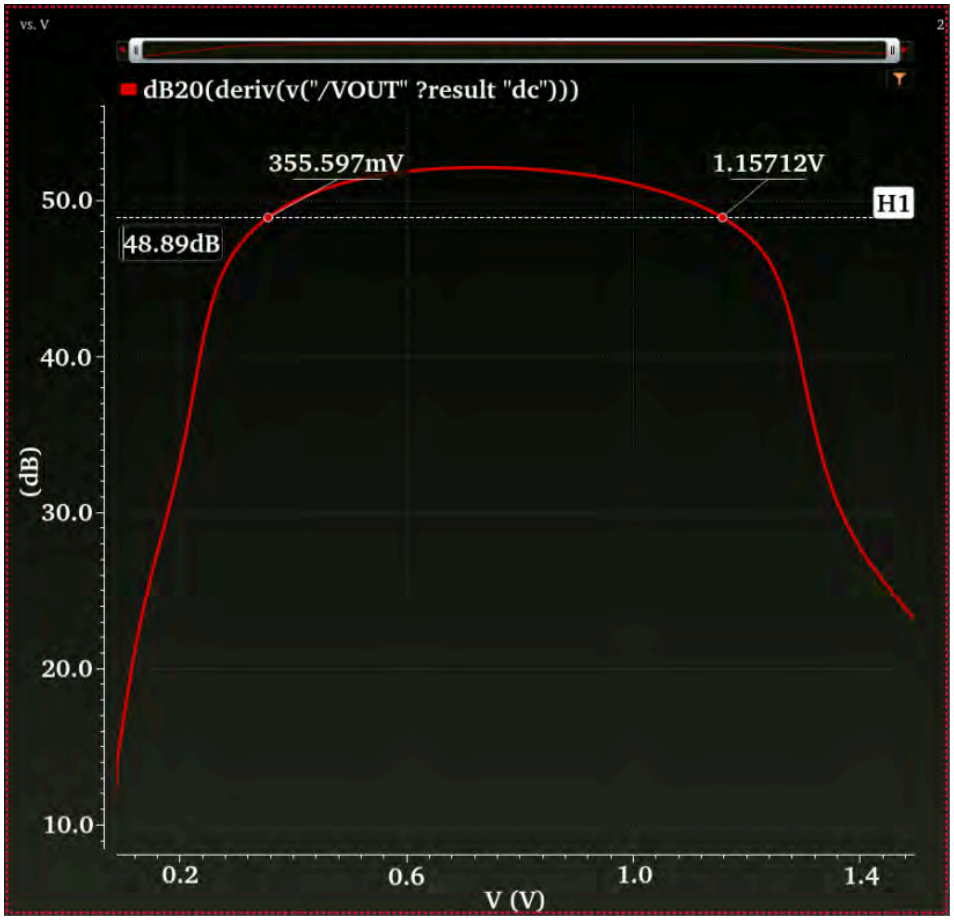


**Figure 10:** Output Swing Graph for 27° & 6pF Capacitor

For **27°** I marked a line at -3 dB from the peak (51.89 dB) gain to get the output swing of **0.8 V**.

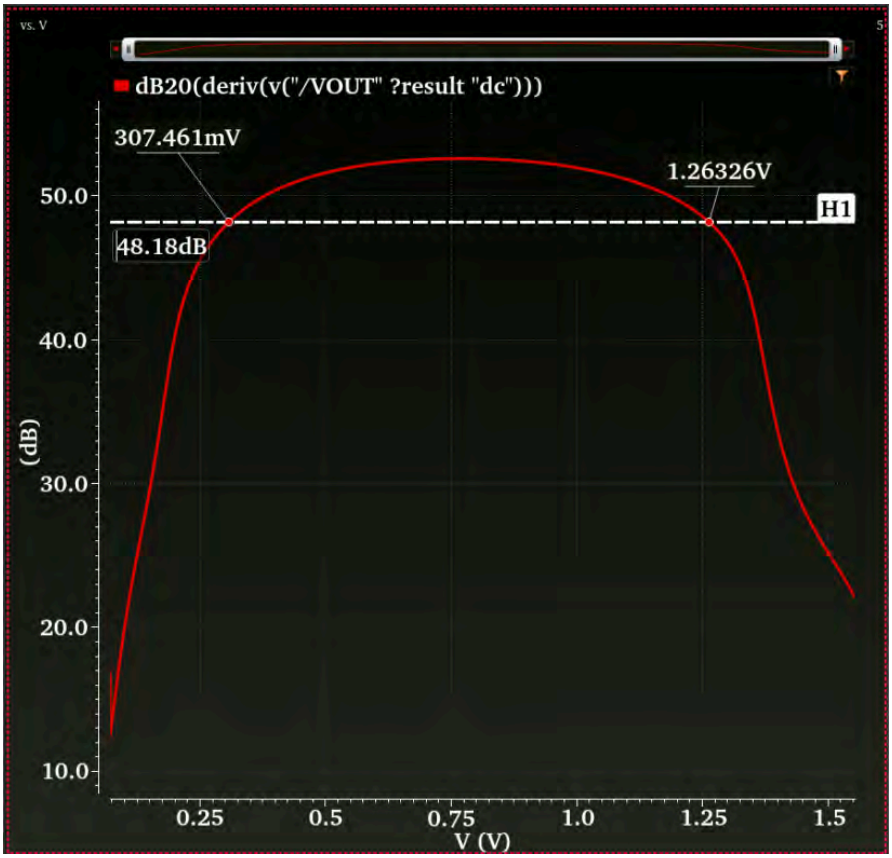


**Figure 10:** Output Swing Graph for 100° & 7.2pF Capacitor

For **100°** I marked a line at -3 dB from the peak (51.19 dB) gain to get the output swing of **0.9 V**.

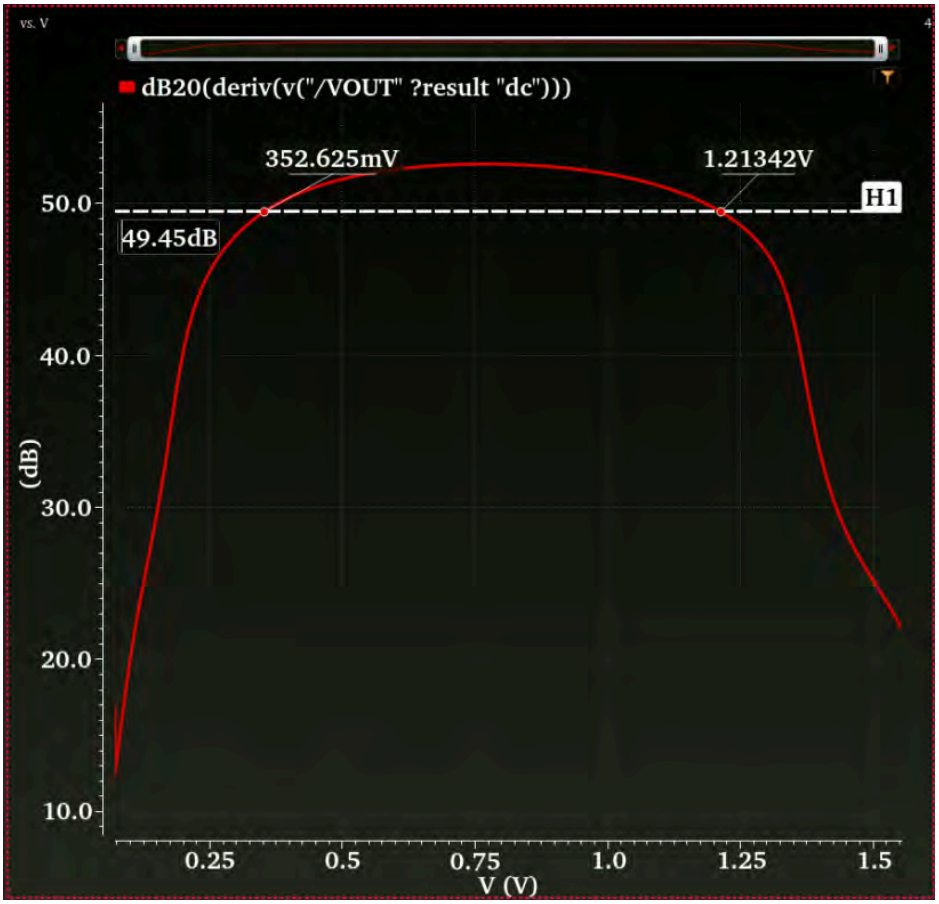


**Figure 10:** Output Swing Graph for -40° & 4.8pF Capacitor

For **-40°** I marked a line at -3 dB from the peak (52.45 dB) gain to get the output swing of **0.86 V**.