ECE 423/523 – CMOS Integrated Circuits II

Problem Set #5

Simulate (transient) the ring oscillator shown below to verify its operation. Then do the layout of this circuit. Layout is to be done in Cadence using the setup for TSMC 0.18um process found at the class layout webpage http://web.engr.oregonstate.edu/~moon/ece423/cadence. Attach small screen shots of your passing DRC and LVS windows. If you do not pass DRC and LVS fully, comment on why you could not pass.

This will be an email submission homework. You need to make a TAR file of your directories and files related to homework and email as an attachment to the TA. The Subject line of the email should say "ECE4/523 – HW5 – *YourName*." Consult the TA if you do not know how to make a TAR file. He may give you a different set of instructions or have more to say about this at the tools/layout lectures.