ECE 423/523 – CMOS Integrated Circuits II

Problem Set #6

Take a prior opamp design (either of the designs from hw4 or hw1) and do IC layout of the opamp using Cadence. If you did not use a resistor in the opamp, please use one somewhere (e.g. in place of the ideal reference current source – just to practice using these). Also go ahead and put an output load capacitor if your opamp does not include one (more practice). You have to edit the schematic, of course, to make LVS work. Perform DRC and LVS to show that the layout matches schematic and all layout design rules are met.

This is an email submission homework, like the last one (hw5). You need to make a TAR file of your stuff and email it to TA with the Subject line of the email "ECE4/523 – HW6 – *YourName*" and whatever the TA told you to do. Now you should definitely know how to do this (same as hw5). The TA will perform DRC and LVS of your files to verify your work.