ECE 423/523 – CMOS Integrated Circuits II

Problem Set #7

This is your LAST homework assignment.

Take an existing opamp design (e.g. hw4 or hw1) and convert it to a fully differential output opamp with common-mode feedback (CMFB).

Use an ideal voltage source (you choose the voltage) as the output common-mode voltage reference. In the test bench use any fixed ideal input common-mode voltage.

Specifications (fill in with your design results in the empty places)

Power supply	1.8V
Load	10pF (for each of the two output nodes to ground)
**Differential *loop* gain	-
**Differential *loop* UGBW	-
**Differential *loop* PM	-
CMFB loop gain	-
CMFB loop UGBW	-
CMFB loop PM	> 45°
Output CM accuracy/error	< ±0.1V
Output swing	-
Power consumption	-

** Differential loop characteristics should be obtained with 1pF input and feedback capacitors. You may use 1GΩ resistors for simulation as/where needed.

Eliminate the differential feedback (1pF capacitors) when doing CMFB evaluation.