1 Project Overview

1.1 Specifications and Results

Parameter	Specification	Achieved
Power Supply	1.8 V	1.8 V
Load Capacitance	10 pF (each output)	10 pF
Temperature	–	27 °C
Differential Loop Performance		
Differential Loop Gain	–	34.07 dB
Differential Loop UGBW	–	33.14 MHz
Differential Loop PM	–	91.51°
CMFB Loop Performance		
CMFB Loop Gain	–	32.73 dB
CMFB Loop UGBW	–	27.77 MHz
CMFB Loop PM	$> 45°$	88.62°
DC Performance		
Output CM Accuracy/Error	$< \pm 0.1$ V	± 89.8 mV
Output Swing (Differential)	–	1.2562 V_{pp}
Power Consumption	–	5.41 mW

Table 1: Design Specifications and Performance Results

The usual reminder that you should specify W/L in the schematic that's easy to read. I'm referring to PROJECT write-up. Even if it's a paste of a text like I've demonstrated below for one transistor...

2 Schematics

2.1 Main Amplifier Schematic

BP1 is generated with L=0.54 device in the bias, but here it's biasing couple of L=0.36 devices (far left and right). That should be avoided pretty much always (L should match for current setting devices).

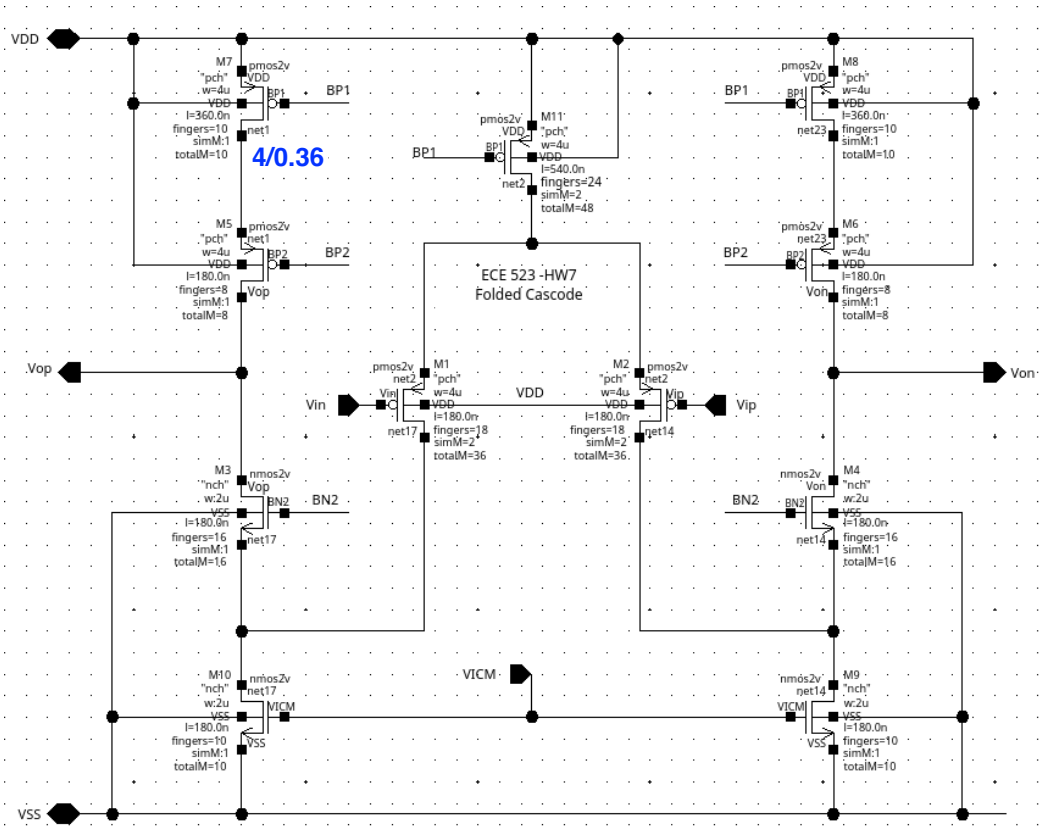


Figure 1: Fully Differential Folded-Cascode Amplifier Schematic

Also helps to specify nominal current you intend for each branch… illustrated for 2.3 Bias Network, for example. Do this for all branches in all of your design.

2.2 CMFB Circuit Schematic

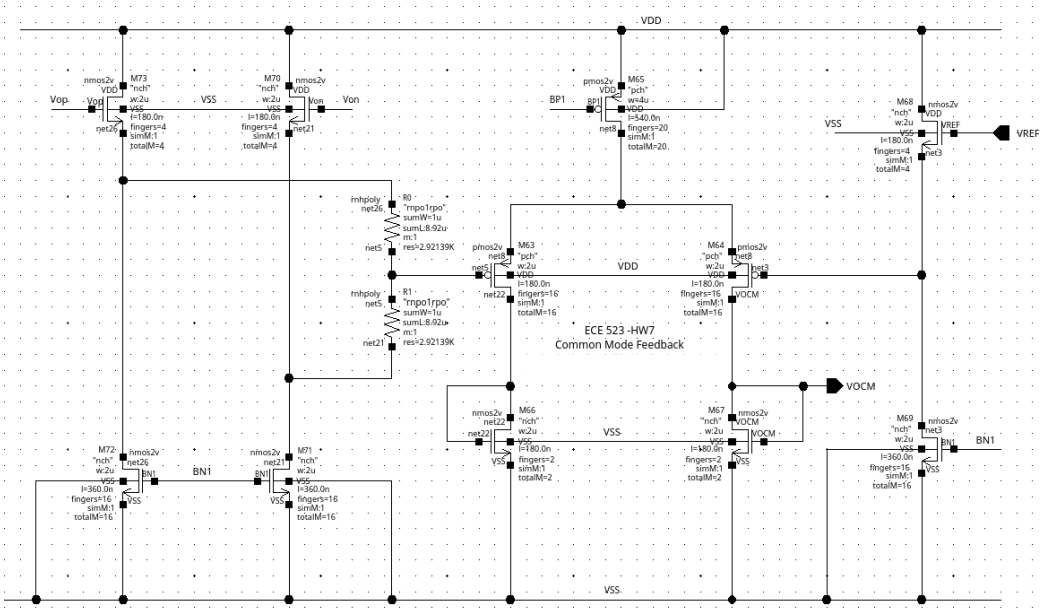


Figure 2: Common-Mode Feedback Circuit Schematic

2.3 Bias Network

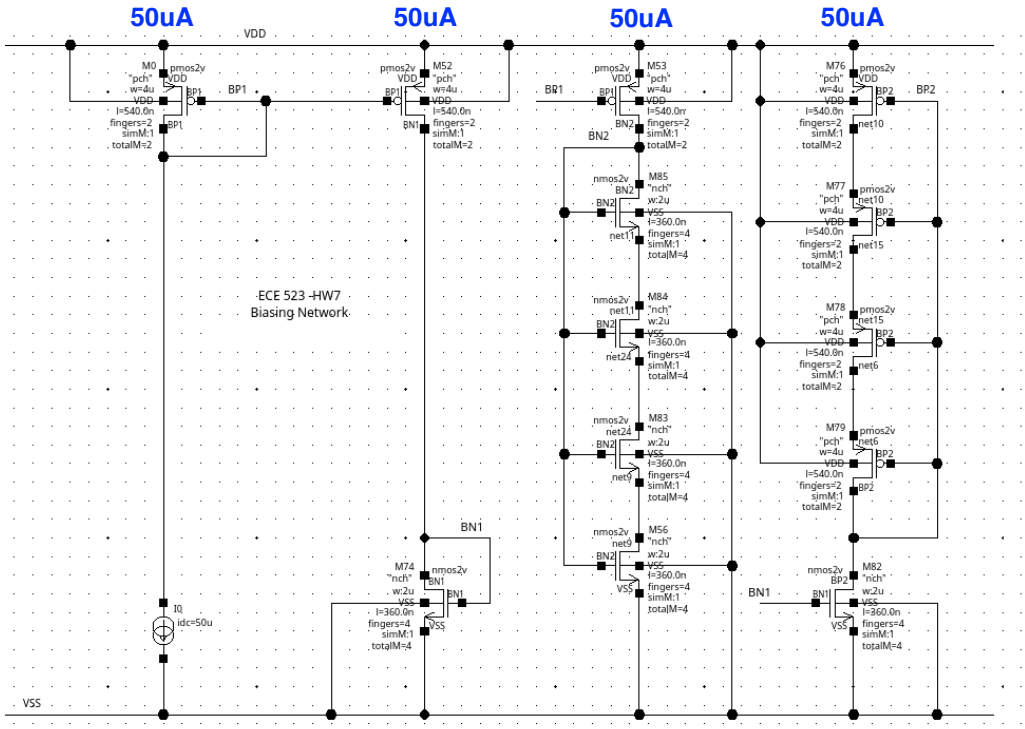


Figure 3: Bias Network

3 Simulation Results

3.1 Differential Loop

3.1.1 Test Bench

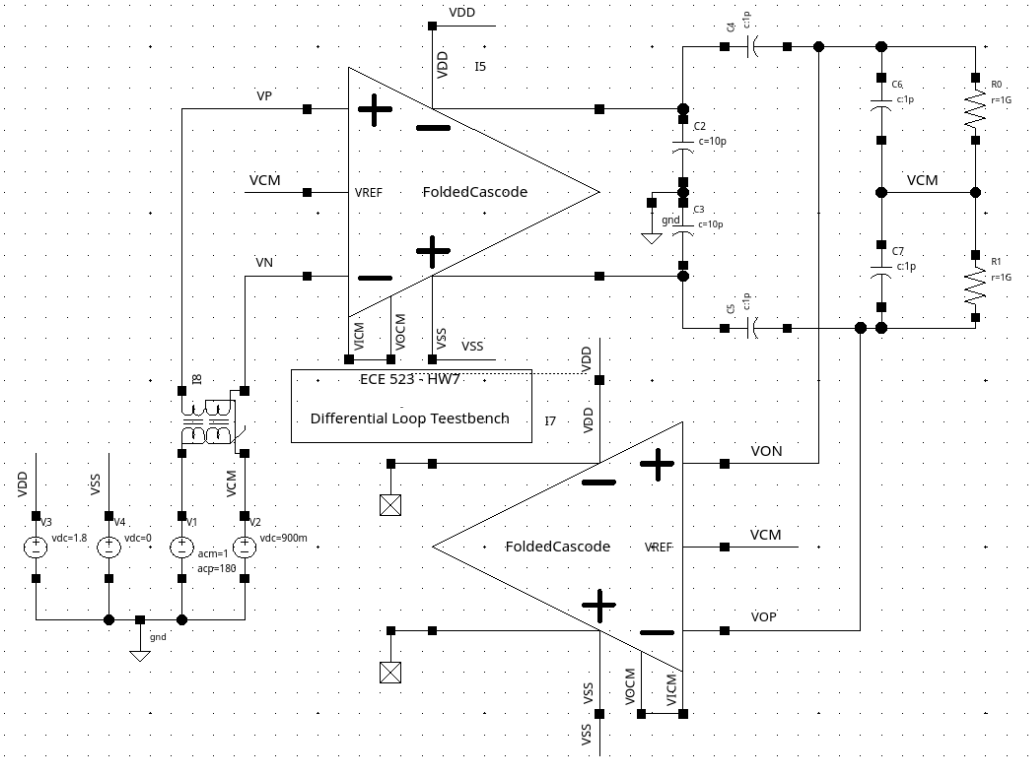


Figure 4: Differential Loop Testbench Configuration

3.1.2 Frequency Response

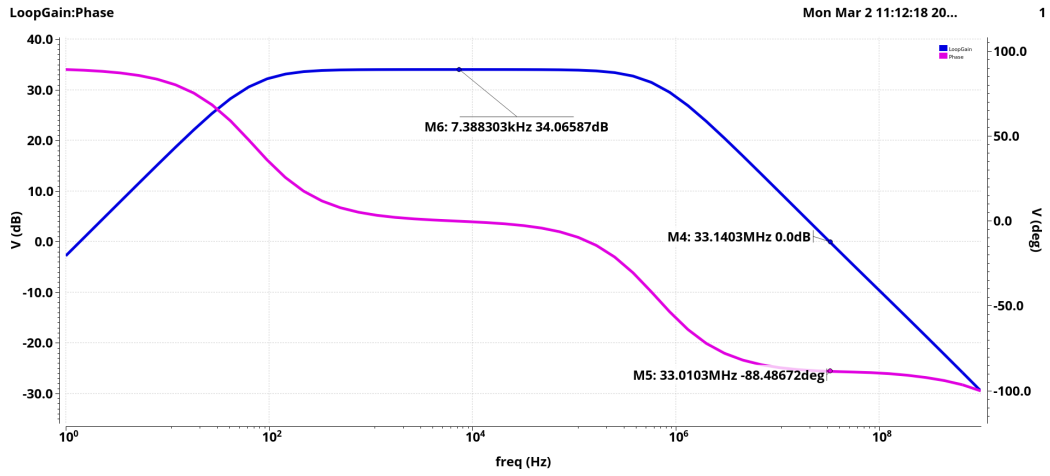


Figure 5: Differential Loop Frequency Response (Gain and Phase)

Results Summary:

- Differential Loop Gain: 34.07 dB
- Unity-Gain Bandwidth: 33.14 MHz
- Phase Margin: $|-180^\circ - (-88.48672^\circ)| = 91.513\,28^\circ$

3.2 Common-Mode Feedback Loop

3.2.1 Test Bench

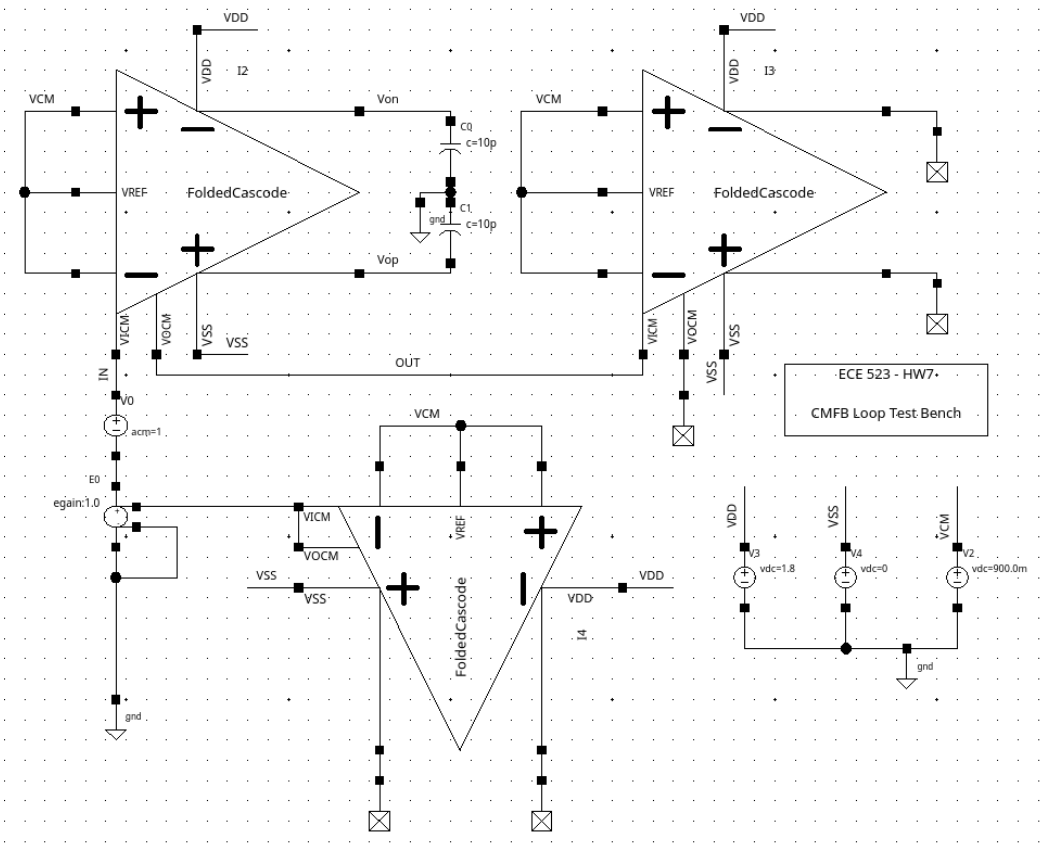


Figure 6: CMFB Loop Testbench Configuration

3.2.2 Frequency Response

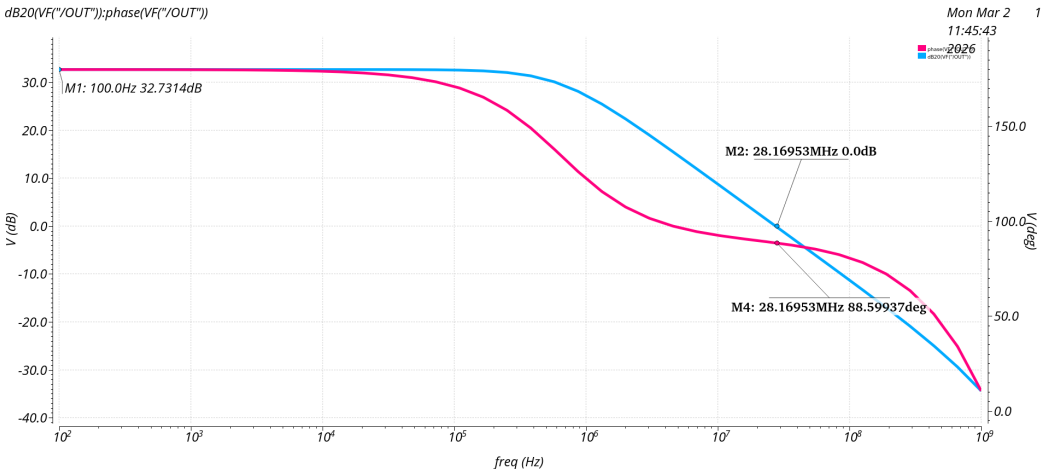


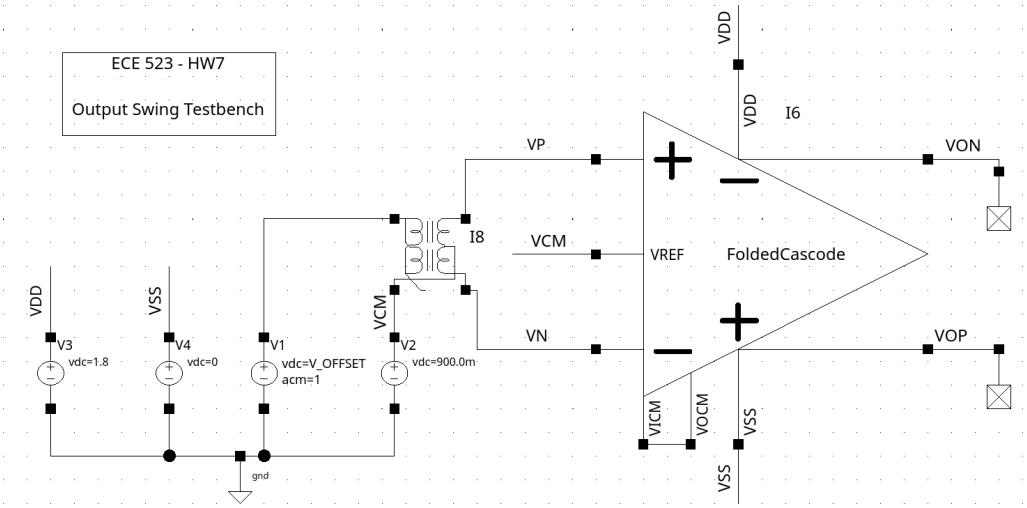
Figure 7: CMFB Loop Frequency Response (Gain and Phase)

Results Summary:

- CMFB Loop Gain: 32.7314 dB
- Unity-Gain Bandwidth: 27.7677 MHz
- Phase Margin: 88.621° (Spec: $> 45°$)

3.3 DC Analysis and Output Swing

3.3.1 Output Swing Test Bench



3.3.2 Output Swing Results

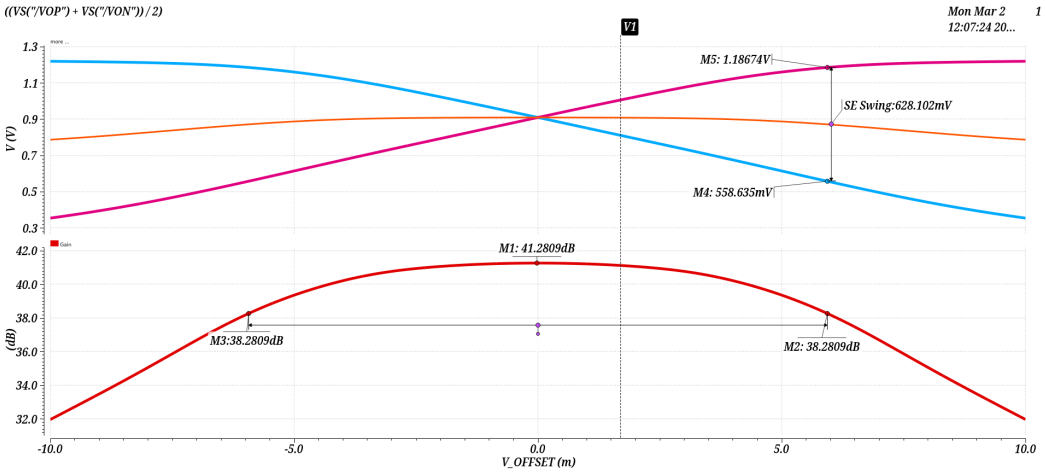


Figure 8: Differential Output Swing Analysis

Output Swing:

- Single-Ended Swing ($V_{o,p}$ or $V_{o,n}$): 628.102 mV
- Differential Swing ($V_{o,p}$ - $V_{o,n}$): 1.2562 V_{pp}

3.3.3 Common-Mode Accuracy and Power Consumption

	Standard	Standard
1	# instance	value [V]
2	/OUT	+7.6502179869E-01
3	/VDD	+1.8000000000E+00
4	/net26	+7.6502179869E-01
5	/VCM	+9.0000000000E-01
6	/VSS	+0.0000000000E+00
7	/net23	+9.0898629939E-01
8	/net22	+9.0898629939E-01
9	/IN	+7.6502179869E-01
10	/Von	+9.0898629939E-01
11	/Vop	+9.0898629939E-01
12	/net63	+7.6502157253E-01
13	/net14	+9.0898629939E-01
14	/net13	+9.0898629939E-01
15	/net60	+7.6502179869E-01

	Standard	Standard
1	# instance	value [W]
2	/:pwr	+5.4129104811E-03

Figure 9: Common-Mode Accuracy and Power Consumption from Results Browser

The Power consumption was taken from the results browser in the Output Swing Testbench, because only one device was instantiated in that test bench. The CM Accuracy was taken from the Results Browse of the CMFB Loop Testbench, and compares the nets Vop and Von to Vcm (Vref) of the DUT.

DC Performance:

- Output CM Reference ($V_{CM,ref}$): 9.000 V
- Output CM Voltage ($V_{CM,out}$): 9.0899 V
- Output CM Error: ± 89.8 mV (Spec: $< \pm 100$ mV)
- Power Consumption: 5.41 mW