

ECE 423/523

Project

Example

Student Name

1. As a general rule, apply commonsense to clearly show what you have done.
2. Create your own material/drawings – there should be no copy/paste from this example found anywhere in your write up.

1) Project Overview

LVS: Passed (if Failed, feel free to comment – just a sentence or two)

DRC: Passed (if Failed, feel free to comment – just a sentence or two)

Table 1: Specifications and Results

| Name | Spec | Slow | Typical | Fast |
|--------------------------------------|-------------|-------|---------|------|
| <i>Power Supply voltage</i> | <i>VDD</i> | 2.25 | 2.5 | 2.75 |
| <i>Output CM voltage</i> | <i>VCM</i> | | 1.0 | |
| <i>Reference current</i> | <i>Iref</i> | | 25uA | |
| <i>Temperature [C]</i> | - | 100 | 27 | -40 |
| Loop Gain [dB] | >70 | 63.8* | 76.2 | 76.1 |
| Loop UGBW [MHz] | >80 | 109 | 177 | 225 |
| Loop PM [Deg] | >60 | 62.8 | 92.6 | 97.5 |
| CMFB PM [Deg] | >60 | | | |
| CM Accuracy [mV] | <+/- 50 | | 2.9 | |
| Out Swing [V _{pk-pk-diff}] | >2 | | 1.496* | |
| Power [mW] | <10 | | 1.02 | |

This table is obviously not complete – yours should be complete with simulations results/plots to follow.

* Highlight your failures in the table.

2) Schematics

Very clearly show device sizes. Additional highlights (e.g. current in each branch) is always a good idea.

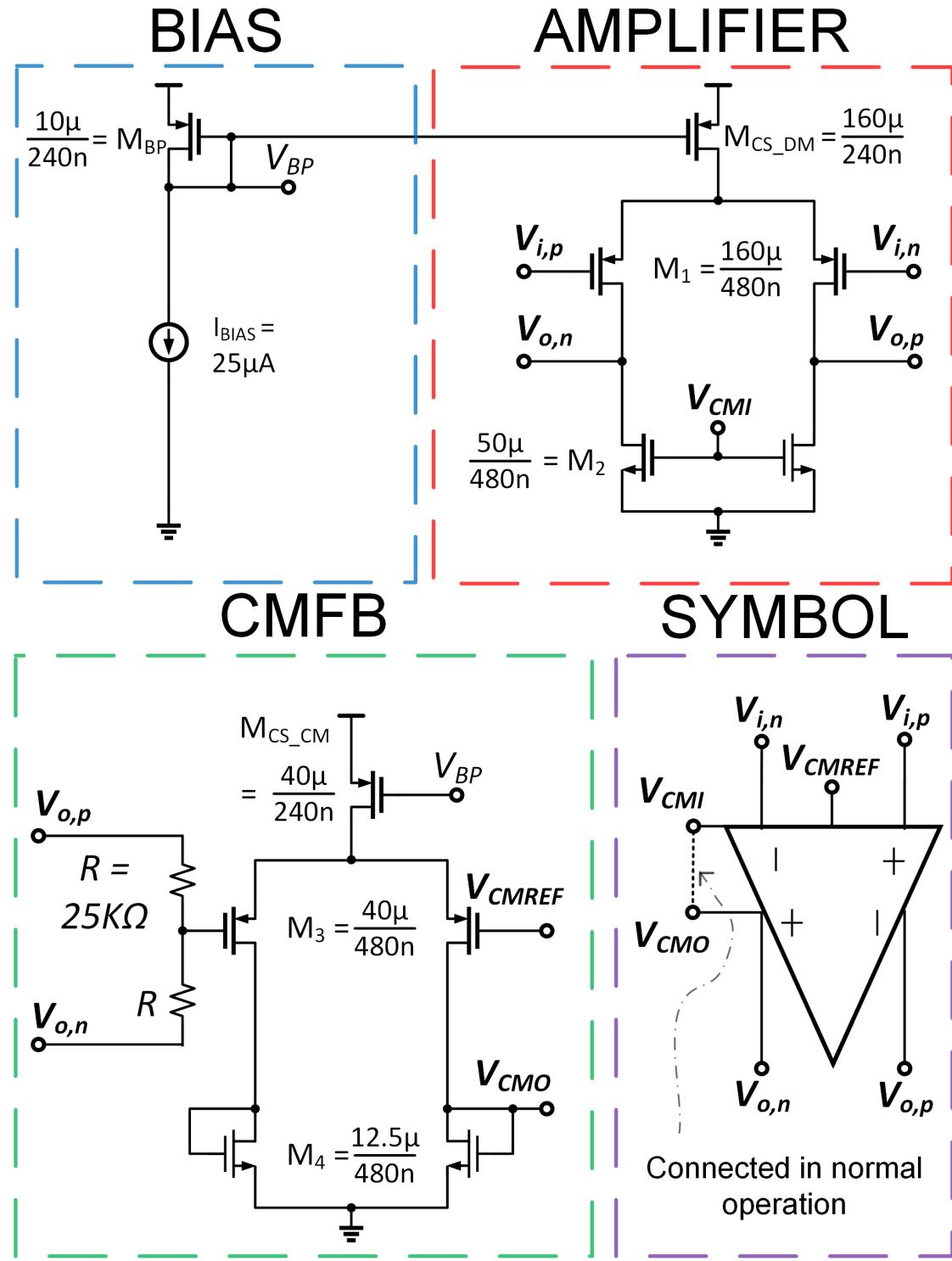


Figure 1: Example schematic that would never meet this projects requirements

3) Simulation Results

a. Differential Loop

Differential Loop [.ac sim]

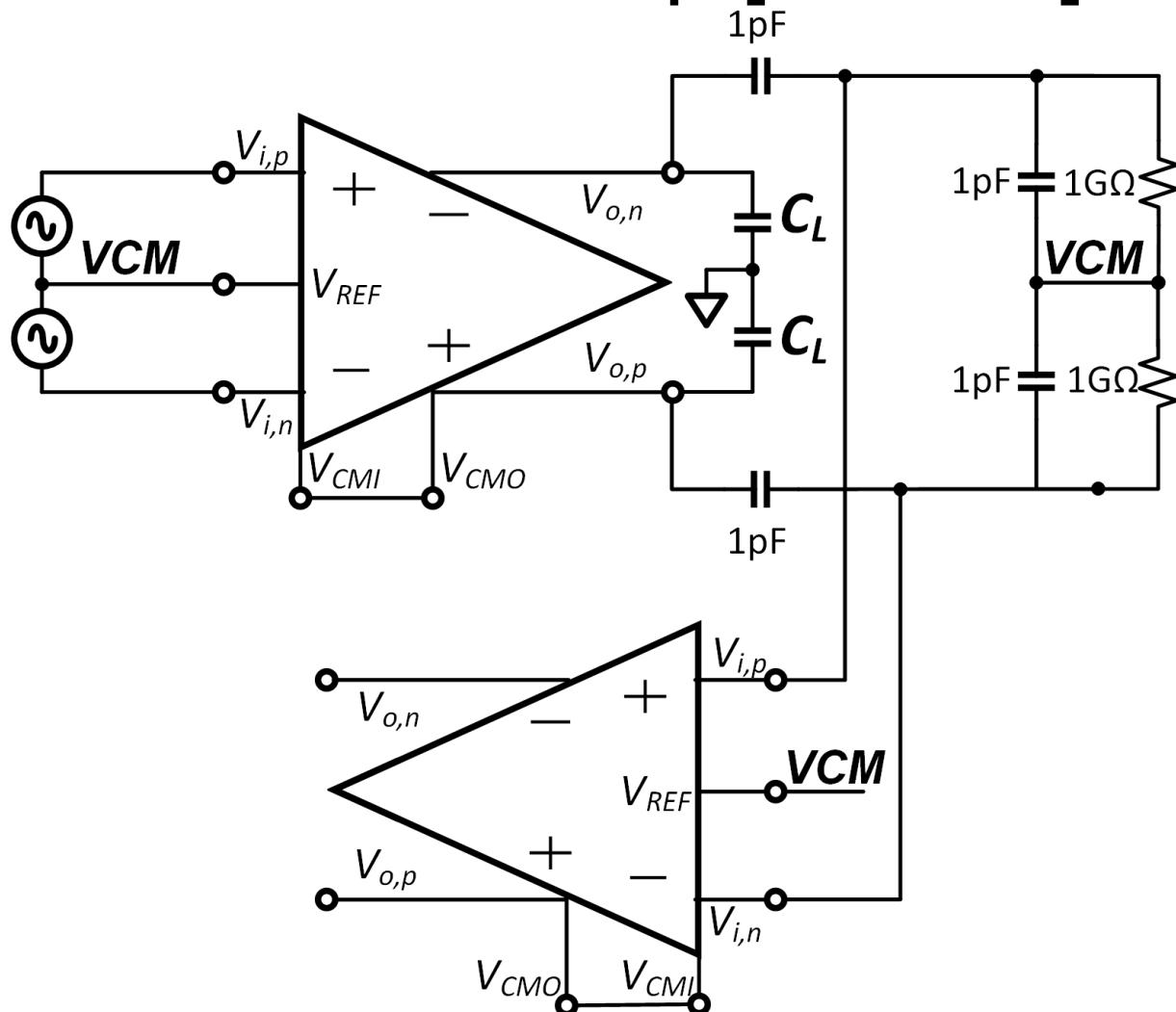


Figure 2: Differential Loop Testbench

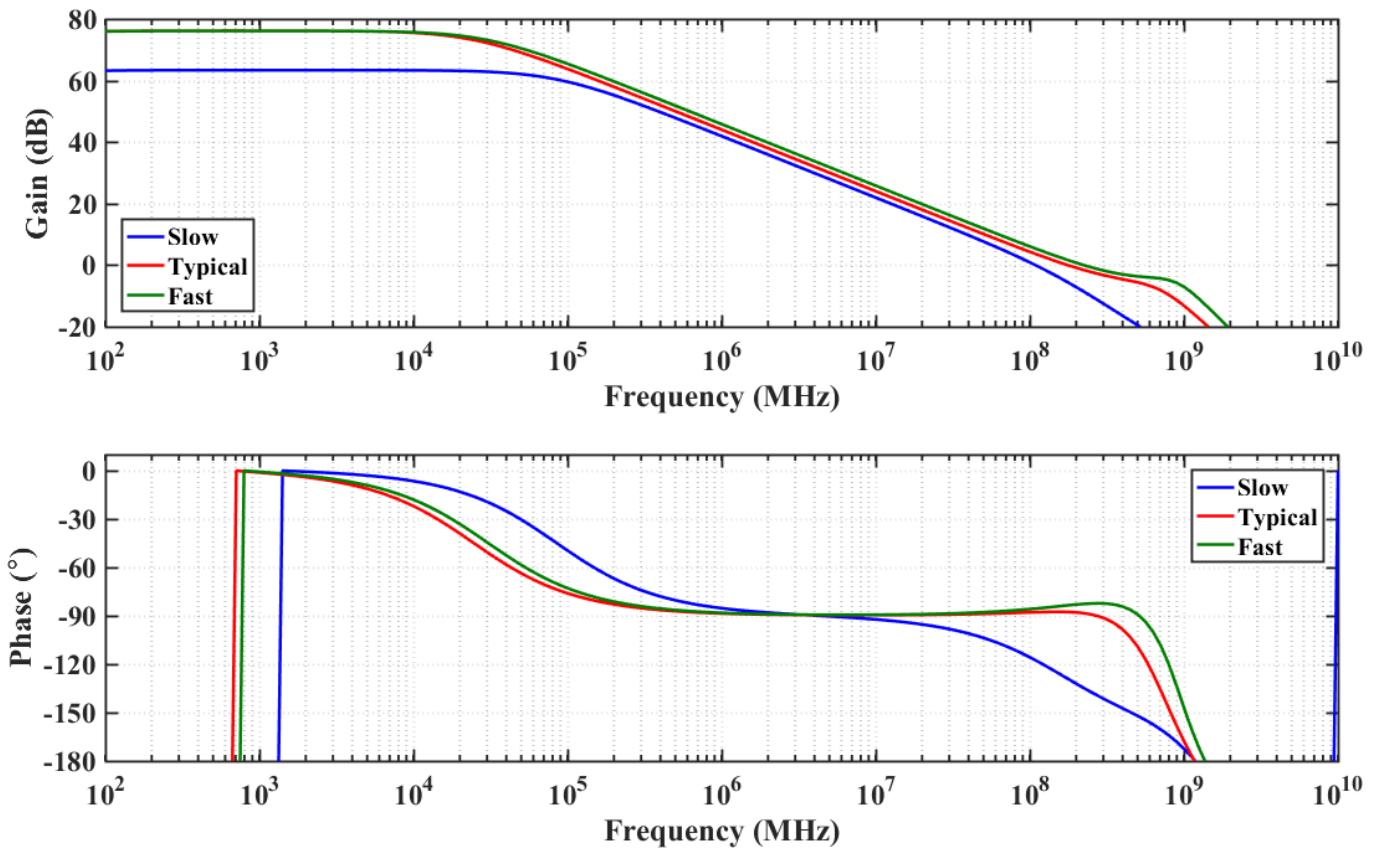


Figure 3: Bode-plot of loop-gain response of all three corners. Highlight the measuring points/values (not shown here) –hand written on the plot is acceptable.

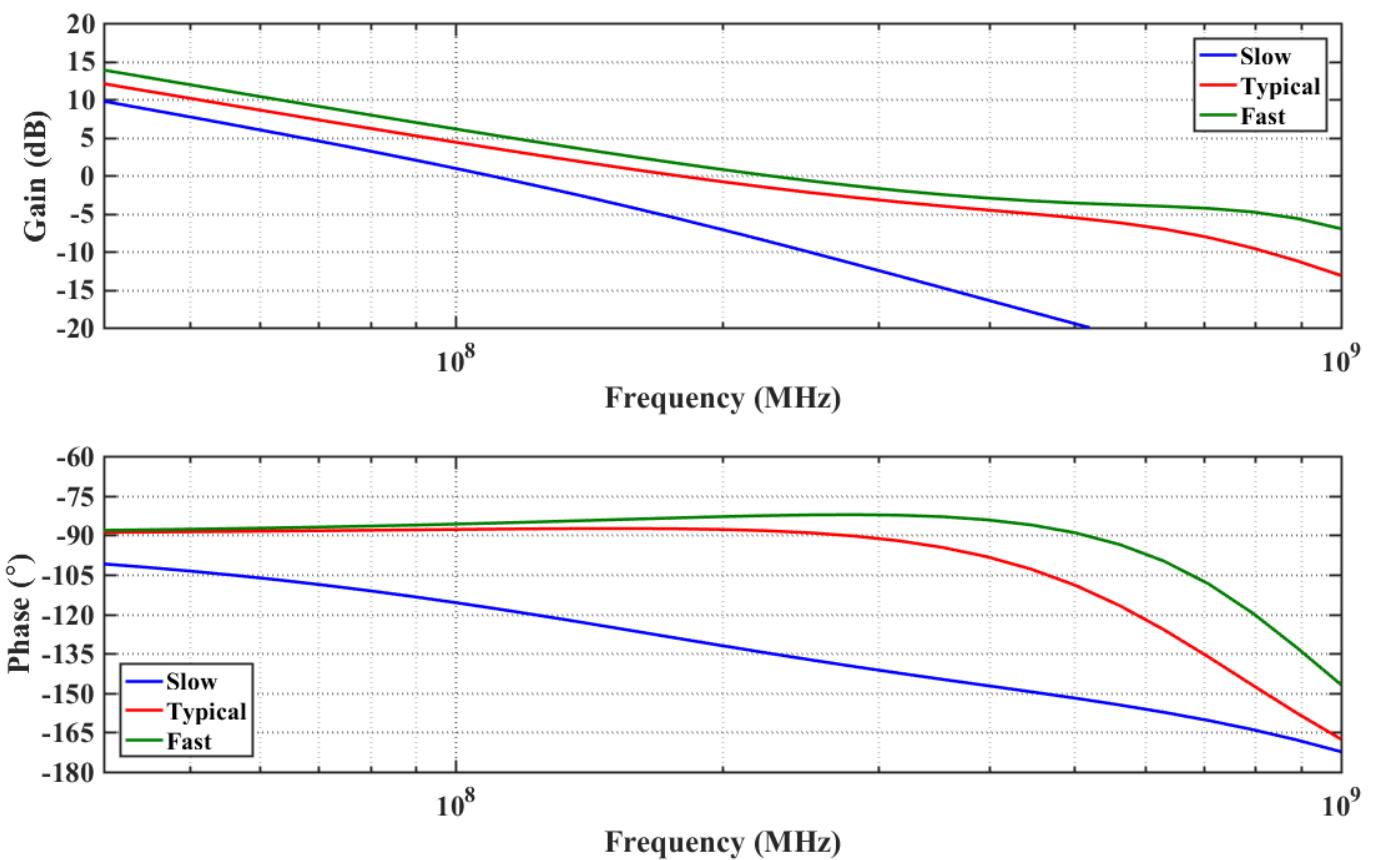


Figure 3: Bode-plot of loop-gain of all three corners zoomed in at UGBW

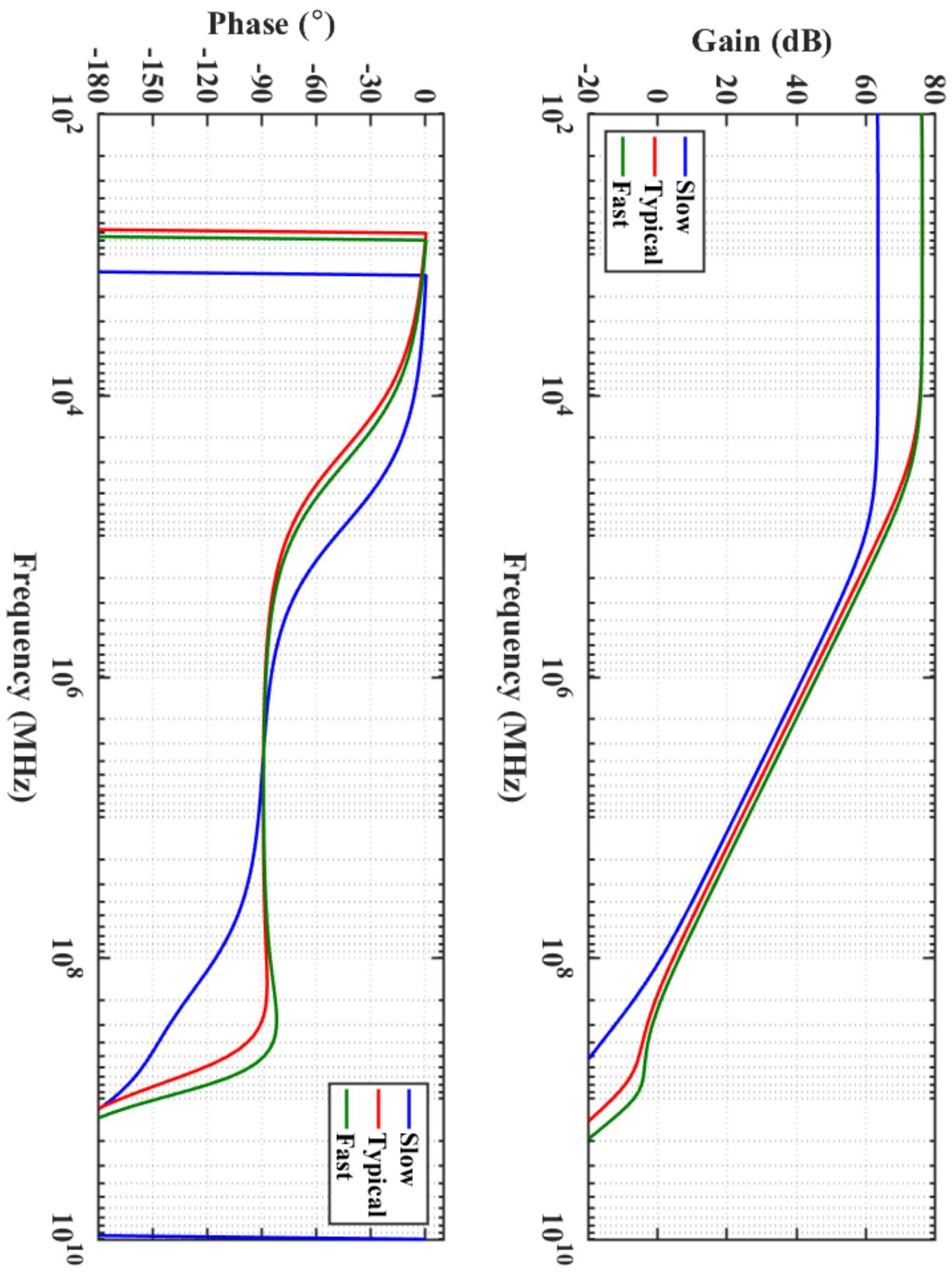


Figure 4: One graph landscape (this is fine)

b. CMFB Loop

CMFB Loop [.ac sim]

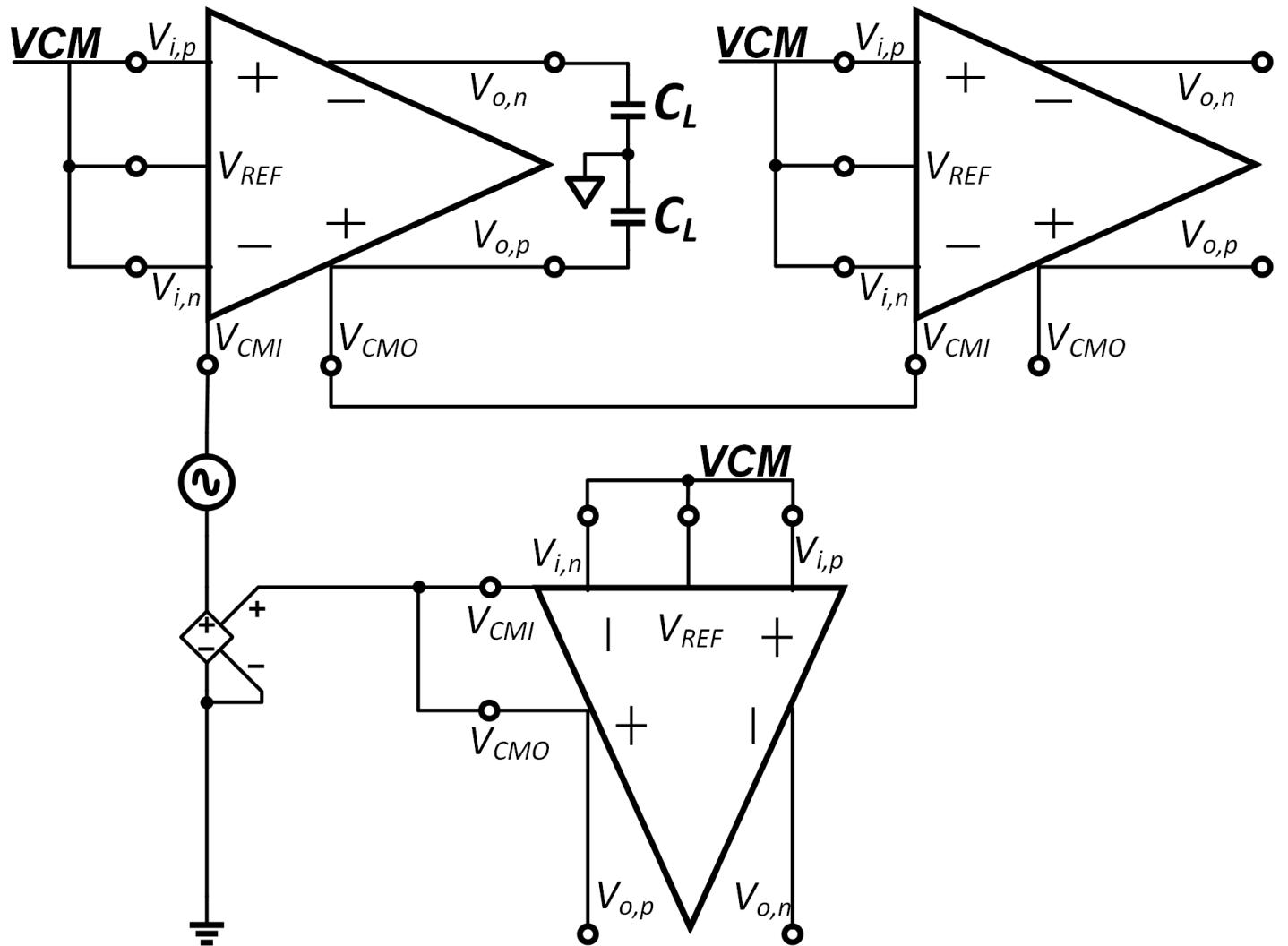


Figure 6: CMFB TestBench

See the plots in loop-gain section. They should look very similar

Figure 5: Bode-Plot of all three-cases

c. DC & Output Swing

Output Swing [.dc sim]

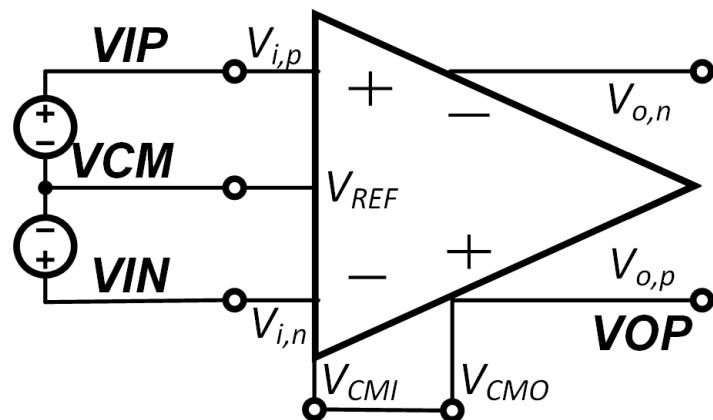
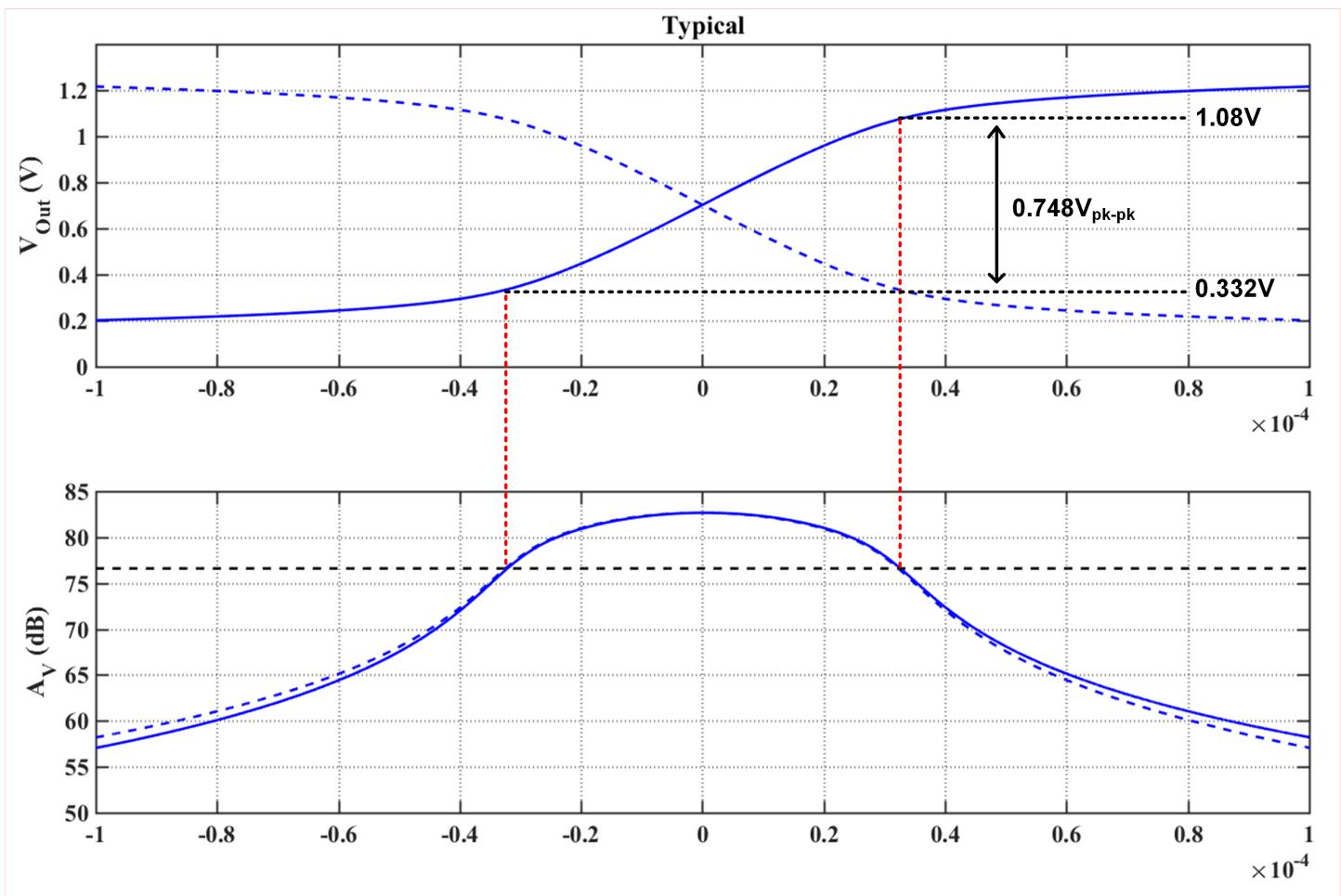


Figure 6: Output Swing TestBench



```
**info** dc convergence successful at GMINDC ramping method
***** HSPICE -- K-2015.06-SP1 linux64 (Aug 23 2015) *****
*****
```

```
***** operating point information tnom= 25.000 temp= 27.000 *****
***** operating point status is all simulation time is 0.
```

| node | =voltage | node | =voltage | node | =voltage |
|-------------|----------------|------------|----------------|------------|----------------|
| +0:vcm | = 700.0000000m | 0:vcm1 | = 750.0000000m | 0:vdda | = 1.4000000 |
| +0:vip | = 700.0000000m | 0:vip | = 700.0000000m | 0:von | = 702.9065028m |
| +0:vop | = 702.9065037m | 1:a1 | = 400.1541588m | 1:a2 | = 400.1541588m |
| +1:a3 | = 1.1519851 | 1:a4 | = 1.1519851 | 1:a5 | = 546.0573191m |
| +1:a6 | = 546.0573191m | 1:a7 | = 979.0359314m | 1:a8 | = 979.0359314m |
| +1:b0 | = 1.1764564 | 1:b1 | = 1.1699937 | 1:b2 | = 189.1653095m |
| +1:b3 | = 138.9689039m | 1:cm_1 | = 752.1678462m | 1:cm_2 | = 702.9065032m |
| +1:cmfb | = 990.1394565m | 1:cmfb_2 | = 932.7930331m | 1:i_in_p | =-236.7281642m |
| +1:vbn_ld | = 496.2612327m | 1:vbn_ld_1 | = 543.7023860m | 1:vbn_tel | = 890.3649403m |
| +1:vbn_tel | = 1.1215964 | 1:vbp_ld | = 987.9716103m | 1:vbp_ld_1 | = 929.8865299m |
| +1:vbp_ld_2 | = 929.8865299m | 1:vbp_ld_b | = 987.9716103m | 1:vbp_2d | = 625.7467995m |
| +1:vbp_3d | = 401.7603535m | 1:vcmr | = 700.0000000m | 1:vdaf | = 187.0635707m |
| +1:vgi | = 186.0866671m | 1:vgi_2 | = 187.0635707m | 1:vo_n_bf | = 702.9065028m |
| +1:vo_p_bf | = 702.9065037m | 1:vx_n | = 752.1678461m | 1:vx_n_bf | = 752.1678461m |
| +1:vx_p | = 752.1678462m | 1:vx_p_bf | = 752.1678462m | | |

```
**** voltage sources
```

| subckt | 0:vis3 | 0:vis4 | 0:vis7 | 0:vis9 |
|---------|---------------|--------|--------------|--------------|
| element | 0:vis3 | | | |
| volts | 1.4000000 | 0. | 700.0000000m | 750.0000000m |
| current | -727.3308145u | 0. | 0. | 0. |
| power | 1.0182631m | 0. | 0. | 0. |

| subckt | xil | xil | 0:vis7 | 0:vis9 |
|---------|--------------|--------------|--------|--------|
| element | 1:vis18 | 1:vis19 | | |
| volts | 700.0000000m | 0. | | |
| current | 0. | 218.4325085u | | |
| power | 0. | 0. | | |

```
total voltage source power dissipation= 1.0182631m watts
```

Figure 8: CM Accuracy and Power Consumption Screenshot.

Make sure the temperature and supply voltages match up with the corner you are highlighting (blue arrow).

4) Layout

Report whether or not you think you passed LVS and DRC. TA will check your database. Include a picture of your layout with the report (no black background).

DO NOT USE BLACK BACKGROUND SCREENSHOTS. INVERT YOUR COLORS AT LEAST! This important point applies to any/all layout, schematics, plots...

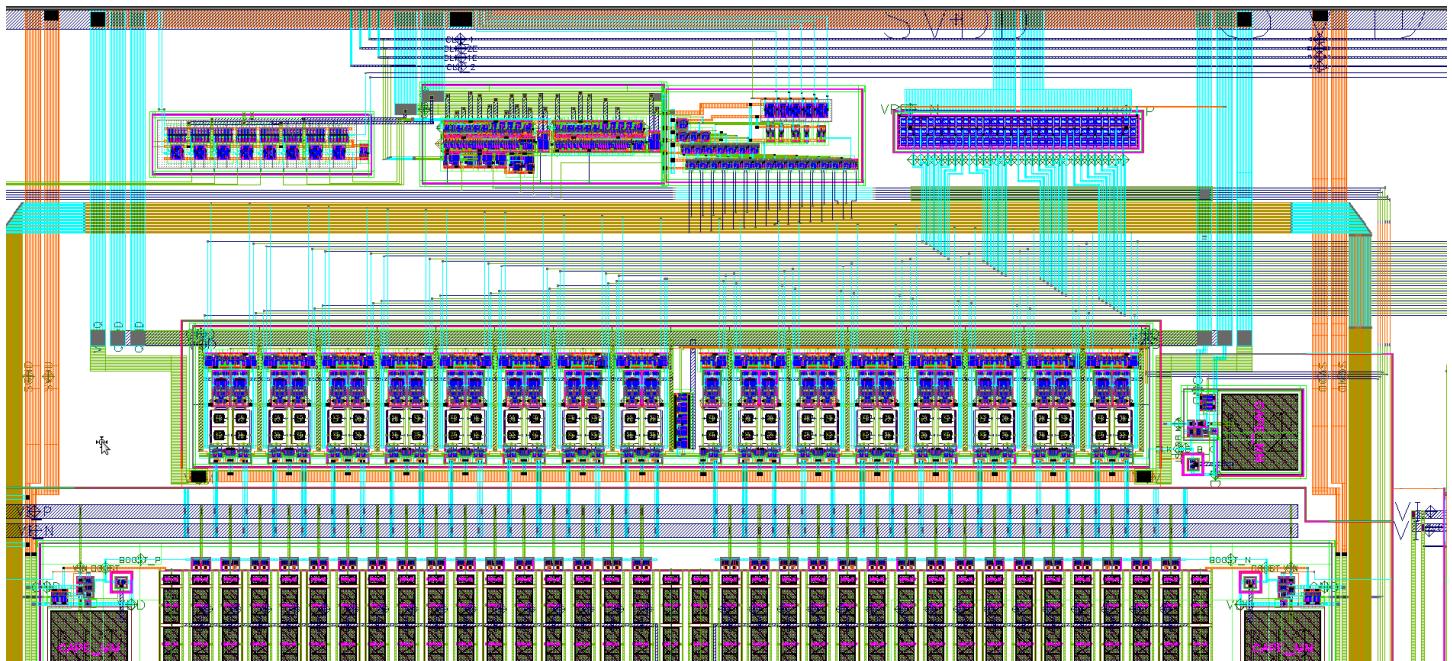


Figure 9: Layout Pics

5) ECE 523 Extras

There should be a section for the additional 523 project if you are a grad student. Follow the guidelines for the project.