Fast Opamp-Free Delta Sigma Modulator

by

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This thesis is dedicated in loving memory of my father Elias A Thomas.

FAST OPAMP-FREE DELTA SIGMA MODULATOR

1. INTRODUCTION

Switched capacitor (SC) circuits are commonly used in integrated circuit (IC) design due to their efficient use of die space, and the ability to accurately construct them on chip. A switched capacitor can be used to realize a large on-chip resistor, saving die area. SC circuit characteristics are determined by ratios of capacitor values as opposed to absolute component values, making their accuracy less suseptible to component variation and mismatch than other analog IC circuit techniques. Therefore, very accurate time constants can be realized. Some examples of SC circuits are precision filters and data converters [5].

There is an increasing need to operate SC circuits at higher speeds. One reason for this need is the emergence of the World Wide Web and other Internet technologies in the last decade. These new technologies have increased the demand for high bandwidth components and systems. One answer for delivering increased bandwidth is Digital Subscriber Line technologies (xDSL), offering data transfer rates that are hundreds of times faster than a standard computer modem. Analog circuits are required for these systems to convert the data stream from analog to digital as information is passed through the transmission channel.

1.1 Problem Definition

The operational amplifier (opamp) is a common analog building block of SC circuits. The typical opamp uses multiple stages to generate high gain. The stages create poles that cause the overall frequency response of the opamp to have a multiple-pole roll-off at higher frequencies. The opamp can become unstable if the additional poles cause the phase margin to be too small at the desired operating frequency.

In SC circuits opamps are typically internally compensated to improve their closed-loop stability. The internal compensation network consists of a capacitor and resistor sized to create a dominant pole in the opamp's frequency response. This pole is placed at a frequency low enough to give the overall opamp response a single-pole roll-off, and thus increasing phase margin. However, an undesirable side effect of internal compensation is that it limits the speed of the opamp.

A typical design rule for SC circuits is that the opamp unity-gain bandwidth (UGBW) should be five times larger than the clock frequency to allow proper settling behavior within each clock phase [6]. Because the opamp bandwidth is constrained by its internal compensation, it follows that the maximum operating frequency for the SC circuit they are used in is also constrained.

1.2 Statement of Purpose

The objective of this work is to explore the feasibility of the replacing internally compensated opamps with a faster gain block in SC circuits. In particular, inverter amplifiers are analyzed for their suitability as SC gain stages.

A couple significant trade-offs can occur when replacing opamps with faster, simpler gain stages. First, the gain of these structures will be lower than a typical op-amp, which is constructed with multiple gain stages to increase the overall gain. Second, rejection of common-mode errors (e.g., power supply noise, signal-dependent charge injection, and clock feedthrough) is also reduced. Therefore, this thesis will also explain circuit and system design techniques to compensate for the trade-offs to achieve performance acceptable for high-speed SC circuits.

1.3 Thesis Outline

The organization of the remaining parts of this thesis is as follows:

- Section 2 briefly describes different analog-to-digital (A/D) converter architectures, reviews fundamental $\Delta\Sigma$ concepts and terminology and defines important $\Delta\Sigma$ modulator performance metrics.
- Section 3 provides details about potential circuit design techniques studied for use in opamp-free SC circuits. It describes the amplifier structure chosen for this thesis work.
- Section 4 describes the system-level and circuit-level implementation of a opamp-free $\Delta\Sigma$ modulator designed for a clock frequency of 500MHz. System-level simulation results are presented.
- Section 5 Transistor-level simulation results for the $\Delta\Sigma$ modulator designed in Section 4 are presented.
- Section 6 outlines a preliminary floorplan for layout of the $\Delta\Sigma$ modulator designed in Section 4. Comments about layout specifics are also provided.
- Section 7 presents conclusions about the opamp-free $\Delta\Sigma$ modulator designed in this thesis. Conclusions and concerns about inverter-based SC circuit design are also provided. Lastly, suggestions for future work in inverter-based SC circuits are given.

2. REVIEW OF LITERATURE

Data converters comprise a major portion of the analog circuits used in signal processing IC's. They are found at locations in the signal chain where the signal is converted from the analog domain to digital domain, and vice versa.

Because this work focuses on the design of a Delta-Sigma ($\Delta\Sigma$) modulator that would be used in an analog-to-digital (A/D) converter, the following section will provide a survey of common A/D architectures, some fundamental $\Delta\Sigma$ A/D concepts, common performance metrics, and some current trends in $\Delta\Sigma$ A/D design.

2.1 Overview of Common A/D Architectures

Many A/D conversion schemes have been proposed and implemented. The ideal A/D converter would be fast and accurate, but unfortunately these performance metrics are contradictive. Thus, the topic of A/D conversion encompasses many designs that offer some compromise between these two qualities. Table 2.1 presented in [7] compares many of the common A/D converter architectures on the basis of accuracy and speed. As noted in the table $\Delta\Sigma$ converters are typically classified as low-to-medium speed, high accuracy data converters.

To relate this information to the work presented in this thesis, the $\Delta\Sigma$ modulator designed in the thesis could be used in a high speed, medium accuracy A/D converter. Thus, the proposed design will broaden the current definition of $\Delta\Sigma$ A/D converters, and allow them to compete with some of the higher speed architectures.

TABLE 2.1: Survey of A/D Converter Architectures.

Low-to-Medium Speed, High Accuracy	***Medium Speed, Medium Accuracy***	***High speed, Low-to-Medium Accuracy***
Integrating	Successive Approximation	Flash
$\Delta\Sigma$	Algorithmic	Two-step
–	–	Interpolating
–	–	Folding
–	–	Pipelined
–	–	Time-Interleaved

2.2 $\Delta\Sigma$ Modulation

$\Delta\Sigma$ A/D converters use oversampling of the input signal and noise shaping to achieve their performance. Oversampling implies that the input signal is captured at a rate higher than the Nyquist rate. A common parameter used for $\Delta\Sigma$ converters is the oversampling ratio (OSR), defined as:

$$OSR = \frac{f_s}{f_{nyq}} \tag{2.1}$$

where f_s is the sampling frequency and f_{nyq} is the Nyquist frequency, defined as a frequency twice the highest frequency component of the input. By oversampling the input signal, the quantization error which is the artifact of the conversion from analog to digital, is spread over a larger range of frequencies. The result is a 3dB increase in the dynamic range every time the sampling frequency is doubled [7].

The other property common to $\Delta\Sigma$ converters is noise-shaping, accomplished with the $\Delta\Sigma$ modulator. Figure 2.1 illustrates a linearized z-domain model of a $\Delta\Sigma$ modulator. The model assumes that the quantization error can be modeled as additive white noise, with properties that that it is independent of the input,

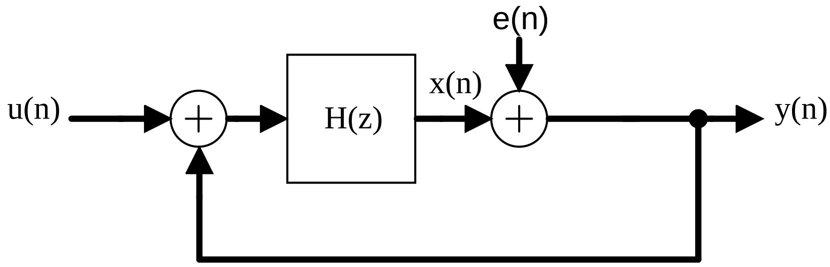


FIGURE 2.1: Linear model of a $\Delta\Sigma$ modulator.

uniformly distributed in $[-\Delta/2, \Delta/2]$ where Δ is the step size of the quantizer, and has a flat ("white") power spectral density. Thus, this quantization error or "noise", denoted $e[n]$, can be decoupled from the input and represented as an additional input to the system.

Using the approximation of the quantization noise, the output of the modulator $Y(z)$ can be expressed as

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.2}$$

where $STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer function. Solving Equation (2.2) for the $STF(z)$ and $NTF(z)$, and expressing them in terms of the $H(z)$ yields

$$STF(z) = \left.\frac{Y(z)}{U(z)}\right|_{E(z)\equiv 0} = \frac{H(z)}{1 + H(z)} \tag{2.3}$$

and

$$NTF(z) = \left.\frac{Y(z)}{E(z)}\right|_{U(z)\equiv 0} = \frac{1}{1 + H(z)} \tag{2.4}$$

Equation (2.4) illustrates that if $H(z)$ is a lowpass function, the quantization noise is shaped by a high-pass type function. By proper design of the modulator, most of the quantization noise can be removed from the signal band. Also, by increasing the order of the loop filter $H(z)$, more of the quantization noise is removed from the signal band.

2.3 ΔΣ Modulator Performance Metrics

The performance of a ΔΣ modulator is commonly evaluated using the metrics of resolution, signal-to-noise-and-distortion ratio (SNDR), input signal bandwidth, and power consumption. This section will briefly define and describe these parameters.

The resolution, often expressed in terms of "bits" (binary digits), is directly related to the the signal-to-noise ratio (SNR) of the modulator. Given a full-scale sine wave input test signal the effective number of bits (ENOB) of the modulator can be expressed as [8]:

$$ENOB = \frac{SNR[dB] - 1.76dB}{6.02dB}[bits] \tag{2.5}$$

The resolution and input signal bandwidth, described next, are conflicting design parameters. For the fast opamp-free ΔΣ modulator designed in Section 4 of this thesis, a moderate resolution design goal was selected. The signal-to-noise-and-distortion ratio (SNDR) provides more realistic measure of modulator resolution because it includes any degradation of performance due to harmonic distortion.

The sampling frequency (or clock rate) and OSR are defined by input signal bandwidth desired for the modulator design. A large input signal bandwidth for a

$\Delta\Sigma$ modulator design translates into minimum OSR, high sampling frequency, or both. Low values of OSR, typically defined as OSR less than 32, normally require multi-bit uniform quantizers in the $\Delta\Sigma$ modulator. However, unlike a single-bit quantizer that has inherent linearity, care must be taken to ensure linearity of a multibit quantizer. A high clock frequency requires fast analog components; a mode of operation where opamp-free SC circuits should excel.

In a $\Delta\Sigma$ modulator design based on SC circuits power is consumed primarily in charging capacitors, whose size is constrained by the desired resolution of the modulator. Because most nonidealities are suppressed by the feedback nature of the $\Delta\Sigma$ loop, the first integrator in the loop filter is the most critical component in the loop. Therefore, the first integrator's kT/C noise, the most significant noise component in SC circuits and controlled by capacitor sizing, usually determines to a large extent the overall power consumption of the modulator [9].

2.4 Review of Current $\Delta\Sigma$ A/D Research

Two major trends dominate $\Delta\Sigma$ A/D converter research. The emphasis of the first trend is on increased resolution. The improved resolution comes from using digital correction techniques to overcome problems in the analog building blocks. Some examples of the these techniques are mismatching shaping and adaptive correction methods [10]. The emphasis of the second trend is wider signal bandwidth, with the intended use of the converters in xDSL, video, or RF baseband applications Some examples are [11], [4], and [12].

2.5 Summary of Review

This review has presented an overview of A/D converter architectures and a brief introduction to $\Delta\Sigma$ modulators. It also presented some performance metrics commonly used to compare $\Delta\Sigma$ designs. The performance parameters from this section will be used to evaluate the modulator design described in this work.

3. OPAMP-FREE SC CIRCUIT DESIGN TECHNIQUES

The main focus for this research was to explore inverter amplifier structures that could be used to replace the internally-compensated opamps commonly used in SC circuits. Some of the inverter configurations explored will be briefly described, and their advantages and disadvantages will be summarized. Lastly, the inverter amplifier configuration chosen as the best solution for fast SC circuits will be presented, and a design intended for use in the fast opamp-free $\Delta\Sigma$ modulator described in Section 4 will be characterized.

Replacing the circuit complexity of a typical opamp for the simplicity of a fast, inverter-based gain is not without sacrifice. The shortcomings of the inverter-based gain must be compensated with other circuit design techniques. The circuit design techniques explored in this research will be summarized, and those chosen for use in the final design will be explained in detail.

Lastly, because the SC integrator is a common circuit block in the design of SC filters and data converters, it was a useful circuit to test the use of opamp-free design techniques. A proposed inverter-based SC integrator design is explained and characterized.

3.1 Fast Gain Stage Tradeoffs

The first major tradeoff when replacing the opamp in SC circuits with a faster gain stage is lower gain. Typical opamps use internal compensation to ensure the stability of the opamps in closed-loop applications, such as SC circuits. This internal compensation is required, because a common opamp design uses a multistage architecture to boost the overall gain. Opamp designs, such as telescopic or folded cascode architectures, exist that do not have internal compensation and thus have improved high frequency response. However, they typically sacrifice output swing to achieve this frequency response.

The second major tradeoff when replacing the opamp in SC circuits with a faster gain stage is loss of the common mode noise and power supply rejection. Once again, compensation techniques can be applied, and some are also discussed in the next section.

3.2 Fast Gain Stage Compensation Techniques

Techniques explored in this research to compensate for tradeoffs described in Section 3.1 will now be explained.

3.2.1 Gain Improvement

Some circuit design techniques explored to improve gain were cascoding and regulated cascoding, or gain-boosting. Cascoding of the current source transistors increases the output impedance of the sources which act as active loads to a typical IC amplifier. Since the gain is directly proportional to the output impedance, the gain of the amplifier is increased. Simple cascoding of the amplifying transistor has the benefit of improving the frequency response because the drain-to-gate capacitance of the output transistor is no longer amplified by a large gain (i.e., Miller effect). Regulated cascoding is an effective gain-boosting scheme [13] that was also explored. However the technique introduces doublets in the amplifier frequency response that are a concern for high frequency operation and thus was not used.

Another technique explored for improving the gain of the opamp-free SC circuits was correlated double sampling (CDS). CDS enhances the virtual ground of a gain stage by using a capacitor to cancel the error voltage at the virtual ground, emulating the effect of a larger gain on the virtual ground. As given in [14], the DC gain of a standard SC amplifier is given as

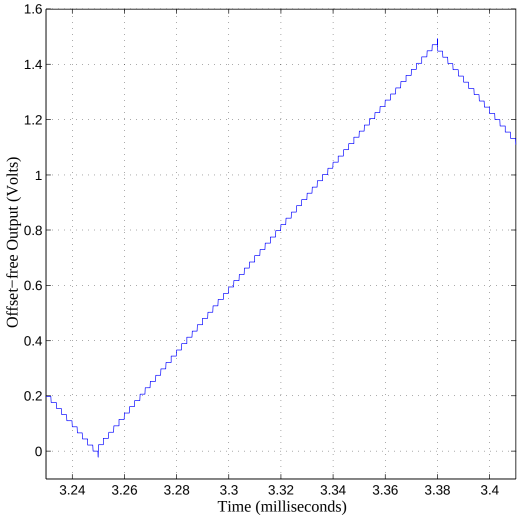
$$A_v = \frac{\frac{-C_1}{C_2}}{\left(1 + \frac{1+\frac{-C_1}{C_2}}{A}\right)} \tag{3.1}$$

where A is the finite gain of the opamp in SC amplifier. In contrast, a SC amplifier incorporating CDS has a DC gain given by:

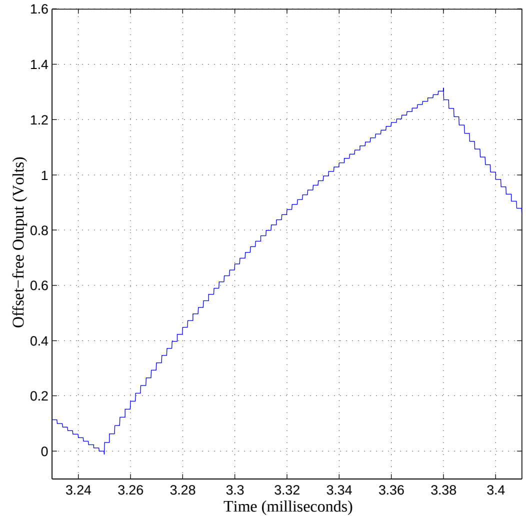
$$A_v = \frac{\frac{-C_1}{C_2}}{\left(1 + \frac{1+\frac{-C_1}{C_2}}{A^2}\right)} \tag{3.2}$$

Thus the effective gain is close to the square of the DC gain (doubles in deciBel units).

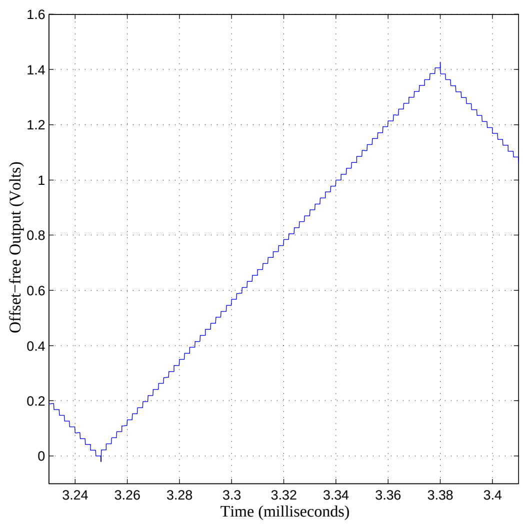
In SC integrators, CDS has the property of improving the effective gain of the integrator, similar to the effect described above for SC amplifiers. As a further example, the three plots in Figure 3.1 illustrate a SWITCAP simulation to test the gain improvement afforded by CDS. The input signal is a 90mV peak-to-peak square wave in each simulation. Figure 3.1(a) shows the simulated response for an integrator with opamp DC gain of 60dB, Figure 3.1(b) shows the simulated response for an integrator without CDS and opamp DC gain of 30dB, and Figure 3.1(c) shows the simulated response for an integrator with CDS and opamp DC gain of 30dB.



(a) Integrator without CDS and opamp DC gain = 60dB.



(b) Integrator without CDS and opamp DC gain = 30dB.



(c) Integrator with CDS and opamp DC gain = 30dB.

FIGURE 3.1: Example of the effective DC gain improvement of a SC integrator using CDS.

The plots illustrate that the integrator with CDS and opamp DC gain of 30dB has very similar output response to the integrator with opamp DC gain of 60dB. The integrator without CDS and opamp DC gain of 30dB shows a nonlinear response to the input signal.

3.2.2 Common-Mode Noise and Power Supply Rejection Improvement

Besides effective gain enhancement, CDS also has the added benefits of reducing DC input voltage errors and 1/f noise in SC circuits [7], similar to dynamic biasing (mentioned in Section 3.3.2). The most significant technique explored for improving common-mode and power supply rejection is using a pseudo-differential structure. This technique is especially useful in this application because it can be applied to combine two single-ended structures to form the pseudo-differential structure. As presented in [5], pseudo-differential structures offer nearly the same performance as fully-differential ones. Output swing should also be nearly doubled over that of single-ended structures.

Pseudo-differential structures do require some type of common-mode feedback (CMFB) to keep the output levels in the linear operating range. This CMFB can be added internally to the amplifiers, or implemented by using a pseudo-differential method [15]. The pseudo-differential method was chosen for the SC integrator design described later in Section 3.4.

3.3 Amplifier Design

The inverter architectures evaluated in this research were the CMOS inverter amplifier and NMOS inverter (common-source) amplifier. The following section describes and evaluates the amplifiers for their application in fast SC circuits.

3.3.1 The CMOS Inverter Amplifier

The merits of the simple CMOS inverter as an amplifier have been explained in many publications including [16]. In comparison to other amplifier structures, the CMOS inverter has the highest transconductance for a given bias current [17]. In the amplifying region of operation the PMOS transistor is also used in processing the input signal and thus the effective transconductance of the inverter amplifier is the sum of the transconductance of the two transistors. The amplifier also exhibits very high slew rate due to the single-stage structure. However, a disadvantage of this amplifier is the difficulty of properly maintaining the inverter in its amplifying region, making it sensitive to process and power supply variation.

3.3.2 Dynamic Biasing Of The CMOS Inverter Amplifier

The first amplifier design explored was using the CMOS inverter amplifier with dynamic biasing. Dynamic biasing was introduced to solve problem of properly biasing the amplifier in the its high-gain region of operation, given process and power supply variation. The technique, in essence, uses capacitors to store a voltage required to bias the transistors in the CMOS inverter in their active region of operation. The useful side-effect of dynamic biasing is that the $1/f$ noise transistor noise is reduced by the averaging action of the voltage storage capacitor.

Dynamic biasing of a CMOS inverter amplifier is illustrated in Figure 3.2 [18]. In clock phase ϕ_1, switches S_{in2}, S_1, and S_4 are closed and the transistors in the amplifier are biased. In clock phase ϕ_2, switches S_{in} and S_3 are closed, applying the input signal to the amplifier and the amplified result to the capacitive load (the type of loading common in SC circuits).

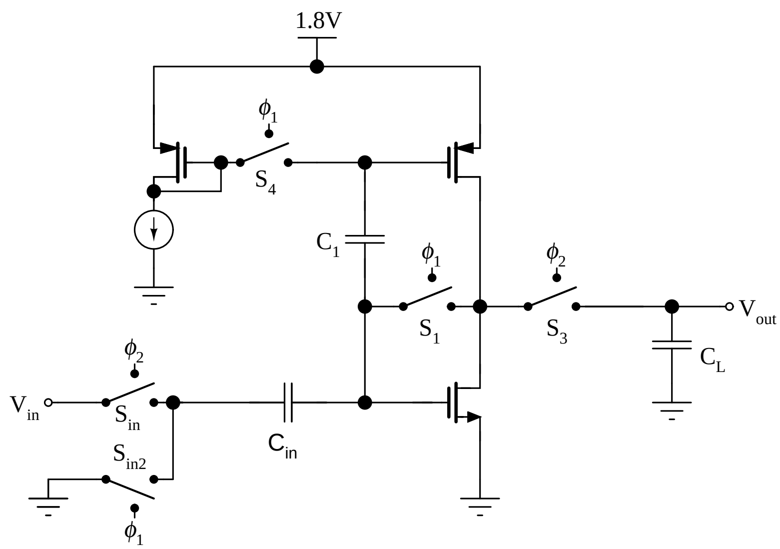


FIGURE 3.2: CMOS inverter amplifier with dynamic bias.

A problem with using the dynamically-biased CMOS inverter amplifier shown in Figure 3.2 as a fast gain stage for opamp-free circuits was that it exhibits low gain unless large transistors are used. Therefore, a cascode transistor was added for the p-channel transistor (current mirror) to boost the gain. Cascoding did improve the gain of this amplifier, however the input capacitance of the amplifier was large due to the addition of the gate-to-source capacitance of the p-channel transistor.

The large input capacitance inhibited the high-frequency operation of the circuit. Also, the correlated double sampling (CDS) technique described in Section 3.2 has similar advantages as dynamic biasing.

3.3.3 Inverter Amplifier With Active Load

The inverter amplifier with active load was also evaluated in this research and eventually chosen as the inverter-based fast opamp-free gain stage. In this configuration of the inverter amplifier the input signal is applied to the n-channel transistor device only and the p-channel transistor serves as an active load. The gain of the inverter amplifier with active load was improved by cascoding the current mirror transistor (PMOS) and thereby increasing the output impedance. Frequency response was improved by cascoding the amplifying transistor (NMOS). This design is shown in Figure 3.3. The cascode transistors increased the requirements for the bias voltage circuit from two bias voltages to four. The bias circuit was designed for wide-swing operation [7] to allow maximum output voltage swing. The bias circuit is shown in Figure 3.4.

An actively-loaded inverter amplifier was designed for use as the gain stage of the first integrator of the fast opamp-free $\Delta\Sigma$ modulator described in Section 4 of this thesis. Because the first integrator has to drive the largest capacitance values in the modulator (the first integrator is the most critical component in the modulator, as explained in Section 4) and the design goal was a clock frequency of 500 MHz, the bias current and transistor widths had to be large. Also note that minimum transistor channel length was used for all devices to improve the frequency response and to keep the transistor sizes from becoming excessively large.

Table 3.1 show the performance results from simulation for the amplifier de-

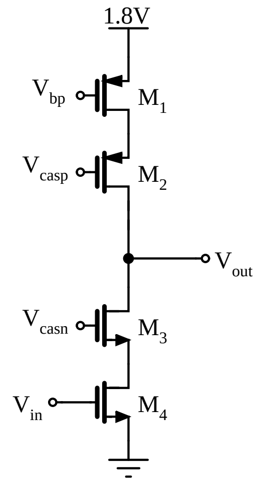


FIGURE 3.3: Proposed inverter-based fast gain stage.

signed for the first integrator. The amplifier was simulated using SpectreS to verify its performance, with a 1 pF load capacitance (expected load). Performance of the design was also confirmed with fast and slow device models. Note that the loop gain of the amplifier was measured, with the amp loaded with a 1 pF capacitance, to more accurately model its use in SC circuits.

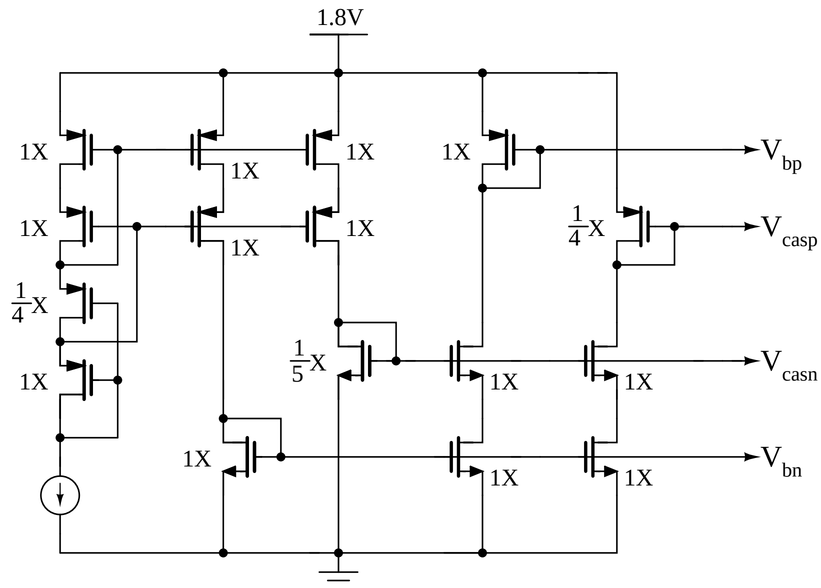


FIGURE 3.4: Bias circuit for the proposed fast inverter-based gain stage.

TABLE 3.1: Summary of fast inverter amplifier design.

Parameter	**SpectreS**
I_{BIAS}	6.8 mA
Loop Gain (dB)	32.4
Loop UGBW (GHz)	1.12
Loop Gain Phase Margin	84.4°
Output Swing (V)	1.0
Power Consumption (mW)	12.24
$(W/L)_{M1}$ (μm/μm)	1749/0.18
$(W/L)_{M2}$ (μm/μm)	1749/0.18
$(W/L)_{M3}$ (μm/μm)	915/0.18
$(W/L)_{M4}$ (μm/μm)	915/0.18
$(C_{gs})_{M4}$ measured	0.922pF

3.4 A Pseudo-differential, Inverter-based, Fast SC Integrator

3.4.1 Design Description

Using a CDS-enhanced SC integrator circuit [19], a SC integrator was designed and simulated with the opamp replaced by the proposed fast gain stage. The integrator was also constructed as a pseudo-differential structure, and a pseudo-differential CMFB circuit similar to that presented in [15] was designed for the circuit. The complete design is shown in Figure 3.5 on page 21. Note that the polarized capacitors are used in the drawing to indicate the proper placement of the capacitor's bottom plate to minimize parasitic capacitance effects [7].

The circuit requires three clock phases. During clock phase ϕ_{1d}(and ϕ_{1dn}, the complement of ϕ_{1d} for the PMOS transistor in the CMOS switches S_1), the input signal is sampled, and this phase has a delayed falling edge to reduce signal-dependent charge injection errors. During clock phase ϕ_1, the output error voltage is stored in the CDS capacitor C_{ds}. In clock phase ϕ_2, the sampled input is integrated and the error voltage stored in the CDS capacitor is subtracted. Note that the value of C_{ds} is the same as $\mathrm{C}_{\mathrm{int}}$, the integrating capacitor.

The output common-mode voltage is set to 900mV, half of the power supply voltage to allow maximum output swing. This voltage is set by the pseudo-differential CMFB circuit made up of switches $\mathrm{S}_{\mathrm{cm1}}$ and $\mathrm{S}_{\mathrm{cm2}}$ and capacitors C_{m}. During clock phase ϕ_1 (and ϕ_{1n}, the complement of ϕ_1 for the PMOS transistor in the CMOS switches $\mathrm{S}_{\mathrm{cm1}}$), desired output common-mode voltage is stored on the C_{m} capacitors. During clock phase ϕ_2 (and ϕ_{2n}), the outputs are sampled and the average value is stored in the C_{m} capacitors and a correction charge is delivered to the integrating capacitors $\mathrm{C}_{\mathrm{int}}$. Note also that the input common-mode voltage can be set through switch S_2.

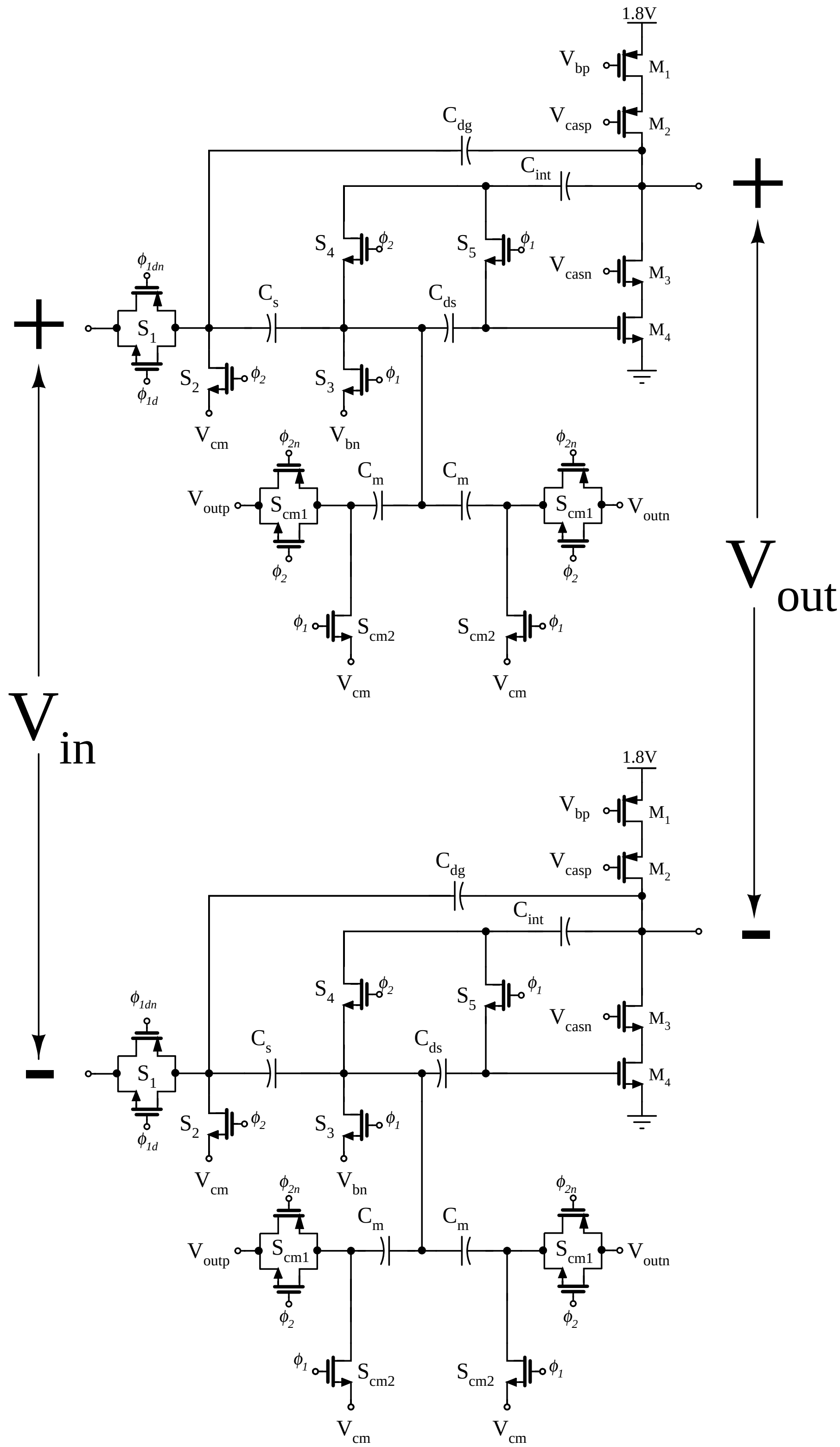


FIGURE 3.5: A pseudo-differential, inverter-based SC integrator.

3.4.2 SC Integrator Simulation Results

Figure 3.6 shows a simulated output spectrum of pseudo-differential, inverter-based SC integrator. The spectrum was calculated from a full-scale differential output from the integrator (i.e., 1V peak-to-peak), generated from a 98mV peak-to-peak, 1.9532MHz sinusoidal input.

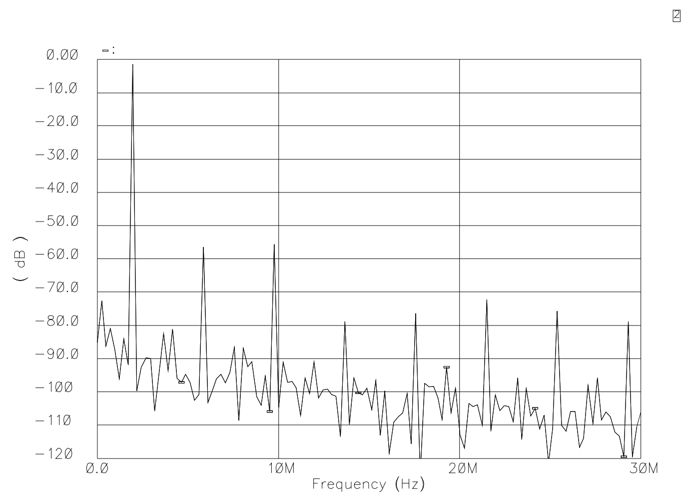


FIGURE 3.6: Output spectrum of the pseudo-differential, inverter-based SC integrator.

4. FAST OPAMP-FREE ΔΣ MODULATOR DESIGN

A fast ΔΣ modulator was chosen as a test vehicle for the proposed inverter-based SC circuits. In particular, inverter-based SC integrators are used in the design. The following sections will describe the design process for the modulator. The design was simulated using models for a 1.8V, 0.18μm CMOS process.

Section 4.1 outlines the chosen design goals for the modulator. Section 4.2 describes system-level considerations used to construct the ΔΣ modulator. Initial design considerations are presented, followed by a description of the selection of the modulator order and topology. Then, the coefficents selection methodology is described. Lastly, system-level simulations of the design are presented. Section 4.3 describes the circuit design of the ΔΣ modulator system components. These components include the opamp-free SC integrators, the 1-bit quantizer, the 1-bit DAC's, and the clock generator. Pertinent system-level simulation results are provided.

4.1 Design Goals

A "high" clock rate or frequency was the most important design goal to test the feasibility of inverter-based SC circuits. In mixed-signal CMOS circuit design, a typical definition of a "high" clock rate is one above 100MHz. Therefore, an aggressive clock rate of 500MHz was selected for the design described in this section. A moderate OSR of 64 was chosen, thereby fixing the signal bandwidth(BW) for the fast, op-amp free ΔΣ modulator to 3.90625MHz.

As mentioned in Section 2.1, a high operating frequency requires a sacrifice of accuracy. Therefore a medium resolution goal of 12-bit resolution was selected for this design. Table 4.1 summaries the chosen design goals.

TABLE 4.1: Summary of the design goals for the fast, opamp-free $\Delta\Sigma$ modulator.

Parameter	***Goal***
Operating Speed	500 MHz
Resolution	12 bits
Signal BW	3.90625MHz

4.2 System-Level Design

4.2.1 Topology Selection

Because the inverter-based circuits lack the linearity of a high gain opamp, a modulator topology tolerant of integrator non-linearity is desired. Such a topology was presented in [1] and is shown in Figure 4.1. With proper selection of gain coeficients of the integrators and feedforward paths, the integrators process very little of the input signal. However, the quantization noise is still second-order noise-shaped by the modulator loop. A second-order, single-loop topology also is a good compromise between the inherent stability of lower-order (less than 2) loop structures and superior noise-shaping of higher-order loop structures.

It is important to note that the amount of signal processed by the integrators is inversely proportional to the resolution of the quantizer in this topology. Because a single-bit quantizer was selected for this design, we can expect the integrators will still process a small amount of the input. We can accept decreased performance of the modulator, compared to the performance if a multi-bit quantizer was used, because only medium resolution is desired.

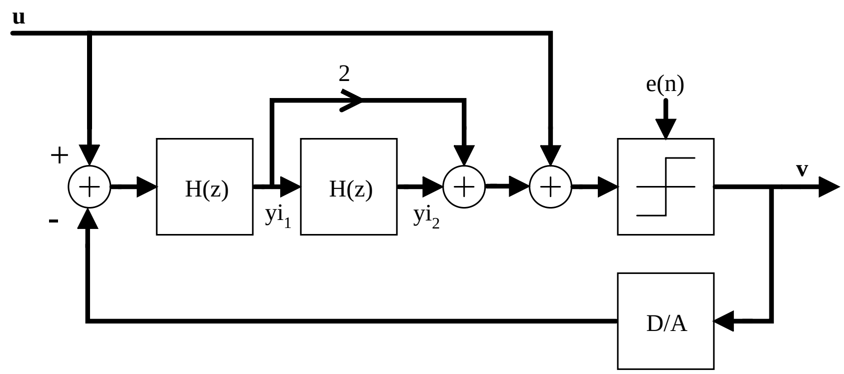


FIGURE 4.1: $\Delta\Sigma$ modulator topology presented in [1].

4.2.2 Gain Coefficient Selection

As shown in Figure 4.1, gain coefficients for the integrators and feedforward paths are selected to ensure the following:

- The gain of the input feedforward path to the comparator input is unity.
- The gain of the feedforward path from the first integrator output to the comparator input is two.
- The gain of the forward path through the two integrators and gain block is also unity.

The $\Delta\Sigma$ modulator was modeled and simulated in MATLAB. The discrete integrators are realized as forward-Euler (delaying) structures modeled with a DC gain of 60dB. This gain value was considered a conservative value given that the CDS-boosted effective gain of the inverter-based integrators should be approximately double the actual DC gain (in decibel units) of the amplifier used in the integrator (i.e. 40dB, effectively 80dB, in the amplifier described in Section 3.2). The transfer function of the integrators with finite DC gain become

$$H(z) = \left(\frac{-C_1}{C_2}\right) \cdot \frac{(1 - \frac{1}{DCGain[V/V]})z^{-1}}{1 - (1 - \frac{1}{DCGain[V/V]})z^{-1}} \tag{4.1}$$

Note as the DC gain of the gain stage used in the integrator becomes large (i.e., greater 80dB) the transfer function approaches the ideal transfer function of:

$$H(z) = \left(\frac{-C_1}{C_2}\right) \cdot \frac{z^{-1}}{1 - z^{-1}} \tag{4.2}$$

The single-bit quantizer was modeled as a uniform quantizer with two output levels. Using the gain coefficient guidelines listed at the beginning of this section, the system was simulated to achieve a signal-to-noise-and-distortion ratio (SNDR) to achieve the desired resolution. The gain coefficents found through simulation were 1, 1/2, 1/2, 4, and 4 for the input signal feed-forward path, first integrator gain, second integrator gain, first integrator output feed-forward path, and the forward signal path, respectively. These gains are illustrated in the block diagram shown in Figure 4.2. The gain of the integrators is set by the ratio of C_1 and C_2 as shown in Equations (4.1) and (4.2).

4.2.3 System Simulation Results

System simulation results from MATLAB for the $\Delta\Sigma$ modulator with the gains given in Figure 4.2 are shown in Figures 4.3 and 4.4. Figure 4.3 shows the performance of the modulator, expressed in signal-to-noise-and-distortion (SNDR),

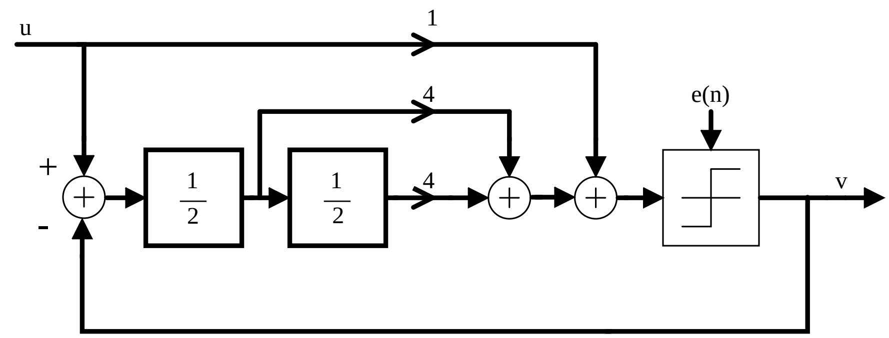


FIGURE 4.2: ΔΣ modulator gain coefficents found from Simulink simulation.

as the input signal amplitude is varied. Also plotted in Figure 4.3 is the theoretical maximum SNR calculated from

$$SNR = \frac{3\pi}{2} \cdot A_x^2 \cdot (2n+1) \cdot \left(\frac{OSR}{\pi}\right)^{2n+1} \tag{4.3}$$

where A_x is the signal amplitude and n in the ΔΣ loop order. [30] Figure 4.4 on page 29 shows results for the modulator when it was simulated with a 0.75 (normalized to the reference voltage range), 488.28125 KHz input signal. The simulation data segment was 16,384 (2^{14}) samples; this segment was taken after discarding the first 512 samples of the simulation to remove transient effects. Figure 4.4(a) (page 29) shows the histogram and spectrum of the internal state yi_1 (labeled in Figure 4.2, page 27), Figure 4.4(b) shows the histogram and spectrum of yi_2, and Figure 4.4(c) shows the output spectrum of the modulator. The calculated SNDR from this simulation was 68.7 dB.

Note that this input frequency was chosen in order to capture the first seven harmonics in the input signal band (i.e., 3.906 MHz, as defined from $f_s = 500$ MHz, $OSR = 64$, and using Equation (4.4) where f_u is the input signal band. Dithering was not applied in this simulation.

$$f_u = \frac{0.5 f_s}{OSR} \tag{4.4}$$

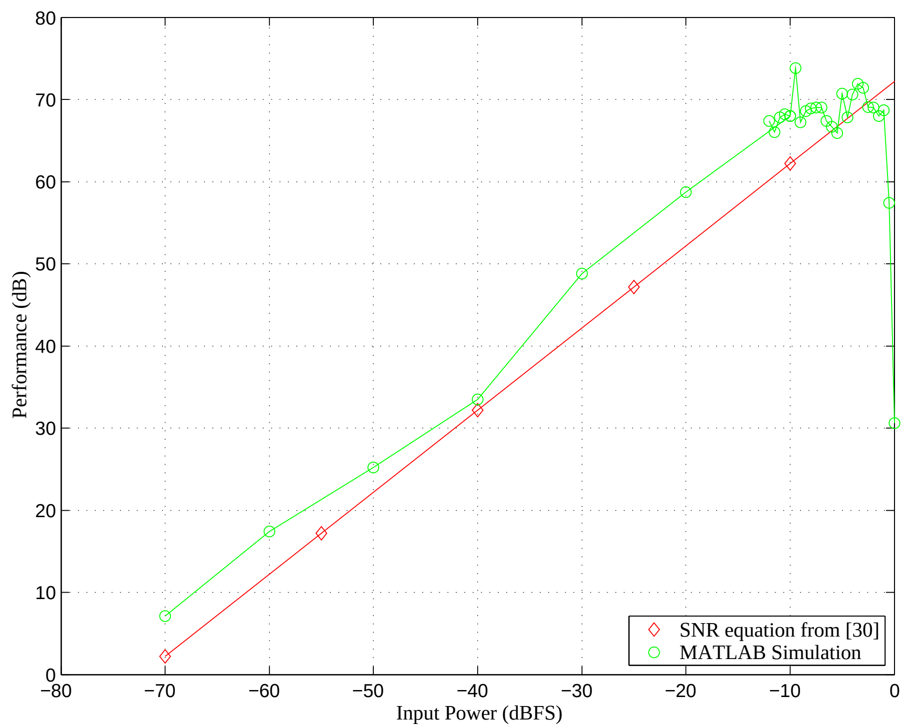
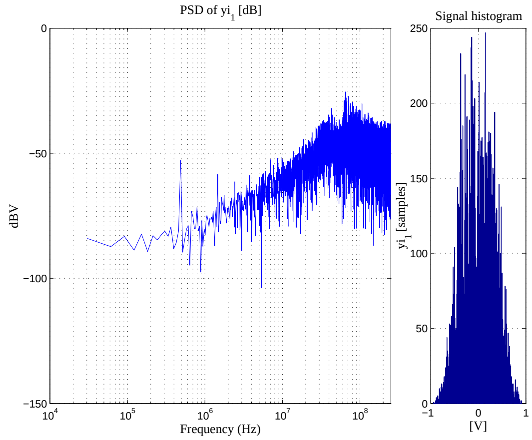
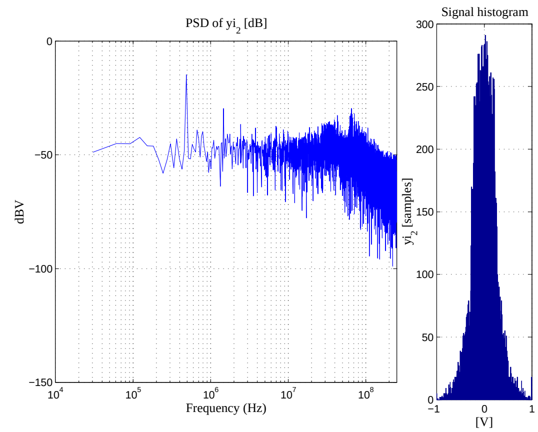


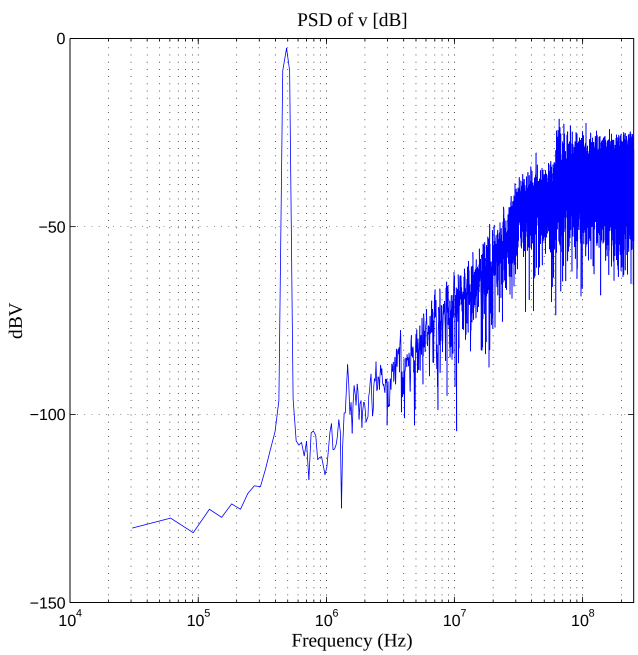
FIGURE 4.3: System simulation of input amplitude versus SNDR for the $\Delta\Sigma$ modulator.



(a) Spectrum and histogram of yi_1.



(b) Spectrum and histogram of yi_2.



(c) Output spectrum of the modulator.

FIGURE 4.4: MATLAB simulation results for the $\Delta\Sigma$ modulator

4.3 Circuit-Level Design

4.3.1 SC Integrator Design

The design of the pseudo-differential, inverted-based SC integrator was discussed in detail in Section 3. In order for the integrator to operate properly at a clock frequency of the 500 MHz, care must be taken to properly size the capacitors and switches. Improper sizing of either component could result in excessive power consumption or inadequate settling.

Because of noise and error shaping properties of the $\Delta\Sigma$ modulator, components near the input of the modulator are the most critical [20]. Thus, extra care in the design of the first integrator is important to ensure that the system meets the design goal. Another reason that the design of the first integrator is important is that it also samples the input signal, which is critical to achieve proper resolution of the conversion process.

The noise power of the first integrator can be used to calculate the size of the sampling capacitor because its noise power will dominate the noise power of the overall system. Because the modulator will incorporate double-polarity reference voltages, it will use the input capacitor for both sampling and subtracting the feedback signal from the quantizer, and it will be a differential structure, the sampling capacitor size can be calculated from Equation (4.5), where V_{ref} is the reference voltage and OL represents the overload level of the converter.[11]

$$SNR_{kT/C} = \frac{(2 \cdot OL \cdot V_{ref})^2}{2} \cdot \left(\frac{C_s \cdot OSR}{4 \cdot k \cdot T}\right) \tag{4.5}$$

Assuming conservative values of OL = 900mV, V_{ref} = 900mV, and OSR=64, it can be found that a 2pF sampling capacitance will provide $SNR_{kT/C}$= 94dB. Even though a $SNR_{kT/C}$ of approximately 72dB will provide the desired resolution, this capacitance value is a reasonable value and should provide some margin of error. Capacitance values can be scaled down for the second integrator and the summing node switches due to the noise and error shaping properties of the modulator. Therefore, the inverter-based gain stage for the second integrator can be scaled for the reduced capacitive load, reducing the power consumption of the modulator.

As explained in [11] the time constant of the sampling capacitor and the series combination of the input switches should meet the criteria:

$$\left(\frac{1}{2\pi \cdot R_{sw} \cdot C_s}\right) > 4f_s \tag{4.6}$$

where R_{sw} is the series combination of the resistances of the input switch S_1 and the sampling switch S_3 (Figure 3.5, page 21). Assumptions made in Equation (4.6) are that the DC gain of the gain stage is 80dB and that the closed-loop pole frequency is five times the sampling frequency. In this inverter-based design, the effective gain of the integrator with CDS is approximately 80dB, however the closed-loop pole frequency is only two times the sampling frequency. However, Equation (4.6)provided approximate switch sizing that was further optimized in simulation. Solving Equation (4.6) with a 2pF sampling capacitor size it can be found that the series combination of the input switch S_1 and switch S_3 must be less than 40 Ω. Note that this resistance value does account for time lost due to the non-overlap time between clock phases (see Section 4.3.4 and Figure 4.9, page 36).

To meet the low resistance requirement for the sampling time constant a CMOS switch, or transmission gate, is used as the input switch to each integrator. The CMOS switch provides reasonably good harmonic distortion performance and the two transistors tend to cancel their charge injection effects. From the equations for the on-resistance of a transistor in its triode region found in [7], and from switch simulations in SpectreS using the chosen technology models, the required input switch size was found as 60μm/0.18μm. The sampling switches for the second integrator were found in a similar manner, and scaled according to the sampling capacitor. The remaining switch sizes in both integrators were found through the analysis of signals processed by each switch, and approximate sizing in proportion to the input switch.

Note that it was a design choice not to use clock-boosting or switch bootstrapping because the resolution goal was only medium accuracy. Both of these techniques can be used to improve linearity [21].

4.3.2 One-bit Quantizer Design

The quantizer is made from a regenerative feedback comparator. Common performance errors of such a comparator are offset and hysteresis; however, $\Delta\Sigma$ modulators are quite tolerant of these errors because they are suppressed by the noise and error shaping effect (second-order in this design) of the loop [20]. Thus, a high-speed, medium-resolution comparator was selected, as presented in [2] and shown in Figure 4.5. The realized circuit was designed for a 500MHz clock frequency and consumes 1.2 mW. The unit transistor size (labeled “X” in Figure 4.5) in the drawing is 5μm.

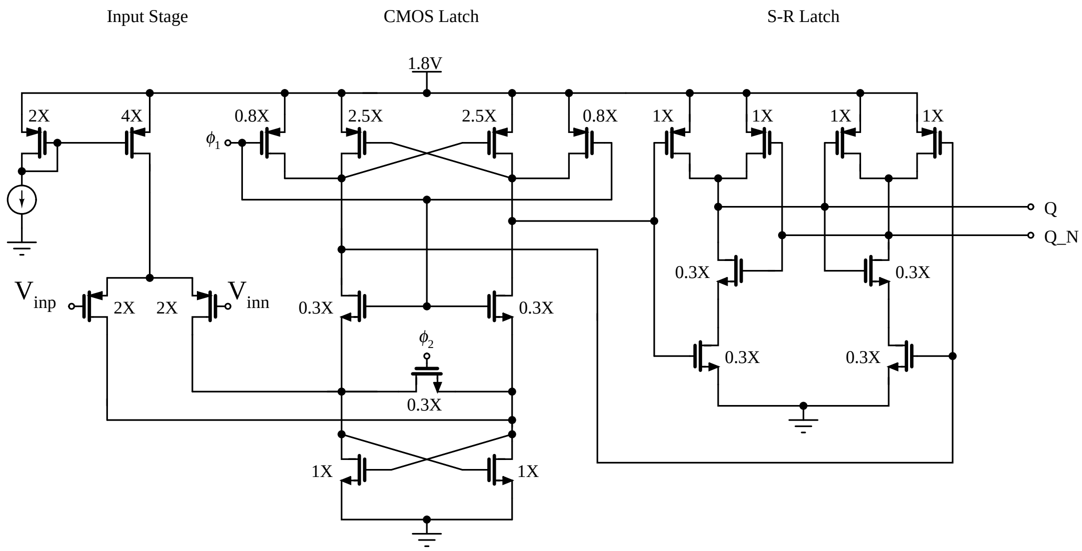


FIGURE 4.5: Regenerative feedback comparator presented in [2].

4.3.3 One-bit DAC Design

A schematic of the one-bit DAC used in the $\Delta\Sigma$ modulator is shown in Figure 4.6 [22]. To ensure proper timing of the feedback signals Q and Q_N, the AND gates U1 and U2 control delivery of the feedback signals to the input of the first integrator. The original DAC design was modified to include CMOS switches (for the switches used to inject the positive and negative reference voltages Vrefp and Vrefn) to provide low resistance and ensure fast switching. The inverters U4 and U5 provide the complementary control signal for the CMOS switches. The design was also modified to include gates U3 and U6 (the schematic of each gate is shown in Figure 4.7 and is described in [3]). These gates provide a delay that prevents ambiguous switching of the CMOS switch transistors. The delay is designed to match the propagation delay of a single inverter (i.e., the delay of gate U4 or U5).

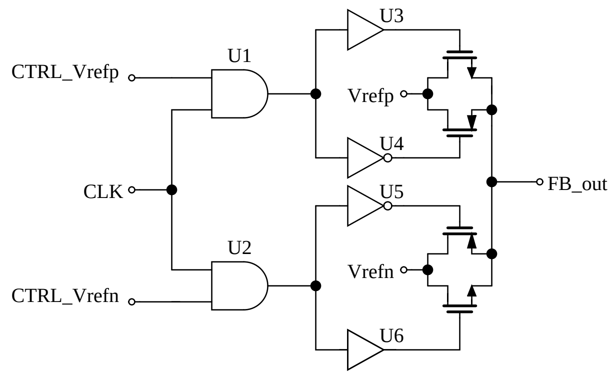


FIGURE 4.6: Single-bit DAC used in the $\Delta\Sigma$ modulator design.

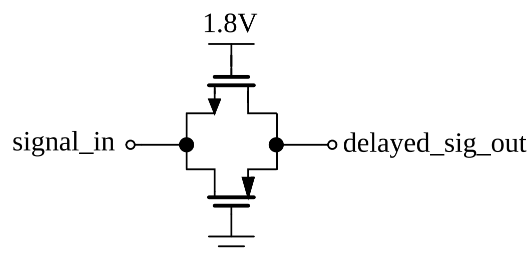


FIGURE 4.7: Delay circuit presented in [3].

4.3.4 Clock Generator Design

The clock generator shown in Figure 4.8 was presented in [4]. The circuit generates two phases and their complements (for CMOS switches). It also generates a delayed version of each phase to use for reducing signal-dependent charge injection. A design feature is that the circuit only delays the falling edge of the clock phases, making it especially suitable for high speed designs.

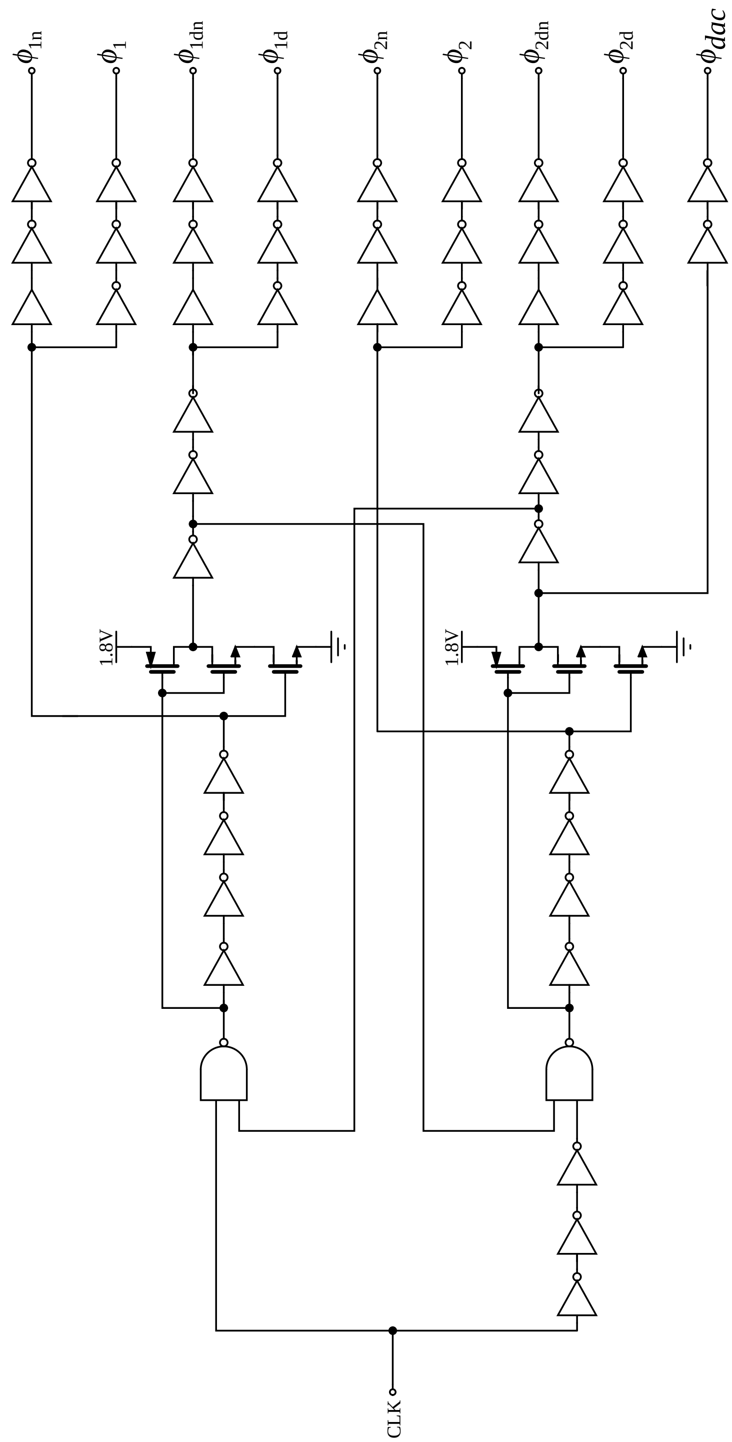


FIGURE 4.8: Clock generator presented in [4].

Note that the buffers shown in schematic were realized with the delay circuit shown in Figure 4.7 and scaled to match the propagation delay of one inverter in the clock generator. The timing of the clock phases is shown in Figure 4.9.

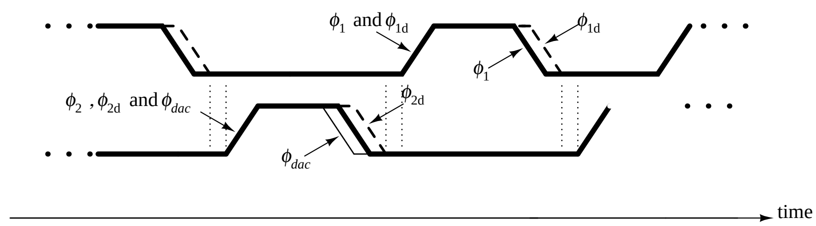


FIGURE 4.9: Timing diagram of the clock generator.

4.3.5 Overall System Schematic

The overall system schematic of the fast, opamp-free $\Delta\Sigma$ modulator is shown in Figure 4.10. Note that the pseudo-differential, inverted-based gain stages of the integrators are represented with an alternate symbol [5] instead of at the transistor level to simplify the drawing.

Also note this drawing shows the realization of the summing node in front of the comparator. Switches labeled S_{sn1}, S_{sn2}, and S_{sn5}were implemented using CMOS switches. Switches labeled S_{sn3}, S_{sn4}, and S_{sn6} were implemented using NMOS switches.

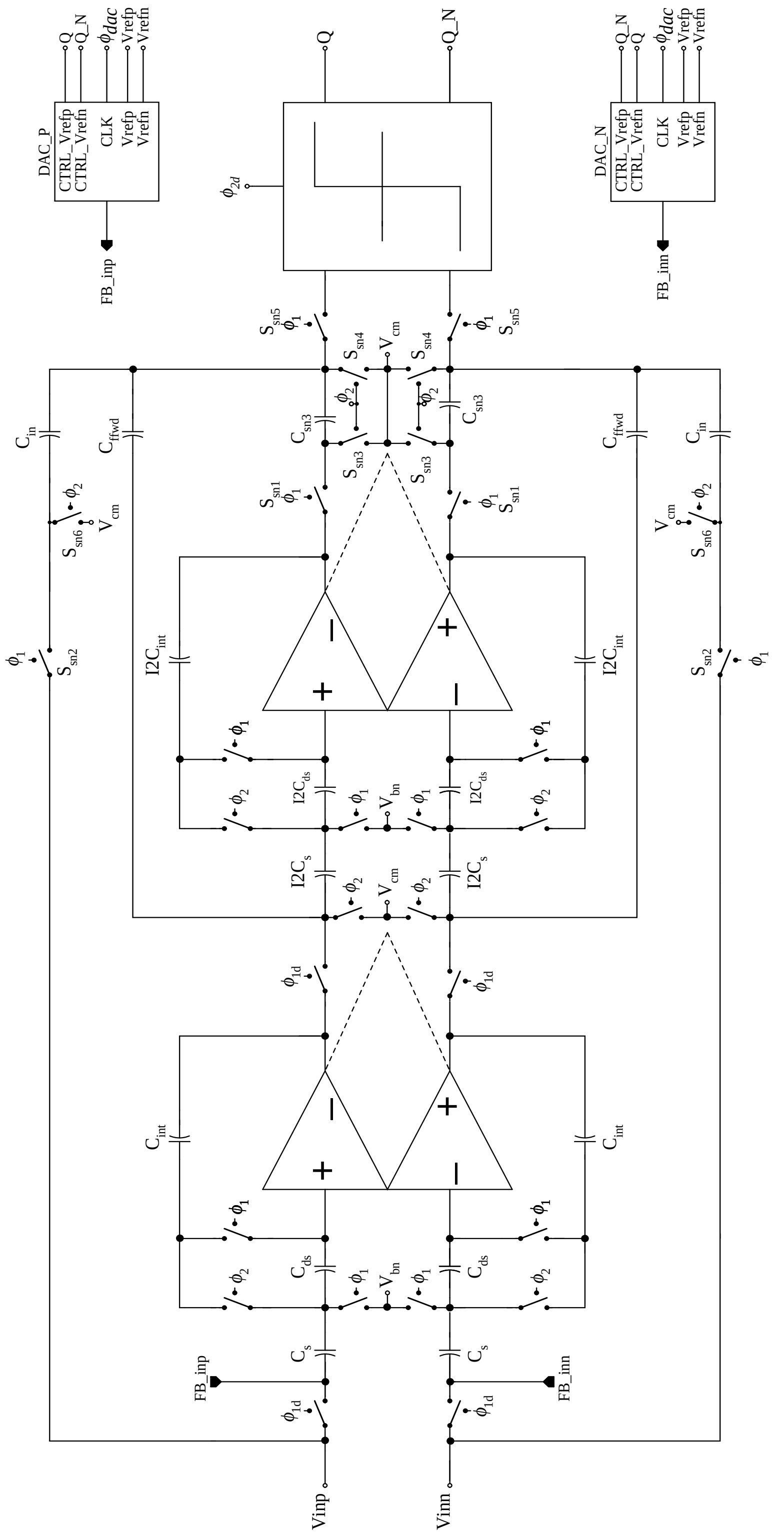


FIGURE 4.10: Overall schematic of the inverter-based ΔΣ modulator.

5. SIMULATION RESULTS

The following sections present transistor-level simulations of the fast opamp-free $\Delta\Sigma$ modulator. These results will be compared to system-level simulations and their differences will be discussed.

5.1 Simulation Overview

Simulations were performed assuming a 1.8V, 0.18μm, 5-metal layer process technology. Poly-to-poly capacitors are available in the process and were used in place of ideal capacitors in all transistor-level simulations.

5.2 Output Plots

A transistor-level simulation result of the fast opamp-free $\Delta\Sigma$ modulator is shown in Figure 5.1. Note that the clock signals for this simulation were generated from ideal pulse waveform sources. An input amplitude of -2.5 dBFS was used for the simulation because this input level is near the predicted maximum SNDR of the modulator (i.e., based on the MATLAB simulations plotted in Figure 4.3, page 28). The input frequency was 488.28125 kHz, to match the frequency chosen for the MATLAB simulations and to capture the first seven harmonics in the desired signal band (i.e., 3.906 MHz). A total of 8192 points were used for the simulation, after the first 512 points were removed to avoid transient effects. The calculated SNDR from this simulation was 61.6dB.

An unexpected result is this simulation was the observed harmonic distortion. The third harmonic had a peak value of -72 dBFS and the fifth harmonic had a

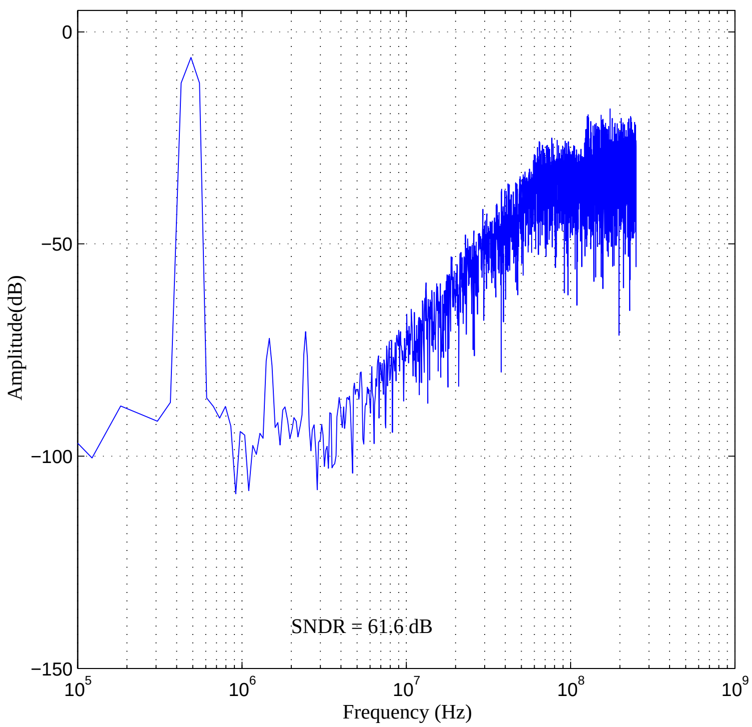


FIGURE 5.1: Transistor-level system simulation for a 488.28125kHz, -2.5dBFS sinusoidal input.

peak value of -70 dBFS. The harmonic distortion degraded the performance of the modulator from the predicted value.

Next, a series of SNDR simulations were run, with the input amplitude varying from -50 dBFS to -1 dBFS. The stepping of input amplitude was chosen to show more detail near the predicted maximum SNDR input value. The results of these simulations are shown in Figure 5.2. A total of 8192 points were used for each simulation, after discarding the first 512 points.

Also plotted in Figure 5.2 are the Matlab system simulation results, originally shown in Figure 4.3, and SpectreS system simulation results shown for a transistor-level quantizer and all other components modeled as "ideal" (i.e., low resistance linear switches were used for the switches in these components, and the amplifiers were modeled with single-pole ideal voltage-controlled voltage sources). Results from the MATLAB system simulations and SpectreS system simulations with transistor-level quantizer only show good agreement; confirming the setup in SpectreS.

A series of simulations transitioning between the two SpectreS simulation cases (i.e., transistor-level quantizer only and all transistor-level components except the clock generator) were run to help diagnose the source of the harmonic distortion. The flow of the transition was from the output of the modulator to the input because the noise and error-shaping properties of the $\Delta\Sigma$ loop cause the input components to have a greater influence on the system performance. A half-scale amplitude input was chosen to minimize the effects of integrator overload. The same input frequency as previous tests (i.e., 488.28125 KHz) was used. A total of 8192 points were used in each simulation, after removing the first 512 points.

The results of the transitional SpectreS simulations are shown in Figure 5.3 Figure 5.4, and Figure 5.5. The system output when a transistor-level quantizer was added to the simulation is shown in Figure 5.3(a). Figure 5.3(b) displays the result when the summing node before the quantizer was realized with transistors.

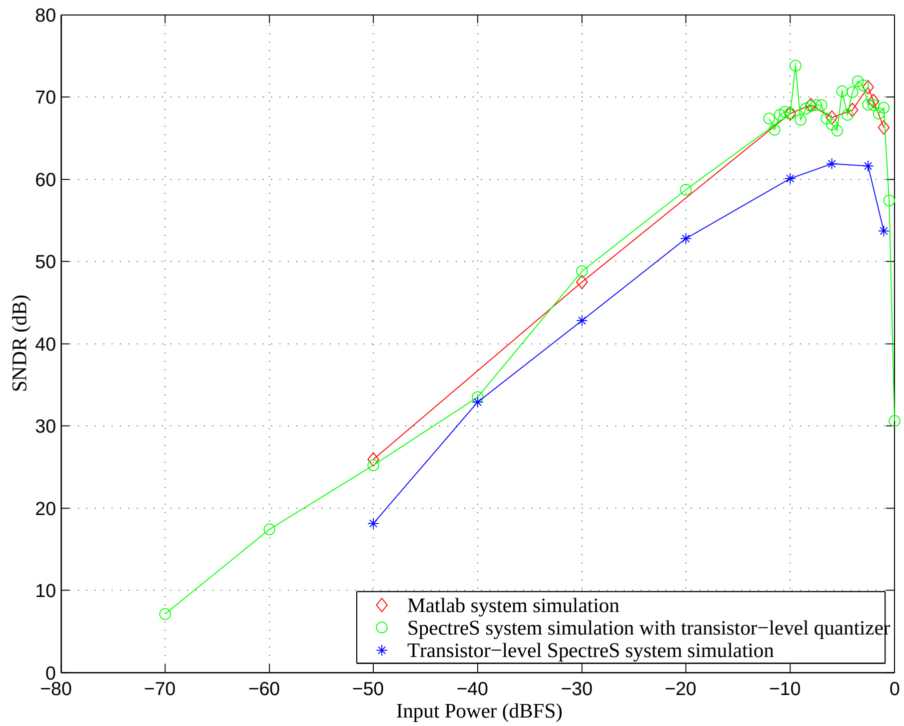
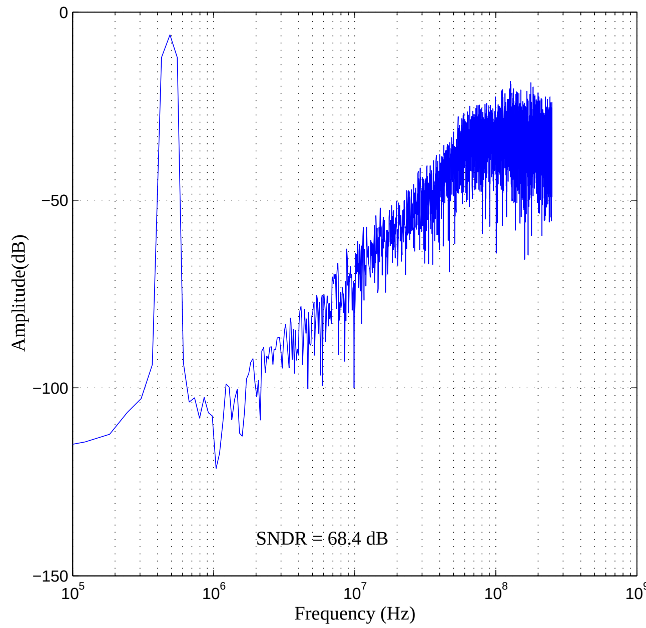


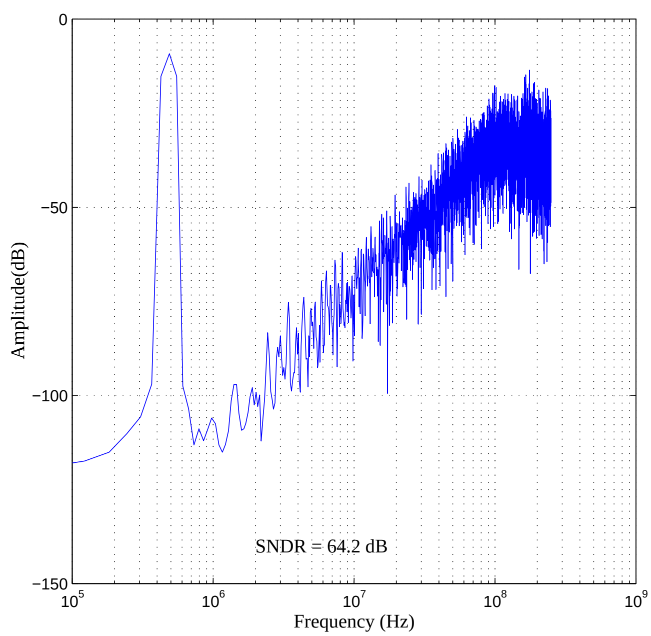
FIGURE 5.2: Input versus SNDR plots, for MATLAB system simulations, SpectreS system simulations with only the quantizer simulated to the transistor level, and full transistor-level SpectreS system simulations (except clock generator).

The system output when a transistor-level second integrator was added is shown in Figure 5.4(a). Figure 5.4(b) displays the modulator output spectrum when a transistor-level first integrator was added. Lastly, the system output spectrum when all transistor-level components (except the clock generator) were used is shown in Figure 5.2.

The transitional simulation results show that the system performance is degraded most severely by the introduction of the transistor-level first integrator. From Figure 5.4(b) it appears the introduction of the first integrator causes the noise floor, and peak value of the third harmonic, to increase significantly. Resizing the switches, or possibly replacing all switches with CMOS switches would reduce node impedances and lead to more complete charge transfer. Of course, increases in switch sizes would be limited by the amount of tolerable charge injection from the switches.

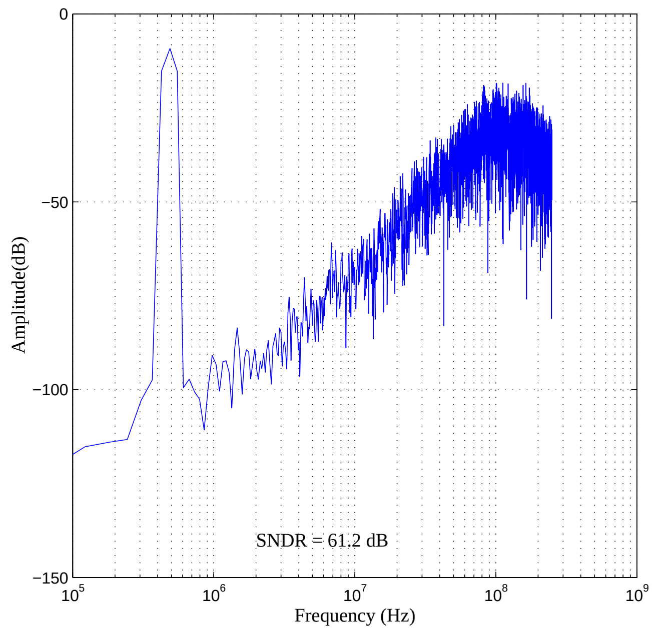


(a) Transistor-level quantizer only.

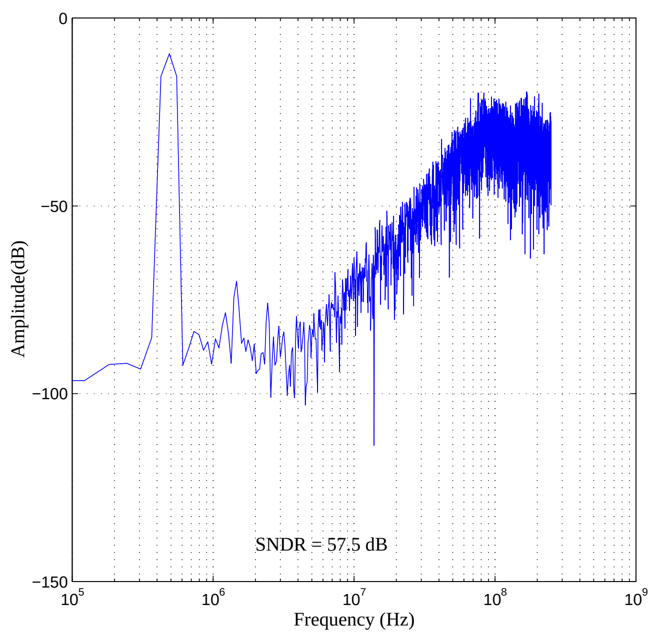


(b) Added transistor-level summing node.

FIGURE 5.3: Spectre transitional simulation results for the $\Delta\Sigma$ modulator



(a) Added transistor-level second integrator.



(b) Added transistor-level first integrator.

FIGURE 5.4: Continuation of Spectre transitional simulation results for the $\Delta\Sigma$ modulator

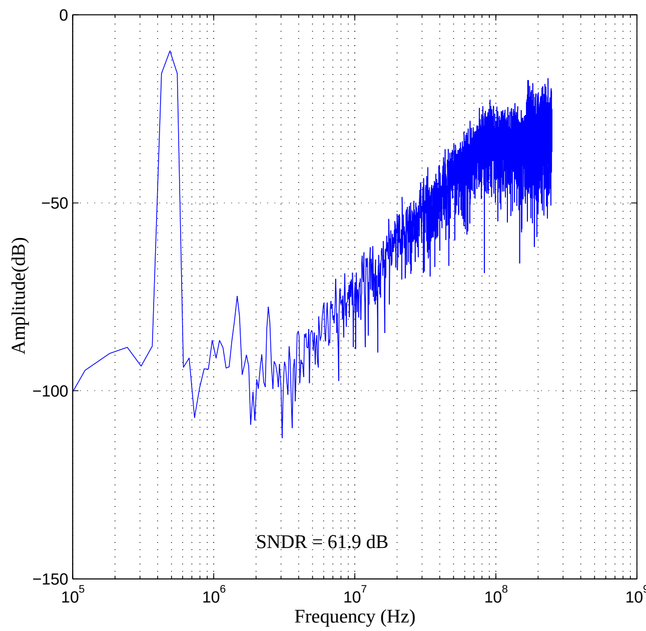


FIGURE 5.5: Real feedback DAC's added.

Another major contributor of performance degradation are the feedback DAC's. They are also likely distortion sources since they tied to the input of the $\Delta\Sigma$ loop. Careful redesign of switch sizing or control logic should correct most of the errors introduced by the DAC's.

Another possible source of distortion could be improper timing of the feedback operation. Because the summing node in front of the quantizer introduces some additional delay in the loop, care must be taken to properly time the comparison operation in the quantizer and subtraction of the feedback signal from the input.

The chosen simulation setup is yet another possible reason why the system performance did not meet the designed response. The accuracy setting of the transistor-level simulator (in this case SpectreS) could impact the simulated system performance. A moderate accuracy setting was chosen for all simulations presented in this section because "ideal" (as described above) SpectreS simulations showed good agreement with MATLAB simulations. Better results may have been achieved with a conservative setting, but because the setting would also increase the simulation time. Another test setup parameter chosen for these test was the number of points. The number of points used for simulations in this section of this thesis was 8192 points, extracted after 512 points were removed to avoid measuring transient effects. This value was selected as a compromise between simulation time and reasonable observation of the output spectrum. A larger number of points should result in a decreased noise floor, however the sacrifice is longer simulation time.

6. LAYOUT FLOORPLAN

The following section describes a preliminary layout floorplan for the fast opamp-free $\Delta\Sigma$ modulator. The floorplan drawing is presented, followed by a brief justification of the component block placement in the layout.

6.1 Preliminary Floorplan

Following guidelines and suggestions in [23] the following preliminary floorplan shown in Figure 6.1 is proposed. The first integrator is constructed from the regions labeled "Amp 1p" and "Amp 1n" (i.e., the two inverter amplifiers of the pseudo-differential structure), "A1pCAPS" and "A1nCAPS" (i.e., the capacitor arrays for the integrator), "Bias 1" (i.e., the bias circuit for Amp 1p and Amp2n) and a portion of each region labeled "Switches". The cells forming the second integrator follow a similar labeling scheme. The comparator is contained in the cell labeled "Comp".

The design provides good separation of analog and digital circuitry. The symmetric nature of the floorplan equalizes trace lengths for each signal path to improve delay matching. Guard rings around the capacitor arrays and analog circuit region improve the separation of the two signal types.

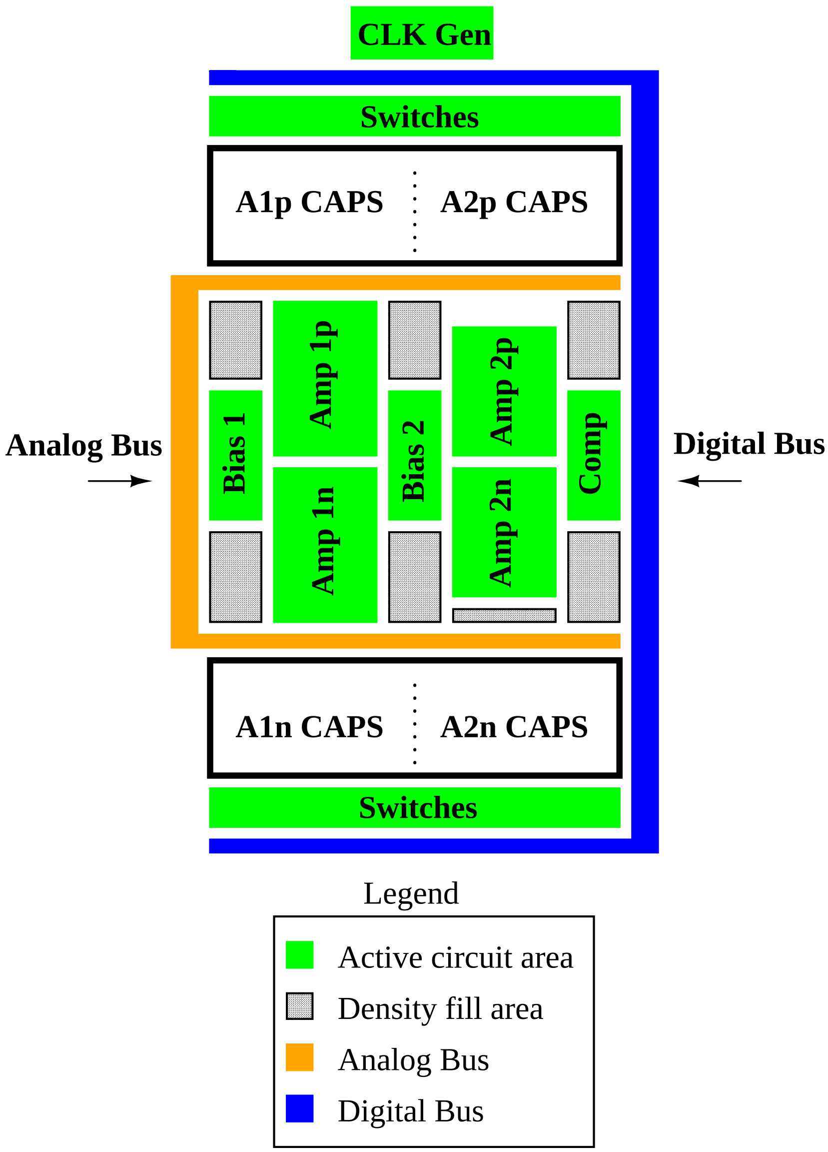


FIGURE 6.1: Preliminary floorplan for the fast opamp-free $\Delta\Sigma$ modulator.

Another feasible floorplan for the $\Delta\Sigma$ modulator is shown in Figure 6.2 [24]. The first integrator is formed from the regions labeled "A1p" and "A1n" (i.e., the inverter amplifiers the pseudo-differential integrator), the region labeled "B1" (i.e., the bias circuit for the amplifiers A1p and A1n), and a portion of the "Capacitor Array" region, and a portion of the "Switches" region. The cells forming the second integrator follow a similar labeling scheme. This design also provides good isolation of the analog and digital signals, along with easier routing of the power supply connections than the floorplan presented in Figure 6.1.

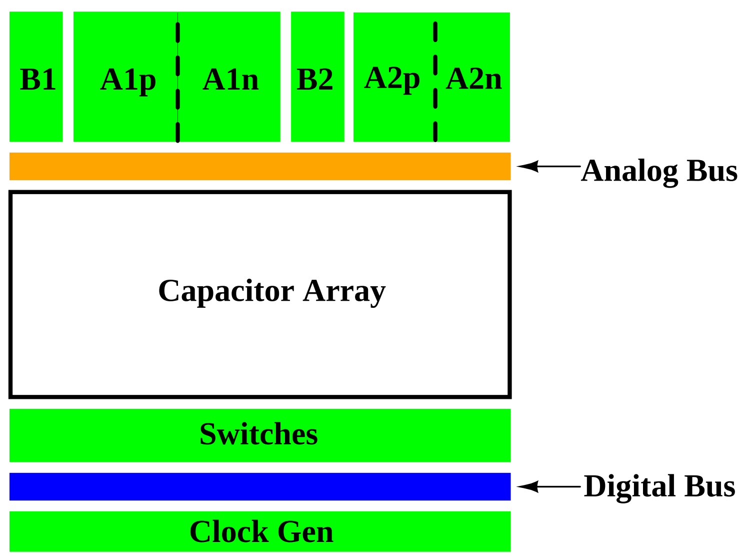


FIGURE 6.2: Another possible floorplan for the fast opamp-free $\Delta\Sigma$ modulator.

6.2 Layout Comments

The layout of this high-speed circuit is not trivial. Great care will need to be taken in minimizing trace lengths and avoiding crossing of the analog and digital signal lines. Ideally the layout and final optimization of the modulator would be an iterative process; i.e., an initial layout of the circuit would be extracted with parasitic capacitances and analyzed. Then, layout changes would be made and this new layout would be extracted with parasitics. The process would be repeated until the desired performance was achieved.

Because the transistors of the gain stages are wide, they should be laid out with multiple fingers to improve area use and reduce gate resistance of the devices. Lastly, the amplifiers were designed such that the cascoded transistors were sized the same width in each case. Given this fact, the devices could share the same junctions for their drain and source regions, thereby significantly reducing the capacitance at these junctions [3].

7. CONCLUSIONS

In this thesis a fast opamp-free $\Delta\Sigma$ modulator was implemented using inverter-based SC integrators. The designed modulator operated at a clock frequency of 500MHz.

7.1 Summary

This thesis explored replacing opamps with a simpler, faster inverter amplifier. A pseudo-differential structure and CDS techniques were used to compensate for shortcomings of the inverter amplifier. The feasibility of these inverter-based SC circuits was tested by using them in a high-speed $\Delta\Sigma$ modulator design.

The single-stage structure of the inverter amplifier made it difficult to design for high-speed operation and still achieve reasonable gain and output swing. Unlike a typical opamp where the overall gain is typically achieved with multiple stages, the gain for the inverter was boosted by cascoding the currrent mirror transistor, and by applying CDS techniques. However, even after applying these techniques, the realized integrator required large transistors and significant power consumption when used as the first integrator in the designed $\Delta\Sigma$ modulator.

7.2 Future Research

An extension of this thesis work in $\Delta\Sigma$ A/D converters would be to use a combination of inverter-based and opamp-based integrators in the converter design. Because the design requirements are relaxed for all integrators after the first, inverter-based integrators could be used for all other integrators in the design, therefore saving die area and conserving power.

This thesis work showed that if the $\Delta\Sigma$ A/D converter is constructed from inverter-based integrators only, a fast, medium resolution converter could be realized. This work could be extended to other variations of $\Delta\Sigma$ modulators. For example, inverter-based integrators could be used in cascade or higher-order $\Delta\Sigma$ modulators to improve resolution. Alternatively, inverter-based integrators could be used in $\Delta\Sigma$ modulators with multi-bit quantization to reduce the oversampling requirements (i.e., lower OSR), and thus achieve a wider input bandwidth.

High-speed filters could also be constructed using the inverter-based integrators. Limited linearity of the integrators would restrict their use to high frequency filters applications with relaxed harmonic distortion requirements.

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